# N-Channel Enhancement-Mode MOS Transistor

## 2N7002

### DESCRIPTION

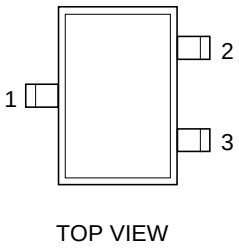
Calogic's 2N7002 device type is a vertical DMOS FET transistor housed in a surface mount SOT-23 for micro-assembly applications. The device is an excellent choice for switching applications where breakdown ($B_V$) and low on-resistance are important.

### ORDERING INFORMATION

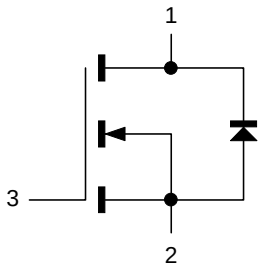
| Part | Package | Temperature Range |
|---|---|---|
| 2N7002 | Plastic SOT-23 Package | -55°C to +150°C |
| X2N7002 | Sorted Chips in Carriers | -55°C to +150°C |

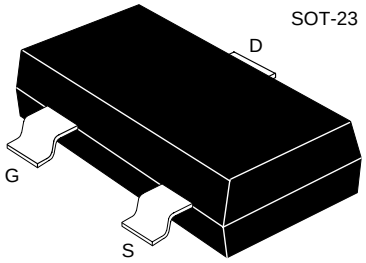
### PIN CONFIGURATION

1 DRAIN
2 SOURCE
3 GATE




TOP VIEW




**CD5**

### PRODUCT SUMMARY

| $V_{(BR)DSS}$ (V) | $r_{DS(ON)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| 60 | 7.5 | 0.115 |

| PRODUCT MARKING | |
|---|---|
| 2N7002 | V02 |

calogic CORPORATION

**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise specified)

| SYMBOL | PARAMETERS | LIMITS | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 60 | V | |
| $V_{GS}$ | Gate-Source Voltage | ±40 | | |
| $I_D$ | Continuous Drain Current | 0.115 | A | $T_A$ = 25°C |
| | | 0.073 | | $T_A$ = 100°C |
| $I_{DM}$ | Pulsed Drain Current[1] | 0.8 | | |
| $P_D$ | Power Dissipation | 200 | mW | $T_A$ = 25°C |
| | | 80 | | $T_A$ = 100°C |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | °C | |
| $T_{stg}$ | Storage Temperature Range | -55 to 150 | | |
| $T_L$ | Lead Temperature (1/16" from case for 10 sec.) | 300 | | |

**THERMAL RESISTANCE RATINGS**

| SYMBOL | THERMAL RESISTANCE | LIMITS | UNITS |
|---|---|---|---|
| $R_{thJA}$ | Junction-to-Ambient | 625 | K/W |

NOTE: 1. Pulse width limited by maximum junction temperature.

**SPECIFICATIONS**[1]

| SYMBOL | PARAMETER | MIN | TYP[2] | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| **STATIC** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | 60 | 70 | | V | $I_D$ = 10µA, $V_{GS}$ = 0V |
| $V_{GS(th)}$ | Gate-Threshold Voltage | 1 | 1.9 | 2.5 | | $V_{DS}$ = $V_{GS}$, $I_D$ = 0.25mA |
| $I_{GSS}$ | Gate-Body Leakage | | | ±100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | | | 1 | µA | $V_{DS}$ = 60V, $V_{GS}$ = 0V |
| | | | | 500 | | $T_C$ = 125°C |
| $I_{D(ON)}$ | On-State Drain Current[3] | 500 | 1000 | | mA | $V_{DS}$ = ≥2$V_{DS(ON)}$, $V_{GS}$ = 10V |
| $r_{DS(ON)}$ | Drain-Source On-Resistance[3] | | 5 | 7.5 | Ω | $V_{GS}$ = 5V, $I_D$ = 50mA |
| | | | 9 | 13.5 | | $T_C$ = 125°C |
| | | | 2.5 | 7.5 | | $V_{GS}$ = 10V, $I_D$ = 0.5A |
| | | | 4.4 | 13.5 | | $T_C$ = 125°C |
| $V_{DS(ON)}$ | Drain-Source On-Voltage[3] | | 0.25 | 0.375 | V | $V_{GS}$ = 5V, $I_D$ = 50mA |
| | | | 1.25 | 3.75 | | $V_{GS}$ = 10V, $I_D$ = 0.5A |
| | | | 2.2 | 6.75 | | $T_C$ = 125°C[4] |
| $g_{FS}$ | Forward Transconductance[3] | 80 | 170 | | mS | $V_{DS}$ = 10V, $I_D$ = 0.2A |
| $g_{OS}$ | Common Source Output Conductance[3, 4] | | 500 | | µS | $V_{DS}$ = 5V, $I_D$ = 50mA |
| **DYNAMIC** | | | | | | |
| $C_{iss}$ | Input Capacitance | | 16 | 50 | pF | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1MHz |
| $C_{oss}$ | Output Capacitance[4] | | 11 | 25 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | 2 | 5 | | |
| **SWITCHING** | | | | | | |
| $t_{ON}$ | Turn-On Time | | 7 | 20 | nS | $V_{DD}$ = 30V, $R_L$ = 150Ω, $I_D$ = 0.2A<br>$V_{GEN}$ = 10V, $R_G$ = 25Ω<br>(Switching time is essentially independent of operating temperature) |
| $t_{OFF}$ | Turn-Off Time | | 7 | 20 | | |

NOTES: 1. $T_A$ = 25°C unless otherwise specified.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = ≤80µS, duty cycle ≤1%.
4. This parameter not registered with JEDEC.