



# 2N7002KDW

## 60V N-Channel Enhancement Mode MOSFET - ESD Protected

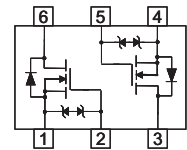
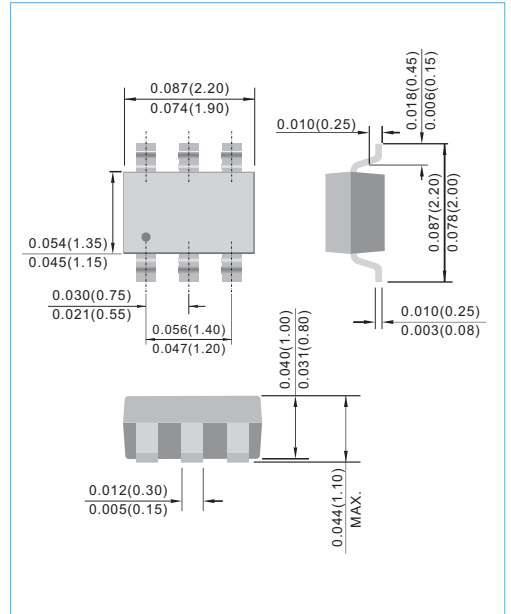
### FEATURES

- $R_{DS(ON)}, V_{GS}@10V, I_{DS}@500mA=3\Omega$
- $R_{DS(ON)}, V_{GS}@4.5V, I_{DS}@200mA=4\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Very Low Leakage Current In Off Condition
- Specially Designed for Battery Operated Systems, Solid-State Relays  
Drivers : Relays, Displays, Lamps, Solenoids, Memories, etc.
- ESD Protected 2KV HBM
- Lead free in comply with EU RoHS 2002/95/EC directives.
- Green molding compound as per IEC61249 Std. . (Halogen Free)

### MECHANICAL DATA

- Case: SOT-363 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0002 ounces, 0.006 grams
- Marking : K27

### SOT-363 Unit : inch(mm)



### Maximum RATINGS and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted )

PARAMETER	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	115	mA
Pulsed Drain Current <sup>1)</sup>	$I_{DM}$	800	mA
Maximum Power Dissipation	$P_D$	200 120	mW
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to + 150	$^\circ\text{C}$
Junction-to Ambient Thermal Resistance(PCB mounted) <sup>2)</sup>	$R_{\theta JA}$	625	$^\circ\text{C/W}$

Note: 1. Maximum DC current limited by the package  
2. Surface mounted on FR4 board,  $t < 5$  sec

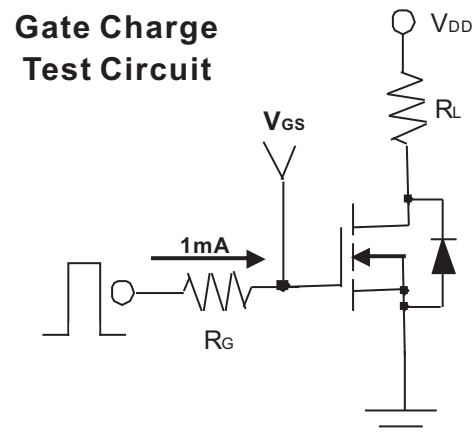
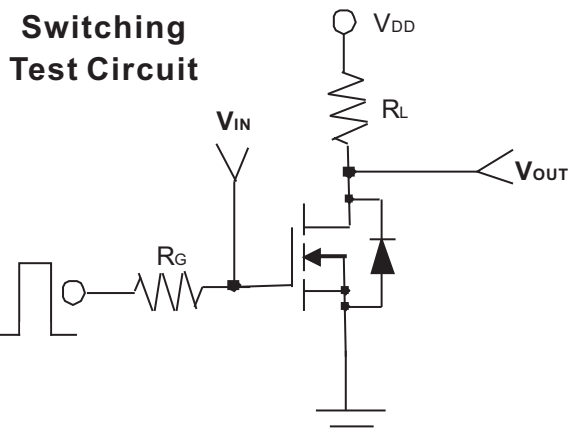
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## ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=10\mu A$	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=200mA$	-	-	4.0	$\Omega$
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=500mA$	-	-	3.0	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	1	$\mu A$
Gate Body Leakage	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 10$	$\mu A$
Forward Transconductance	$g_{fs}$	$V_{DS}=15V, I_D=250mA$	100	-	-	mS
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=15V, I_D=200mA$ $V_{GS}=4.5V$	-	-	0.8	nC
Turn-On Delay Time	$t_{on}$	$V_{DD}=30V, R_L=150\Omega$ $I_D=200mA, V_{GEN}=10V$ $R_G=10\Omega$	-	-	20	ns
Turn-Off Delay Time	$t_{off}$		-	-	40	
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V$ $f=1.0MHz$	-	-	35	pF
Output Capacitance	$C_{oss}$		-	-	10	
Reverse Transfer Capacitance	$C_{rss}$		-	-	5	
<b>Source-Drain Diode</b>						
Diode Forward Voltage	$V_{SD}$	$I_S=200mA, V_{GS}=0V$	-	0.82	1.3	V
Continuous Diode Forward Current	$I_S$	-	-	-	115	mA
Pulsed Diode Forward Current	$I_{SM}$	-	-	-	800	mA





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Typical Characteristics Curves ( $T_A=25^\circ\text{C}$ , unless otherwise noted)

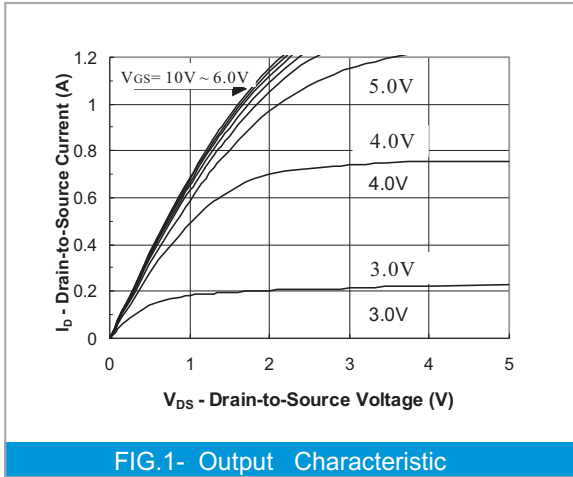


FIG.1- Output Characteristic

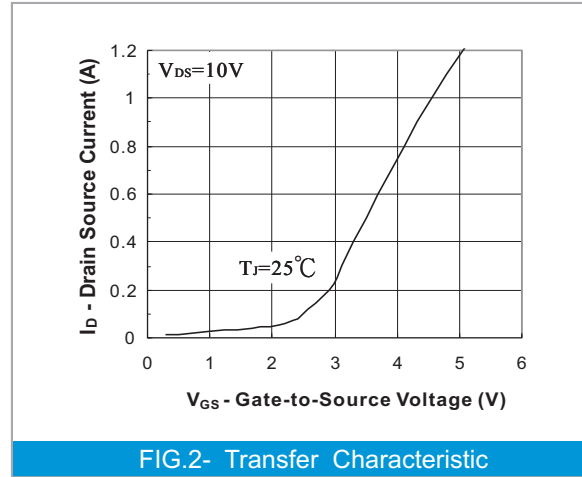


FIG.2- Transfer Characteristic

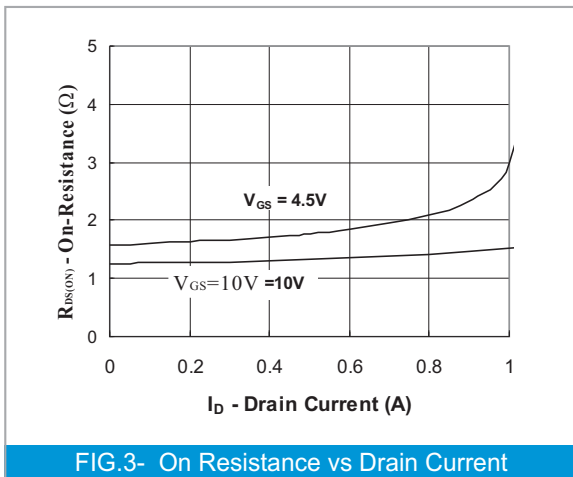


FIG.3- On Resistance vs Drain Current

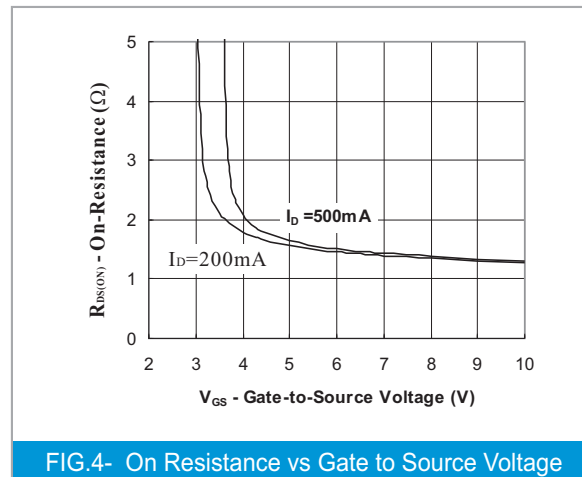


FIG.4- On Resistance vs Gate to Source Voltage

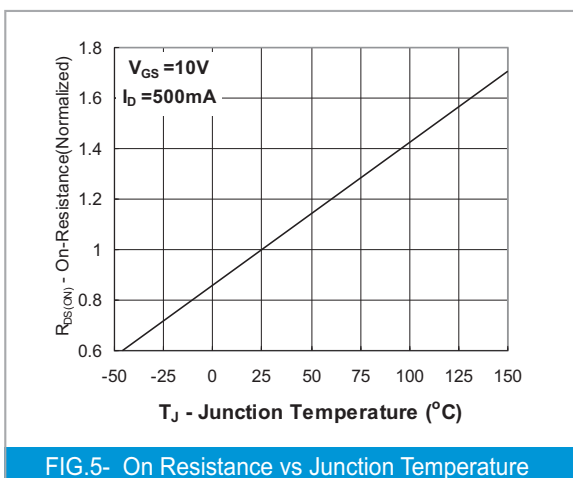
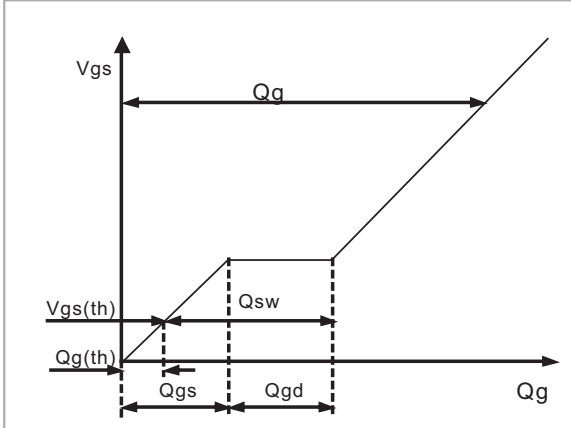


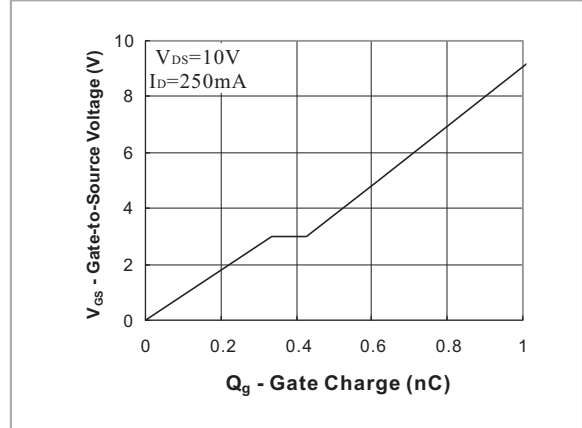
FIG.5- On Resistance vs Junction Temperature



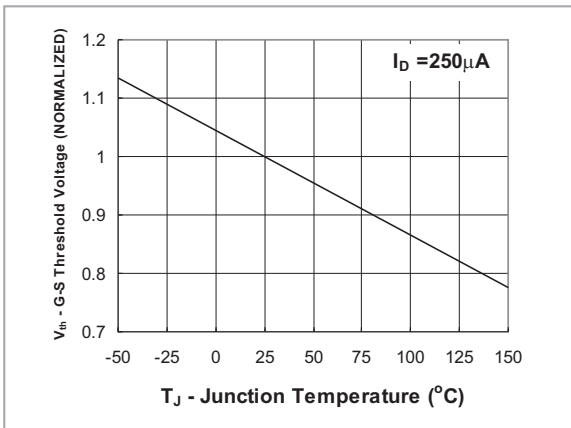
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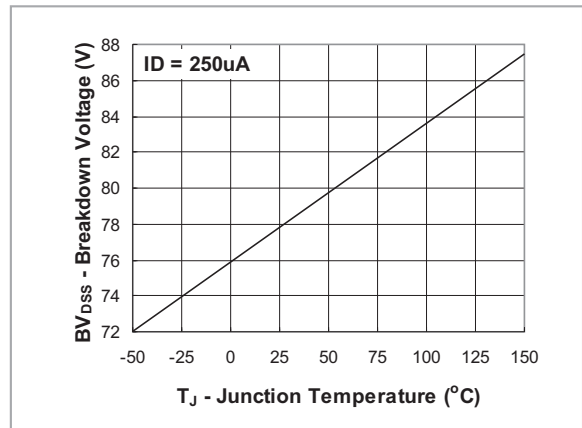
**Fig. 6 - Gate Charge Waveform**



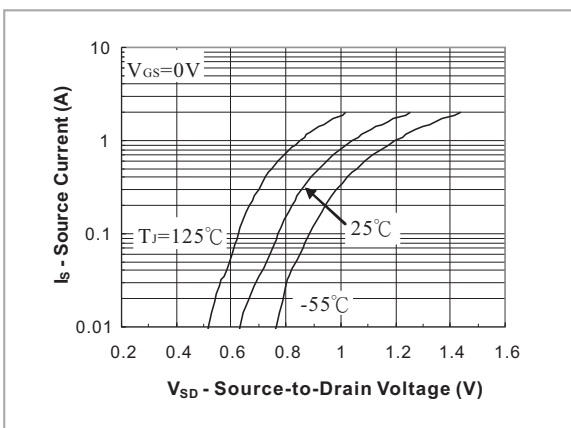
**Fig. 7 - Gate Charge**



**Fig. 8 - Threshold Voltage vs Temperature**



**Fig. 9 - Breakdown Voltage vs Junction Temperature**

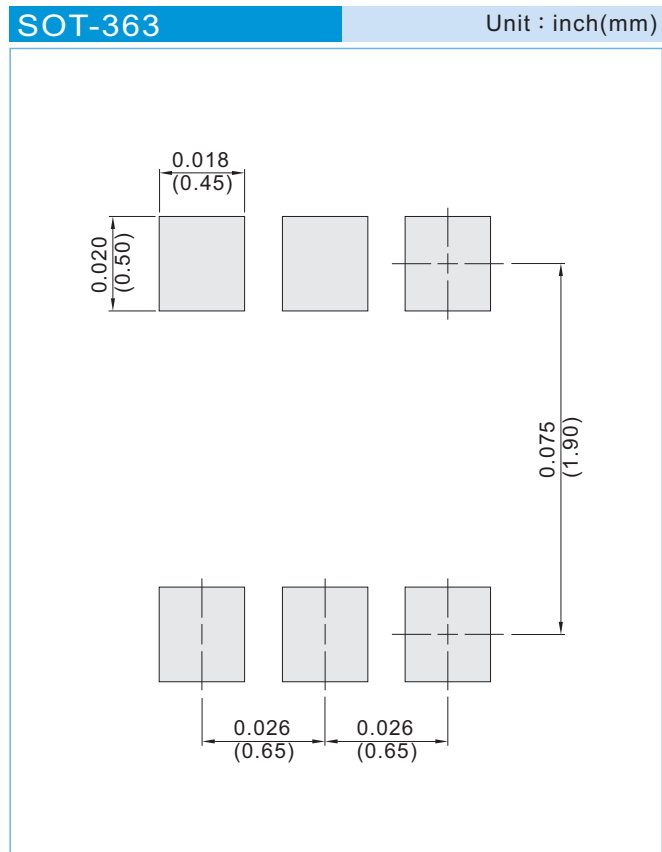


**Fig. 10 - Source-Drain Diode Forward Voltage**



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## MOUNTING PAD LAYOUT



### ORDER INFORMATION

- Packing information  
T/R - 10K per 13" plastic Reel  
T/R - 3K per 7" plastic Reel

### LEGAL STATEMENT

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For example :

RB500V-40\_R2\_00001



Packing Code <b>XX</b>				Version Code <b>XXXXXX</b>		
Packing type	1 <sup>st</sup> Code	Packing size code	2 <sup>nd</sup> Code	HF or RoHS	1 <sup>st</sup> Code	2 <sup>nd</sup> ~5 <sup>th</sup> Code
T/B	A	N/A	0	HF	0	serial number
T/R	R	7"	1	RoHS	1	serial number
B/P	B	13"	2			
T/P	T	26mm	X			
TRR	S	52mm	Y			
TRL	L	PBCU	U			
FORMING	F	PBCD	D			

Part No\_packing code\_Version

2N7002KDW\_R1\_00001

2N7002KDW\_R2\_00001

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