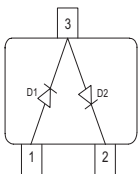


Silicon PIN Diode Array

- Surge protection device
- Designed for surge overvoltage clamping in antiparallel connection
- Pb-free (RoHS compliant) package


BAR66


Type	Package	Configuration	L_S (nH)	Marking
BAR66	SOT23	series	1.8	PMs

Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	150	V
Forward current	I_F	200	mA
Total power dissipation $T_s \leq 25^\circ\text{C}$	P_{tot}	250	mW
ESD contact discharge ¹⁾	V_{ESD}	25	kV
Peak pulse current ($t_p = 8 / 20 \mu\text{s}$) ²⁾	I_{pp}	12	A
Junction temperature	T_j	150	°C
Operating temperature range	T_{op}	-55 ... 125	
Storage temperature	T_{stg}	-55 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ³⁾ , BAR 66	R_{thJS}	≤ 290	K/W

¹⁾ V_{ESD} according to IEC61000-4-2, only valid if pin 1 and pin 2 are connected

²⁾ I_{pp} according to IEC61000-4-5, only valid if pin 1 and pin 2 are connected

³⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

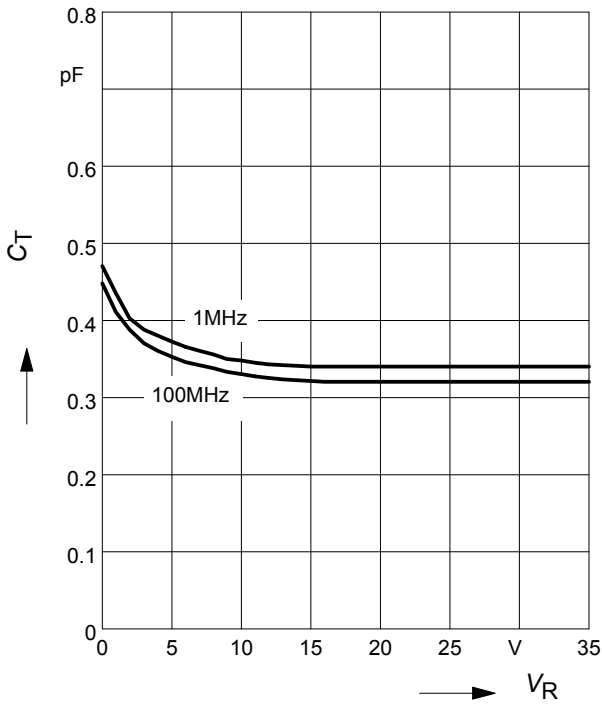
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Breakdown voltage $I_{(BR)} = 5 \mu\text{A}$	$V_{(BR)}$	150	-	-	V
Reverse current $V_R = 100 \text{ V}$	I_R	-	-	20	nA
Forward voltage $I_F = 50 \text{ mA}$	V_F	-	0.95	1.2	V
Clamping voltage $V_{ESD} = \pm 15 \text{ kV (contact)}^1$ $I_{PP} = 12 \text{ A}, t_p = 8/20 \mu\text{s}^2$	V_{CL}	-	tbd 7	-	
AC Characteristics					
Diode capacitance $V_R = 35 \text{ V}, f = 1 \text{ MHz}$ $V_R = 0 \text{ V}, f = 100 \text{ MHz}$	C_T	-	0.4 0.35	0.6 0.9	pF
Zero bias conductance $V_R = 0 \text{ V}, f = 1 \text{ GHz}$	g_P	-	220	-	μS
Forward resistance $I_F = 5 \text{ mA}, f = 100 \text{ MHz}$	r_f	-	1.5	1.8	Ω
Charge carrier life time $I_F = 10 \text{ mA}, I_R = 6 \text{ mA}$, measured at $I_R = 3 \text{ mA}$, $R_L = 100 \Omega$	τ_{rr}	-	0.7	-	μs

¹ V_{ESD} according to IEC61000-4-2, only valid if pin 1 and pin 2 are connected

² I_{pp} according to IEC61000-4-5, only valid if pin 1 and pin 2 are connected

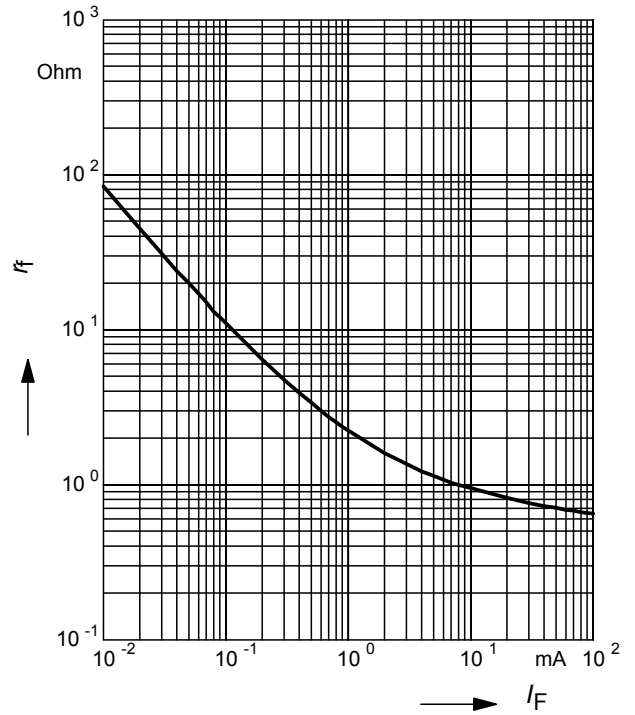
Diode capacitance $C_T = f(V_R)$

$f =$ Parameter



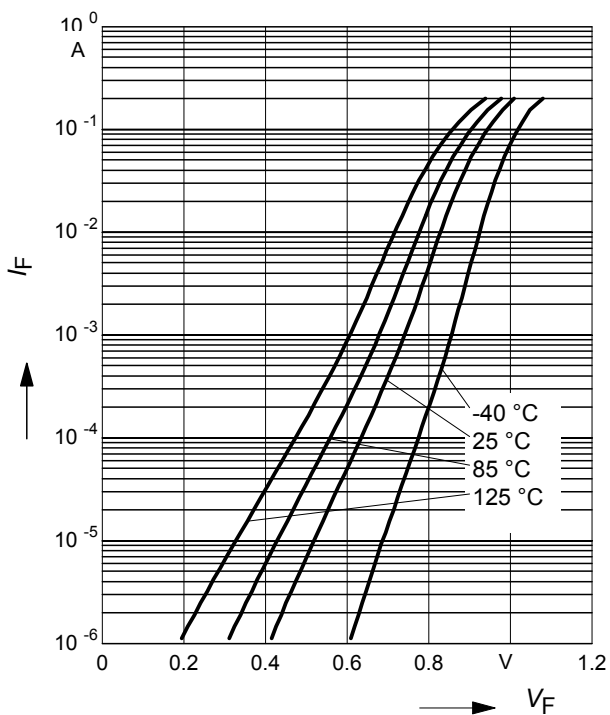
Forward resistance $r_f = f(I_F)$

$f = 100\text{MHz}$



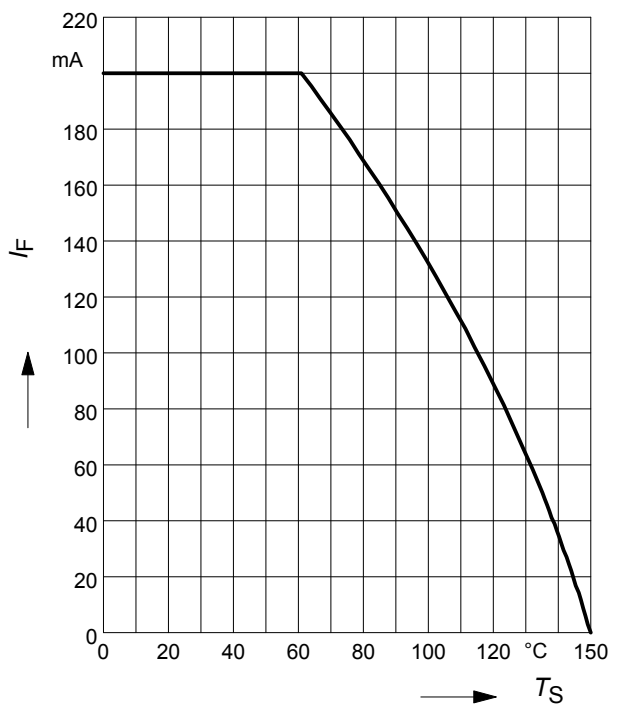
Forward current $I_F = f(V_F)$

$T_A =$ Parameter



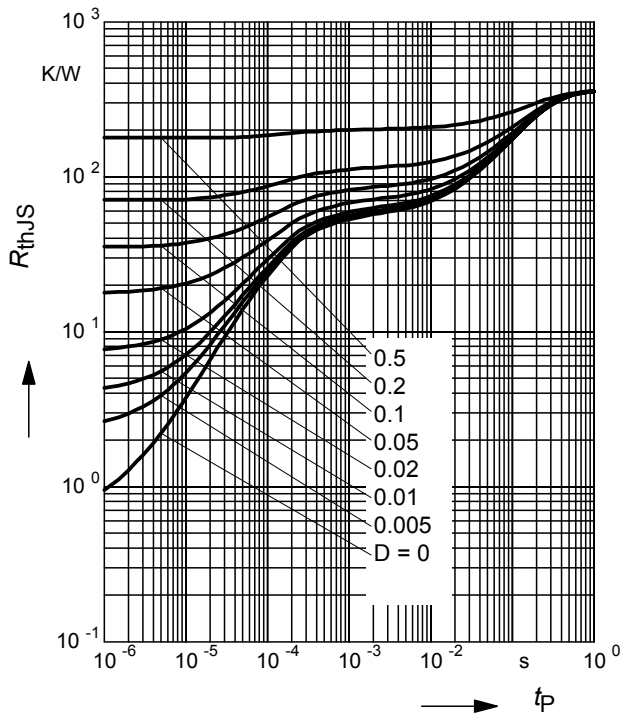
Forward current $I_F = f(T_S)$

BAR66



Permissible Puls Load $R_{thJS} = f(t_p)$

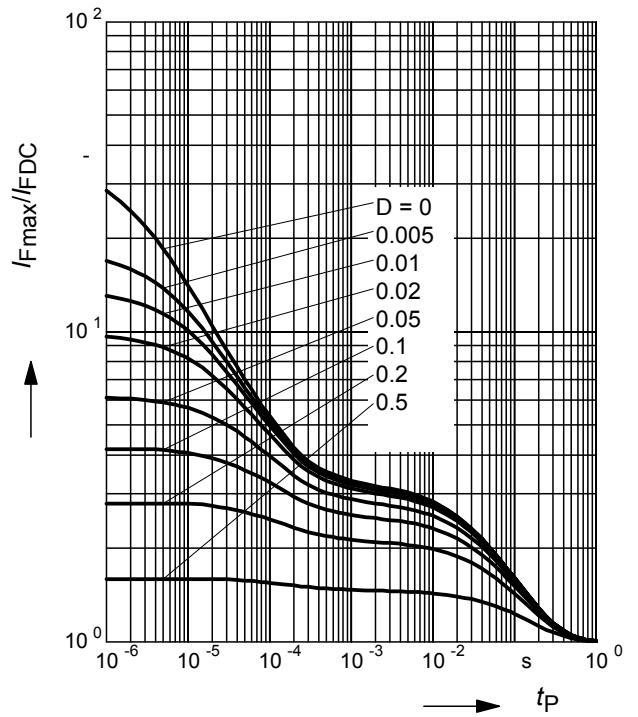
BAR66



Permissible Pulse Load

$I_{Fmax} / I_{FDC} = f(t_p)$

BAR66

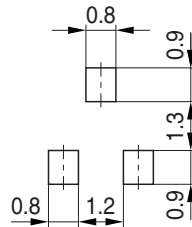


Package Outline



1) Lead width can be 0.6 max. in dambar area

Foot Print



Marking Layout (Example)



Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel



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