

# BSS123

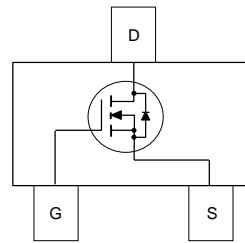
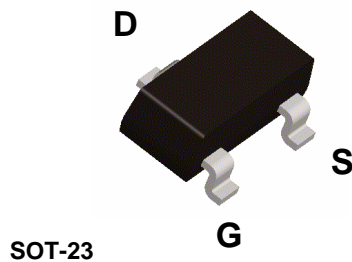
## N-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

### Features

- 0.17 A, 100 V.  $R_{DS(ON)} = 6\Omega @ V_{GS} = 10 V$   
 $R_{DS(ON)} = 10\Omega @ V_{GS} = 4.5 V$
- High density cell design for extremely low  $R_{DS(ON)}$
- Rugged and Reliable
- Compact industry standard SOT-23 surface mount package



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	100	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current – Continuous (Note 1)	0.17	A
	– Pulsed	0.68	
P <sub>D</sub>	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.8	mW/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1)	350	°C/W
------------------	--	-----	------

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
SA	BSS123	7"	8mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

**Off Characteristics**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		97		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			60	$\mu\text{A}$
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			10	nA
$I_{GSS}$	Gate–Body Leakage.	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 50$	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	0.8	1.7	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 1\text{ mA}$ , Referenced to $25^\circ\text{C}$		-2.7		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 0.17\text{ A}$		1.2	6	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 0.17\text{ A}$		1.3	10	
		$V_{GS} = 10\text{ V}, I_D = 0.17\text{ A}, T_J = 125^\circ\text{C}$		2.2	12	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	0.68			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 0.17\text{ A}$	0.08	0.8		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		73		pF
$C_{oss}$	Output Capacitance			7		pF
$C_{riss}$	Reverse Transfer Capacitance			3.4		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		2.2		$\Omega$

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 30\text{ V}, I_D = 0.28\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		1.7	3.4	ns
$t_r$	Turn–On Rise Time			9	18	ns
$t_{d(off)}$	Turn–Off Delay Time			17	31	ns
$t_f$	Turn–Off Fall Time			2.4	5	ns
$Q_g$	Total Gate Charge	$V_{DS} = 30\text{ V}, I_D = 0.22\text{ A},$ $V_{GS} = 10\text{ V}$		1.8	2.5	nC
$Q_{gs}$	Gate–Source Charge			0.2		nC
$Q_{gd}$	Gate–Drain Charge			0.3		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain–Source Diode Forward Current			0.17		A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.34\text{ A}$ (Note 2)		0.8	1.3	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 0.17\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$		11		nS
$Q_{rr}$	Diode Reverse Recovery Charge			3		nC

**NOTE:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- $350^\circ\text{C}/\text{W}$  when mounted on a minimum pad..

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## Typical Characteristics

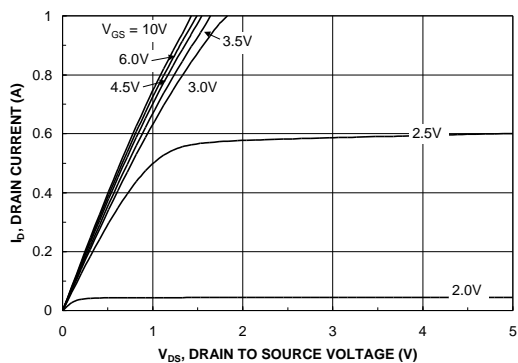


Figure 1. On-Region Characteristics.

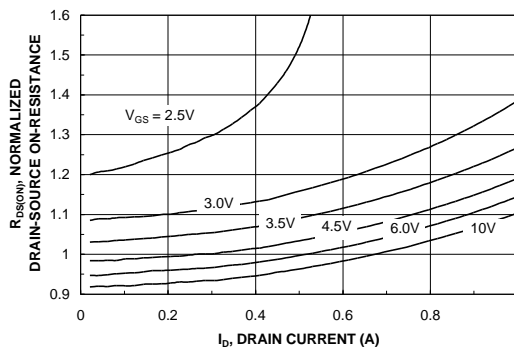


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

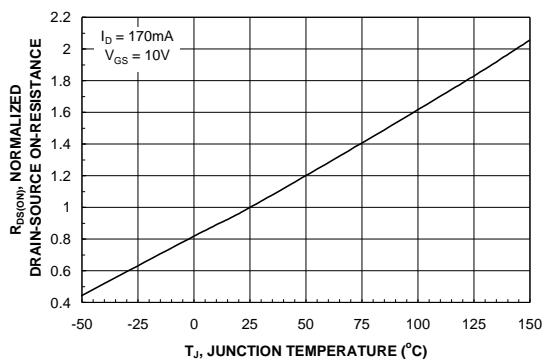


Figure 3. On-Resistance Variation with Temperature.

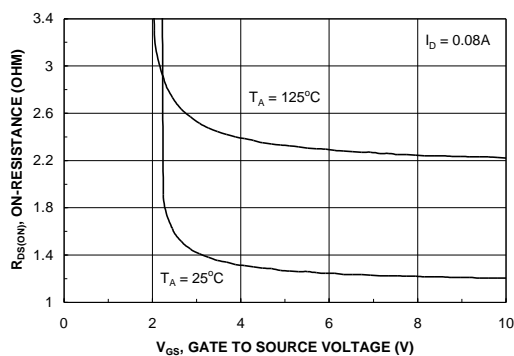


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

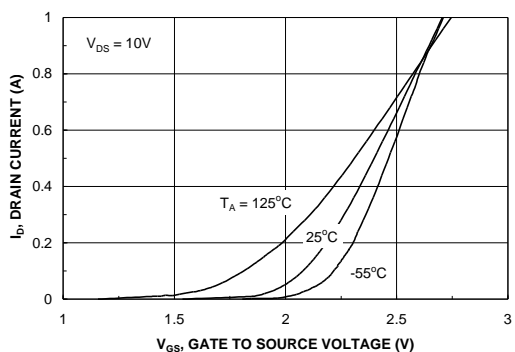


Figure 5. Transfer Characteristics.

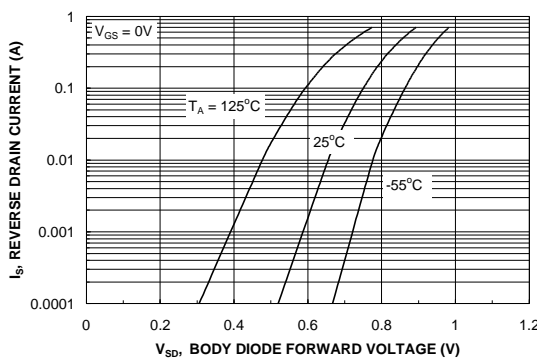


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics

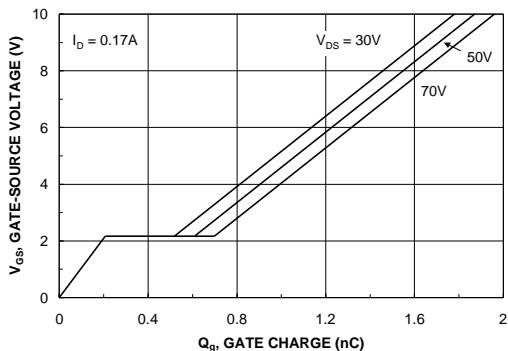


Figure 7. Gate Charge Characteristics.

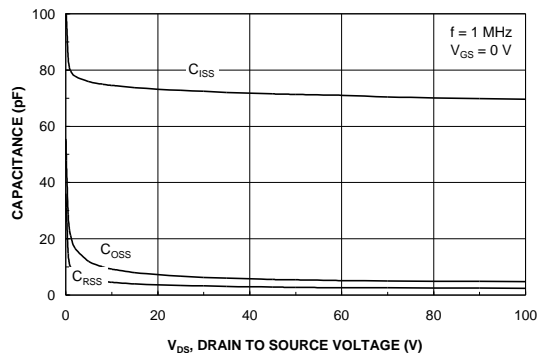


Figure 8. Capacitance Characteristics.

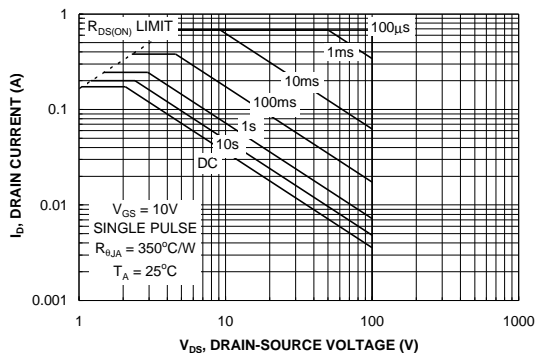


Figure 9. Maximum Safe Operating Area.

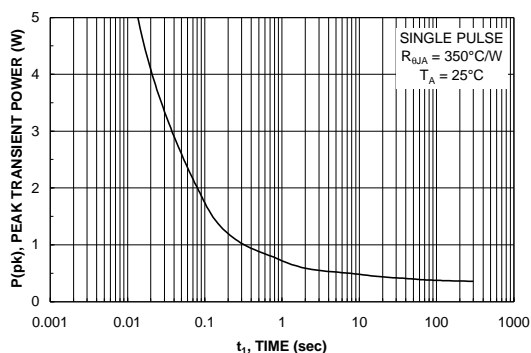


Figure 10. Single Pulse Maximum Power Dissipation.

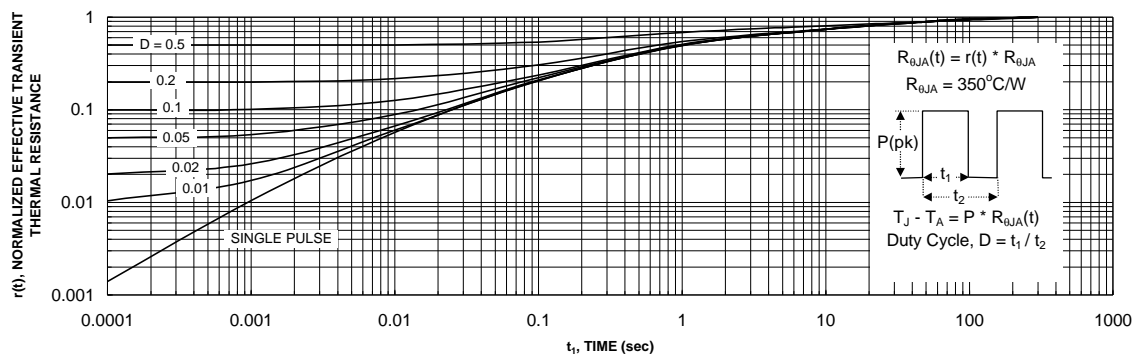


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1a. Transient thermal response will change depending on the circuit board design.

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT™	ImpliedDisconnect™	PACMAN™	SPM™
ActiveArray™	FACT Quiet Series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
E <sup>2</sup> CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I <sup>2</sup> C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

[www.s-manuals.com](http://www.s-manuals.com)