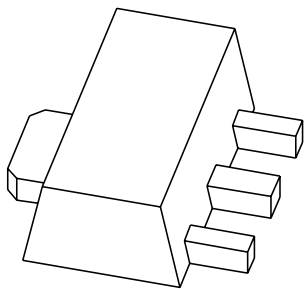


DATA SHEET



BSS87

**N-channel enhancement mode
vertical D-MOS transistor**

Product specification
Supersedes data of 1997 June 23

2001 May 18

N-channel enhancement mode vertical D-MOS transistor

BSS87

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low $R_{DS(on)}$.

APPLICATIONS

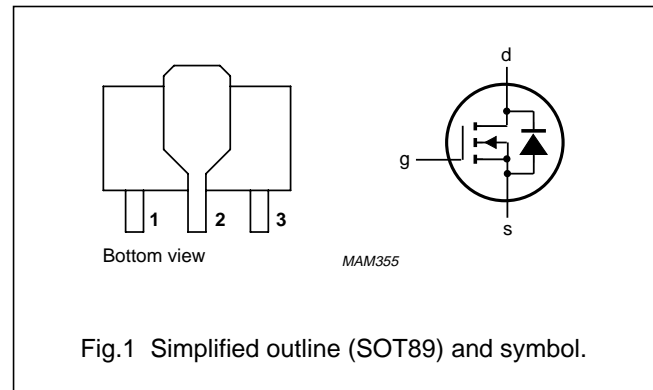
- Line current interruptor in telephone sets
- Applications in relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT89 package.

PINNING - SOT89

PIN	DESCRIPTION
1	source
2	drain
3	gate



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	± 20	V
I_D	drain current (DC)		–	–	400	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$	–	–	1	W
$R_{DS(on)}$	drain-source on-state resistance	$I_D = 400\text{ mA}; V_{GS} = 10\text{ V}$	–	1.6	3	Ω
$ y_{fs} $	forward transfer admittance	$I_D = 400\text{ mA}; V_{DS} = 25\text{ V}$	140	750	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
I_D	drain current (DC)		–	400	mA
I_{DM}	peak drain current		–	1.6	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}; \text{note 1}$	–	1	W
T_{stg}	storage temperature		–55	+150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum $10 \times 10\text{ mm}$

N-channel enhancement mode vertical D-MOS transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note

- Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10×10 mm

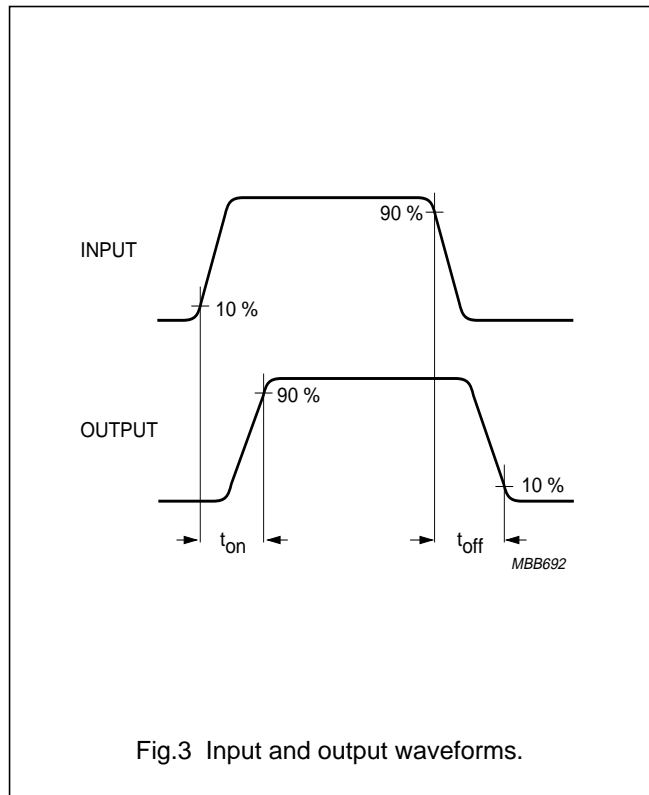
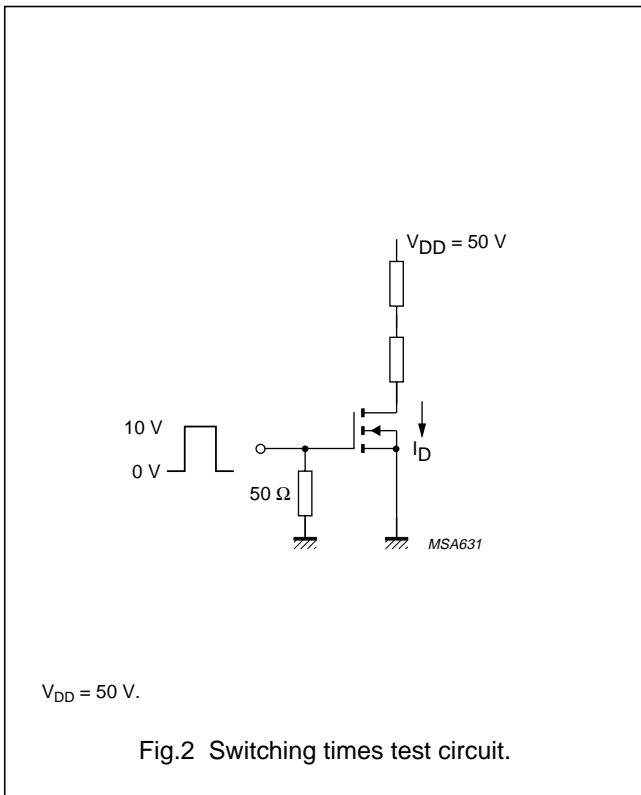
CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0$	200	–	–	V
I_{DSS}	drain-source leakage current	$V_{DS} = 60\ \text{V}; V_{GS} = 0$	–	–	200	nA
		$V_{DS} = 200\ \text{V}; V_{GS} = 0$	–	0.1	60	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	–	–	± 100	nA
V_{GSth}	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{GS} = V_{DS}$	0.8	–	2.8	V
R_{DSon}	drain-source on-state resistance	$I_D = 400\ \text{mA}; V_{GS} = 10\ \text{V}$	–	1.6	3	Ω
$ Y_{fs} $	transfer admittance	$I_D = 400\ \text{mA}; V_{DS} = 25\ \text{V}$	140	750	–	mS
C_{iss}	input capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0;$ $f = 1\ \text{MHz}$	–	100	120	pF
C_{oss}	output capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0;$ $f = 1\ \text{MHz}$	–	20	30	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0;$ $f = 1\ \text{MHz}$	–	10	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V};$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	6	10	ns
t_{off}	turn-off time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V};$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	49	60	ns

N-channel enhancement mode vertical D-MOS transistor

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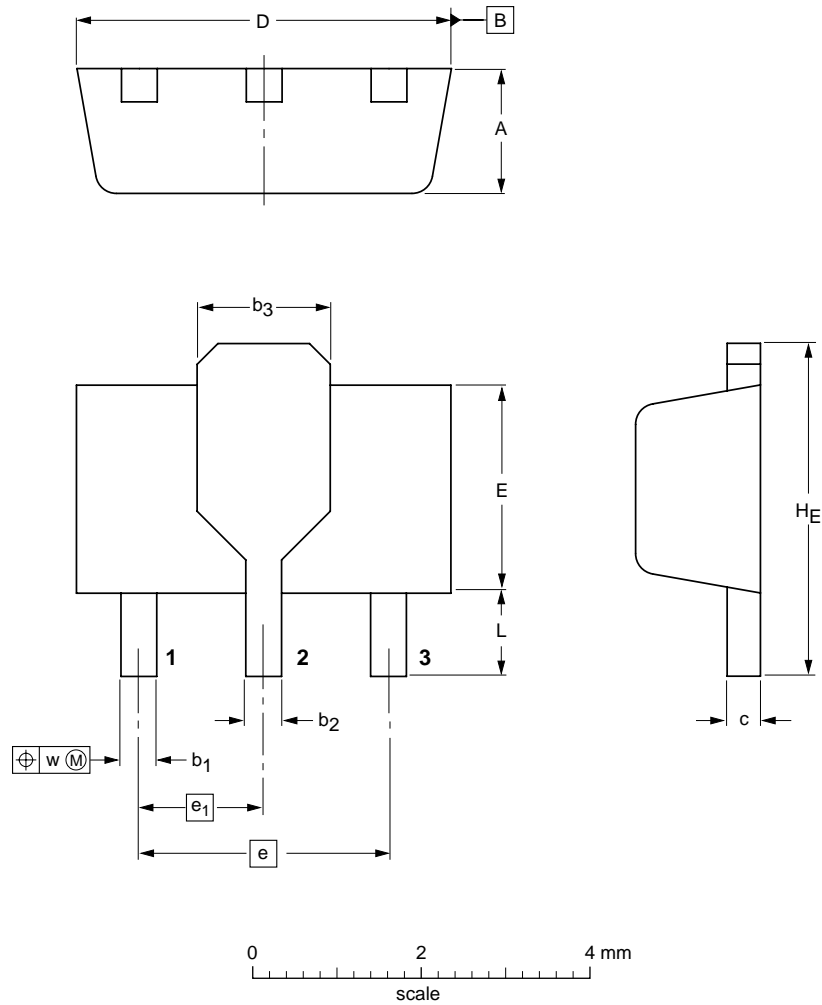
N-channel enhancement mode
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b ₁	b ₂	b ₃	c	D	E	e	e ₁	H _E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89		TO-243	SC-62			97-02-28 99-09-13

N-channel enhancement mode vertical D-MOS transistor

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DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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vertical D-MOS transistor

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Printed in The Netherlands

613510/03/pp8

Date of release: 2001 May 18

Document order number: 9397 750 08278

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