

DATA SHEET

BST84

N-channel enhancement mode
vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

N-channel enhancement mode vertical D-MOS transistor

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DESCRIPTION

N-channel vertical D-MOS transistor in SOT89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

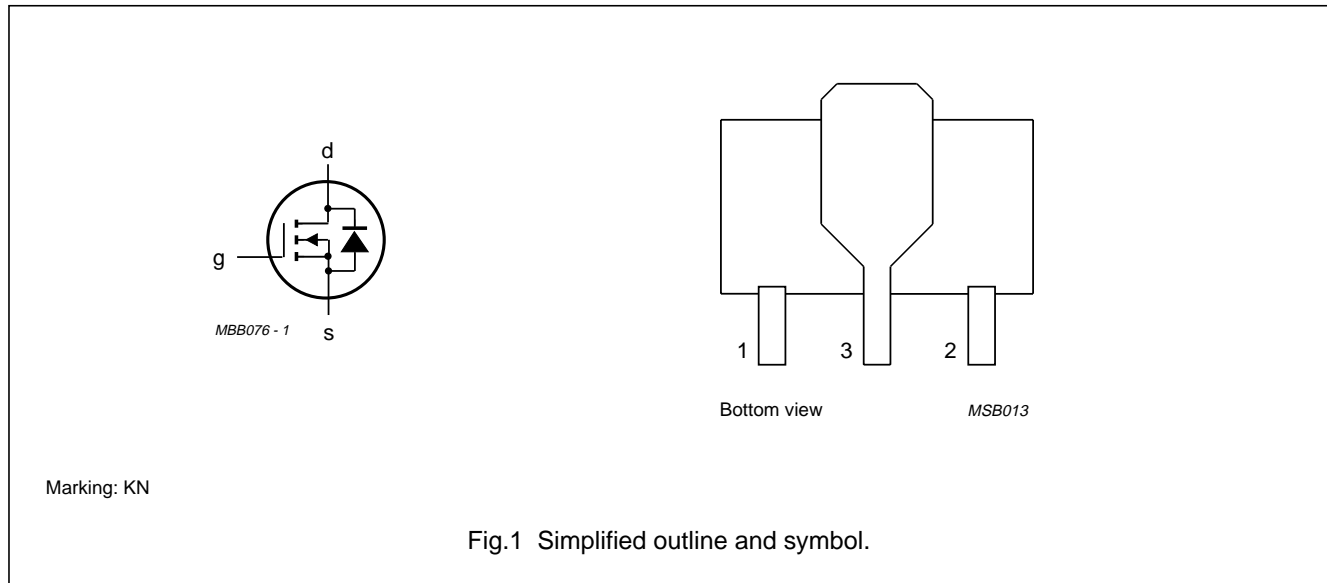
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GS0}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ.	6 Ω
		max.	12 Ω
Transfer admittance $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$	$ Y_{fs} $	typ.	250 mS

PINNING - SOT89

- 1 = source
- 2 = gate
- 3 = drain

PIN CONFIGURATION



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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to $T_{amb} = 25\text{ °C}$ (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		-65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125 K/W
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Note

1. Transistor mounted on a ceramic substrate with area of 2.5 cm² and thickness of 0.7 mm.

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CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Drain-source breakdown voltage

$$I_D = 100\ \mu\text{A}; V_{GS} = 0$$

$$V_{(BR)DSS} \quad \text{min.} \quad 200\ \text{V}$$

Drain-source leakage current

$$V_{DS} = 160\ \text{V}; V_{GS} = 0$$

$$I_{DSS} \quad \text{max.} \quad 10\ \mu\text{A}$$

Gate-source leakage current

$$V_{GS} = 20\ \text{V}; V_{DS} = 0$$

$$I_{GSS} \quad \text{max.} \quad 100\ \text{nA}$$

Gate threshold voltage

$$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$$

$$V_{GS(th)} \quad \text{min.} \quad 0.8\ \text{V}$$

$$\quad \quad \quad \text{max.} \quad 2.8\ \text{V}$$

Drain-source ON-resistance

$$I_D = 250\ \text{mA}; V_{GS} = 10\ \text{V}$$

$$R_{DS(on)} \quad \text{typ.} \quad 6\ \Omega$$

$$\quad \quad \quad \text{max.} \quad 12\ \Omega$$

Transfer admittance

$$I_D = 250\ \text{mA}; V_{DS} = 15\ \text{V}$$

$$|Y_{fs}| \quad \text{typ.} \quad 250\ \text{mS}$$

Input capacitance at $f = 1\ \text{MHz}$

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$$C_{iss} \quad \text{typ.} \quad 70\ \text{pF}$$

$$\quad \quad \quad \text{max.} \quad 90\ \text{pF}$$

Output capacitance at $f = 1\ \text{MHz}$

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$$C_{oss} \quad \text{typ.} \quad 20\ \text{pF}$$

$$\quad \quad \quad \text{max.} \quad 30\ \text{pF}$$

Feedback capacitance at $f = 1\ \text{MHz}$

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$$C_{rss} \quad \text{typ.} \quad 5\ \text{pF}$$

$$\quad \quad \quad \text{max.} \quad 10\ \text{pF}$$

Switching times (see Figs 2 and 3)

$$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V}; V_{GS} = 0\ \text{to}\ 10\ \text{V}$$

$$t_{on} \quad \text{typ.} \quad 4\ \text{ns}$$

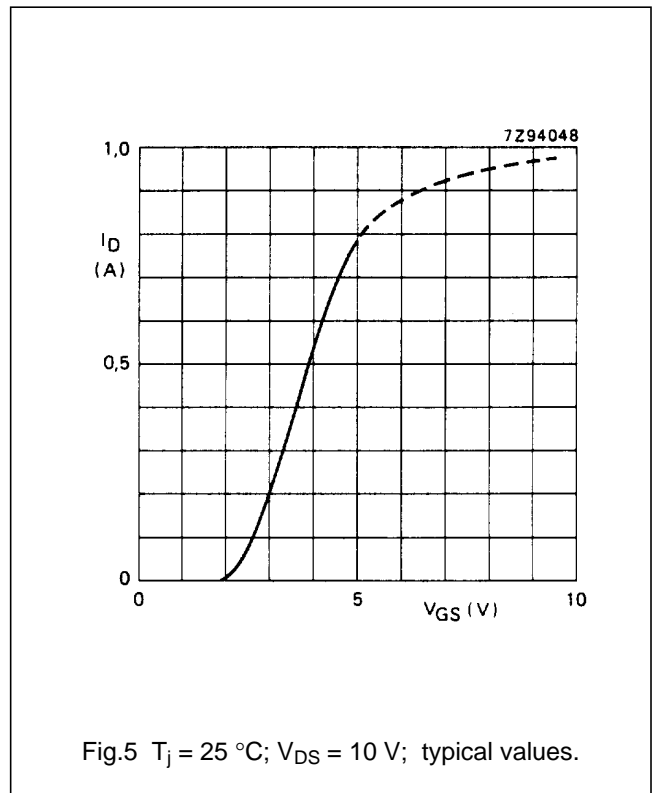
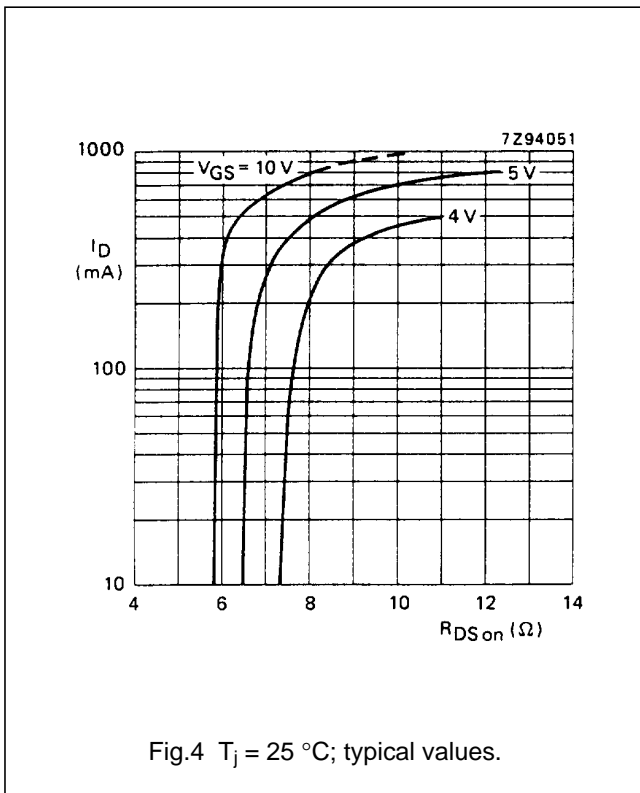
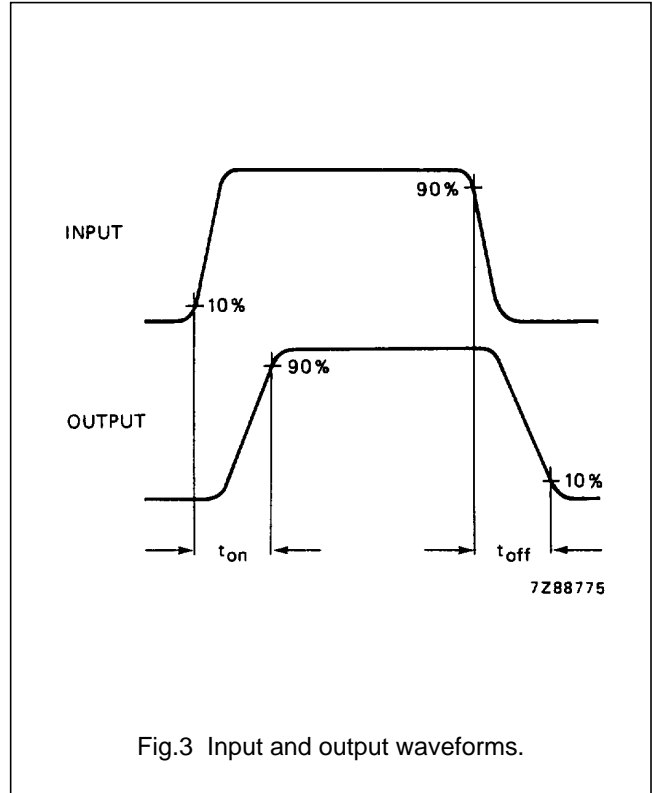
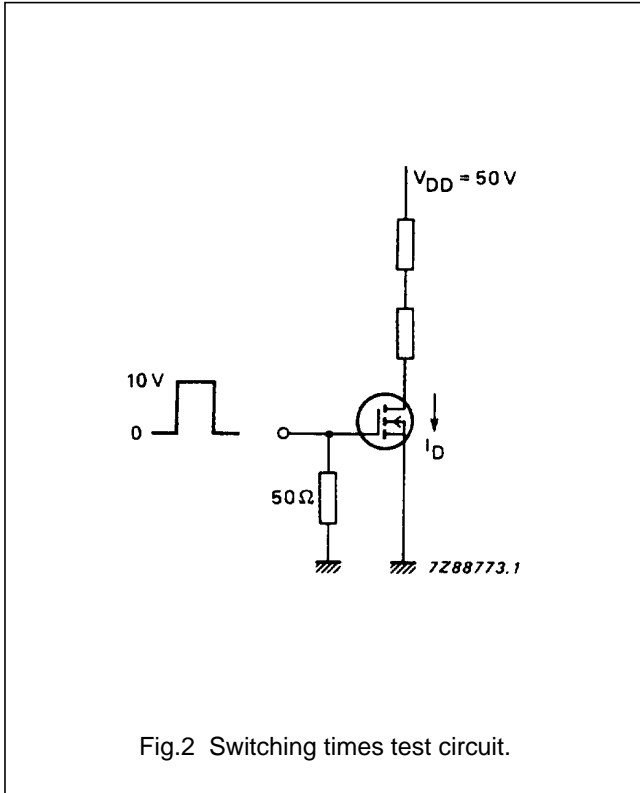
$$\quad \quad \quad \text{max.} \quad 10\ \text{ns}$$

$$t_{off} \quad \text{typ.} \quad 15\ \text{ns}$$

$$\quad \quad \quad \text{max.} \quad 25\ \text{ns}$$

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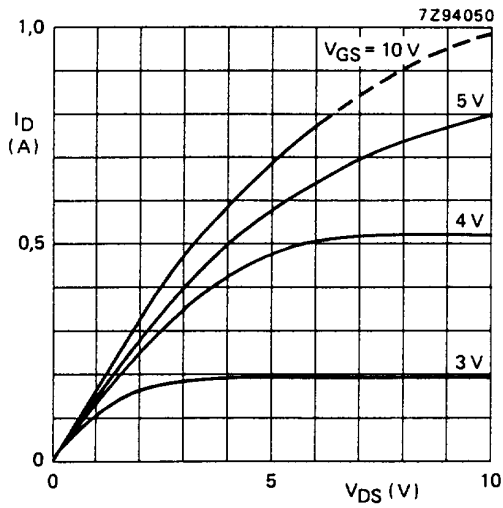


Fig.6 $T_j = 25^\circ\text{C}$; typical values.

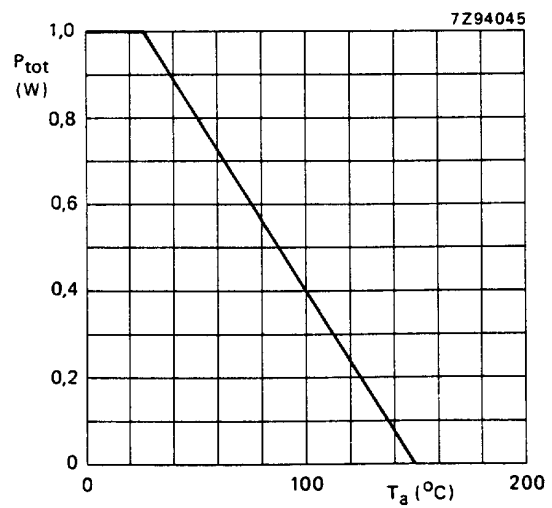


Fig.7 Power derating curve.

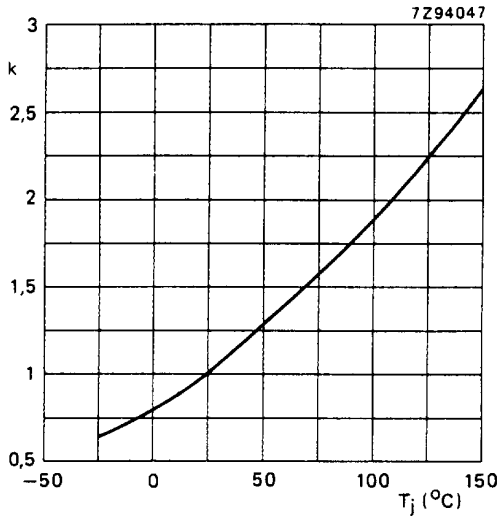


Fig.8

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25^\circ\text{C}}$$

at 400 mA/10 V; typical values.

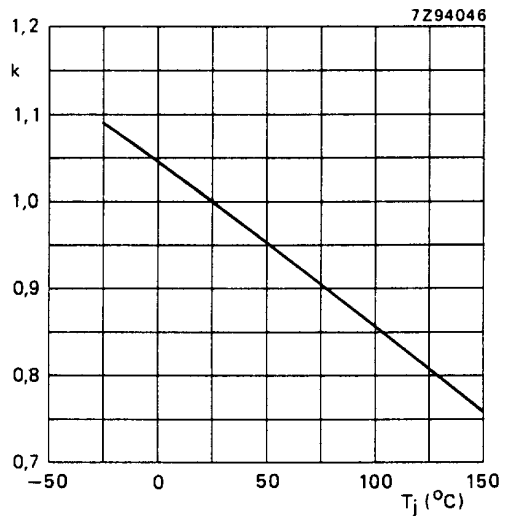


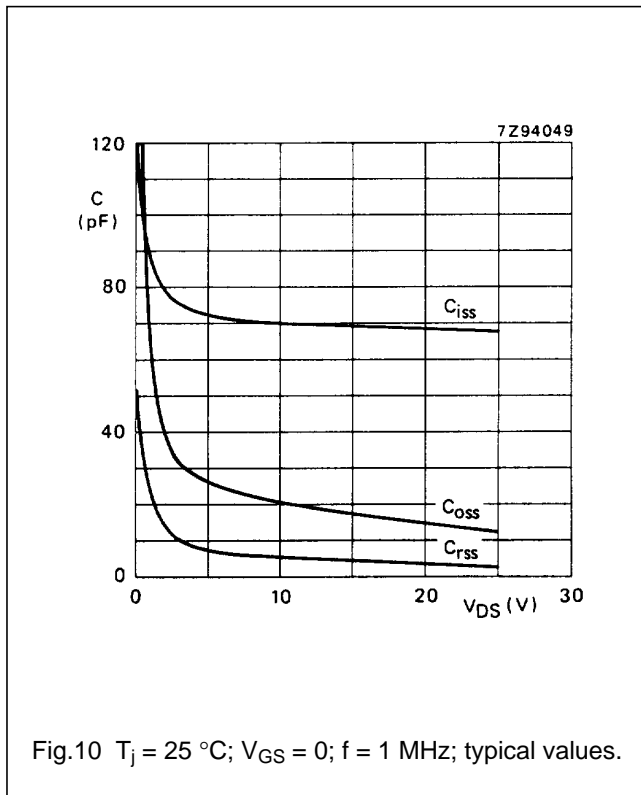
Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25^\circ\text{C}}$$

$V_{GS(th)}$ at 1 mA; typical values.

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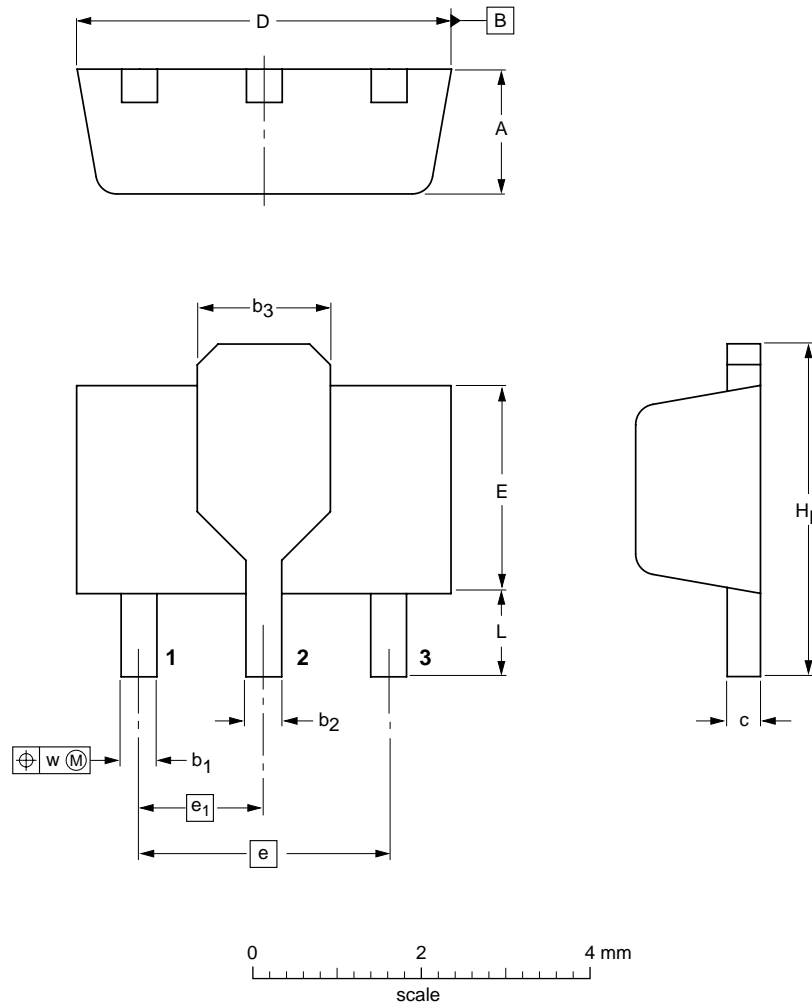
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PACKAGE OUTLINES

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b ₁	b ₂	b ₃	c	D	E	e	e ₁	H _E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

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BST84**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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