ON Semiconductor®

DAP006

PWM Current-Mode Controller for Free Running Quasi-Resonant Operation

The DAP006 combines a true current mode modulator and a demagnetization detector to ensure full borderline/critical Conduction Mode in any load/line conditions and minimum drain voltage switching (Quasi−Resonant operation). Due to its inherent skip cycle capability, the controller enters burst mode as soon as the power demand falls below a predetermined level. As this happens at low peak current, no audible noise can be heard. An internal 5.0 μs timer prevents the free−run frequency to exceed the 150 kHz CISPR−22 EMI starting limit while the skip adjustment capability lets the user select the frequency at which the burst foldback takes place.

The Dynamic Self−Supply (DSS) drastically simplifies the transformer design in avoiding the use of an auxiliary winding. This feature is particularly useful in applications where the output voltage varies during operation (e.g. battery chargers). Due to its high−voltage technology, the IC is directly connected to the high−voltage DC rail. The DSS also offers a better overload trip point.

The transformer core reset detection is done through an auxiliary winding which, brought via a dedicated pin, also enables fast Over−Voltage Protection (OVP). Once an OVP has been detected, the IC permanently latches−off.

Finally, the continuous feedback signal monitoring implemented with an over−current fault protection circuitry (OCP) makes the final design rugged and reliable.

Features

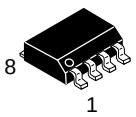
- Free−Running Borderline/Critical Mode Quasi−Resonant Operation
- Current−Mode with Adjustable Skip−Cycle Capability
- No Auxiliary Winding V_{CC} Operation
- Auto−Recovery Over Current Protection
- Latching Over Voltage Protection
- External Latch Triggering, e.g. Via Over−Temperature Signal
- 500 mA Peak Current Source/Sink Capability
- Internal 4.0 ms Soft−Start
- Internal 5.0 μs Minimum T_{OFF}
- Adjustable Skip Level
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient Analysis

Typical Applications

- AC/DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Consumer Electronics (DVD Players, Set−Top Boxes, TVs, etc.)
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

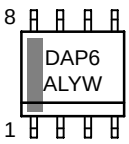
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

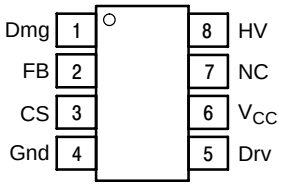


SO−8
D1, D2 SUFFIX
CASE 751

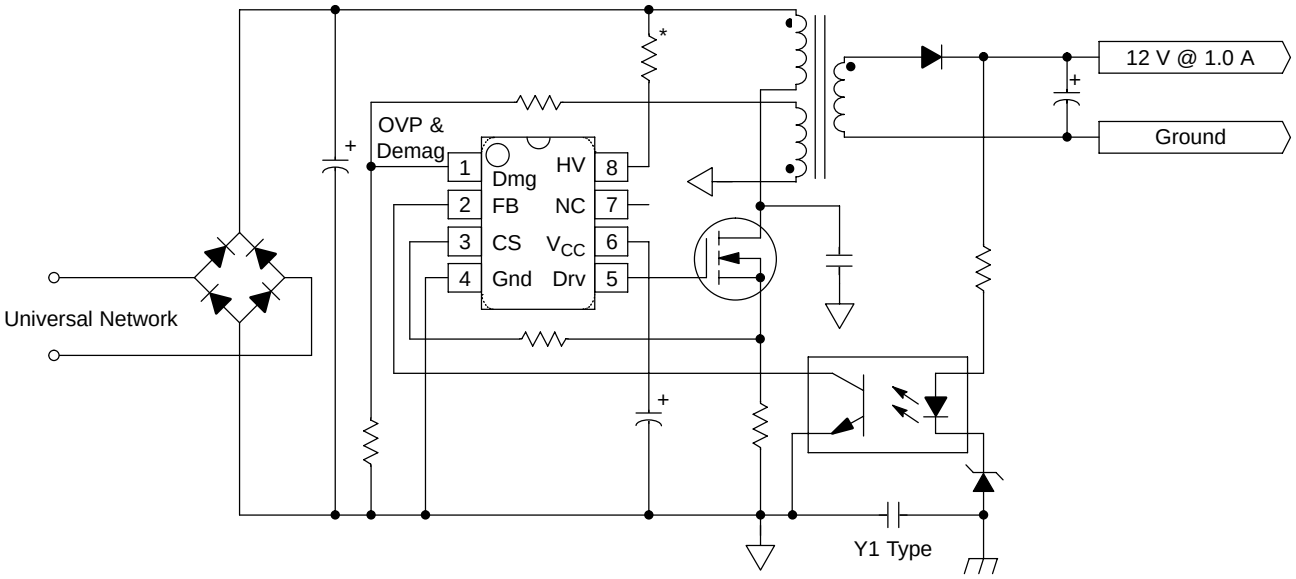
MARKING DIAGRAM



PIN CONNECTIONS



(Top View)



*Please refer to the application information section

Figure 1. Typical Application

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	Demag	Core reset detection and OVP	The auxiliary FLYBACK signal ensures discontinuous operation and offers a fixed overvoltage detection level of 7.2 V.
2	FB	Sets the peak current setpoint	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand. By bringing this pin below the internal skip level, device shuts off.
3	CS	Current sense input and skip cycle level selection	This pin senses the primary current and routes it to the internal comparator via an L.E.B. By inserting a resistor in series with the pin, you control the level at which the skip operation takes place.
4	Gnd	The IC ground	−
5	Drv	Driving pulses	The driver's output to an external MOSFET.
6	V_{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 10 μF.
7	NC	−	This unconnected pin ensures adequate creepage distance.
8	HV	High−voltage pin	Connected to the high−voltage rail, this pin injects a constant current into the V_{CC} bulk capacitor.

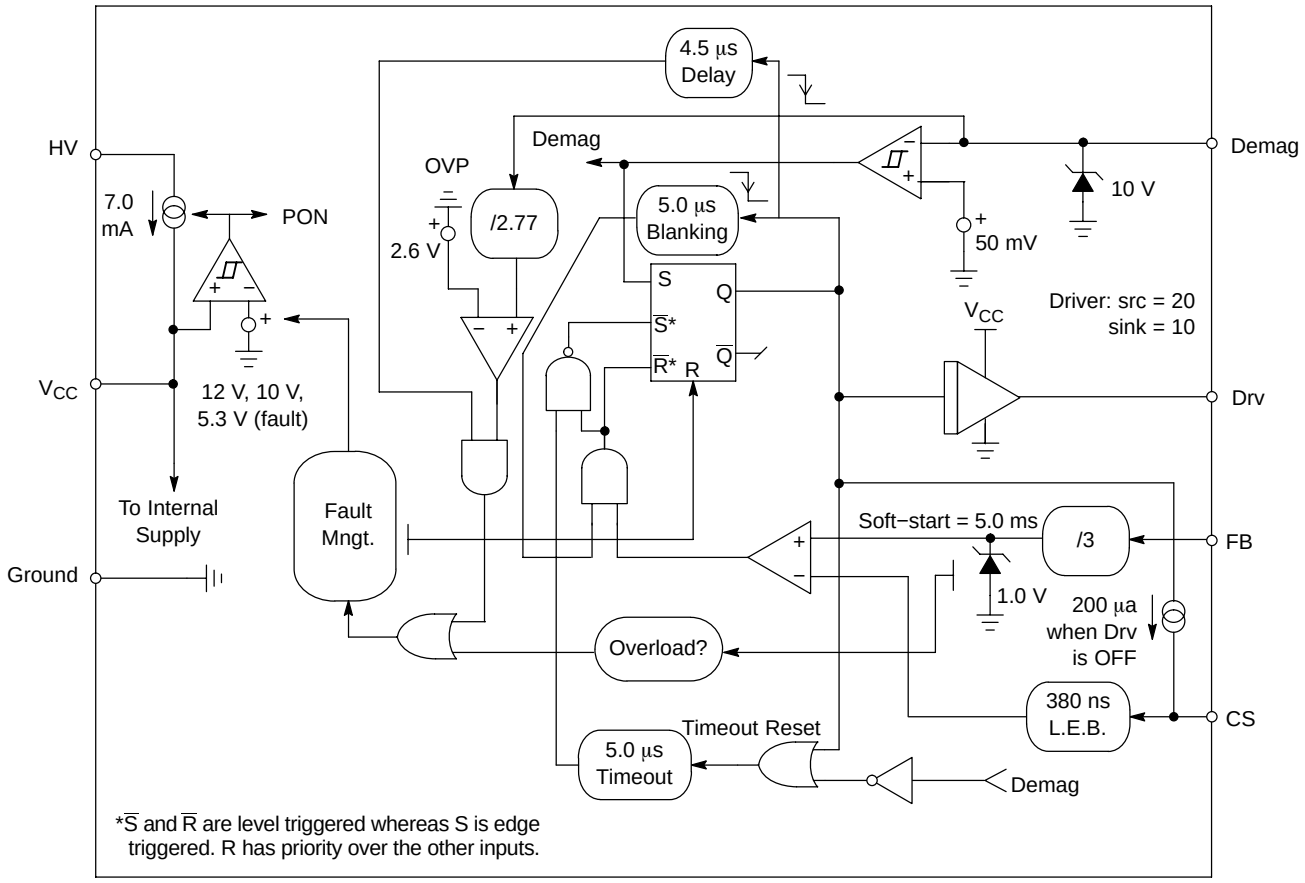


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Units
Continuous Power Supply or Drive Voltage	V_{CC}, Drv	18	V
Transient Power Supply Voltage Duration < 10 ms, I_{VCC} < 10 mA	V_{CC}	20	V
Maximum Voltage on all other pins except Pin 8 (HV), Pin 6 (V_{CC}) and Pin 5 (Drv)	−	−0.3 to 10	V
Maximum Current into all pins except V_{CC} (6), HV (8) and Demag (1) when 10 V ESD diodes are activated	−	5.0	mA
Maximum Current in Pin 1	Idem	+3.0/−2.0	mA
Thermal Resistance, Junction−to−Case	$R_{\theta J-C}$	57	°C/W
Thermal Resistance, Junction−to−Air, SOIC version	$R_{\theta J-A}$	178	°C/W
Maximum Junction Temperature	TJ_{MAX}	150	°C
Temperature Shutdown	−	155	°C
Hysteresis in Shutdown	−	30	°C
Storage Temperature Range	−	−60 to +150	°C
ESD Capability, HBM Model (All pins except V_{CC} and HV)	−	2.0	kV
ESD Capability, Machine Model	−	200	V
Maximum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) decoupled to ground with 10 μF	V_{HVMAX}	450	V
Minimum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) decoupled to ground with 10 μF	V_{HVMIN}	40	V

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, Max T_J = 150°C, V_{CC} = 11 V unless otherwise noted)

Rating	Pin	Symbol	Min	Typ	Max	Unit
DYNAMIC SELF−SUPPLY						
Vcc Increasing Level at which the Current Source Turns−off	6	VCC_{OFF}	10.8	12	12.9	V
Vcc Decreasing Level at which the Current Source Turns−on	6	VCC_{ON}	9.1	10	10.6	V
Vcc Decreasing Level at which the Latch−off Phase Ends	6	VCC_{latch}	−	5.3	−	V
Internal IC Consumption, No Output Load on Pin 5, F_{SW} = 60 kHz, Duty Cycle = TBD	6	ICC1	−	1.0	1.3 (Note 1)	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 60 kHz, Duty Cycle = TBD	6	ICC2	−	1.6	2.0 (Note 1	mA
Internal IC Consumption in Latch−off Phase	6	ICC3	−	330	−	μA
INTERNAL START−UP CURRENT SOURCE (T_J > 0°C)						
High−voltage Current Source, V_{CC} = 10 V	8	IC1	4.3	7.0	9.6	mA
High−voltage Current Source, V_{CC} = 0	8	IC2	−	8.0	−	mA
DRIVE OUTPUT						
Output Voltage Rise−time @ CL = 1.0 nF, 10−90% of Output Signal	5	T_r	−	40	−	ns
Output Voltage Fall−time @ CL = 1.0 nF, 10−90% of Output Signal	5	T_f	−	20	−	ns
Source Resistance	5	R_{OH}	12	20	36	Ω
Sink Resistance	5	R_{OL}	5.0	10	19	Ω
CURRENT COMPARATOR (Pin 5 Unloaded)						
Input Bias Current @ 1.0 V Input Level on Pin 3	3	I_{IB}	−	0.02	−	μA
Maximum Internal Current Setpoint	3	I_{Limit}	0.92	1.0	1.12	V
Propagation Delay from Current Detection to Gate OFF State	3	T_{DEL}	−	100	160	ns
Leading Edge Blanking Duration	3	T_{LEB}	−	380	−	ns
Internal Current Offset Injected on the CS Pin during OFF Time	3	Iskip	−	200	−	μA
OVERVOLTAGE SECTION (V_{CC} = 11 V)						
Sampling Delay after ON Time	1	T_{sample}	−	4.5	−	μs
OVP Internal Reference Level	1	V_{ref}	6.4	7.2	8.0	V
FEEDBACK SECTION (V_{CC} = 11 V, Pin 5 Loaded by 1.0 kΩ)						
Internal Pull−up Resistor	2	Rup	−	20	−	kΩ
Pin 3 to Current Setpoint Division Ratio	−	Iratio	−	3.3	−	−
Internal Soft−start	−	Tss	−	5.0	−	ms
DEMAGNETIZATION DETECTION BLOCK						
Input Threshold Voltage (Vpin 1 Decreasing)	1	V_{th}	35	50	90	mV
Hysteresis (Vpin 1 Decreasing)	1	V_H	−	20	−	mV
Input Clamp Voltage High State (Ipin 1 = 3.0 mA) Low State (Ipin 1 = −2.0 mA)	 1 1	 VC_H VC_L	 8.0 −0.9	 10 −0.7	 12 −0.5	 V V
Demag Propagation Delay	1	T_{dem}	−	210	−	ns
Internal Input Capacitance at Vpin 1 = 1.0 V	1	C_{par}	−	10	−	pF
Minimum T_{OFF} (Internal Blanking Delay after T_{ON})	1	T_{blank}	−	5.0	−	μs
Pin 1 Internal Resistance	1	R_{int}	−	28	−	kΩ

1. Max value at T_J = 0°C.

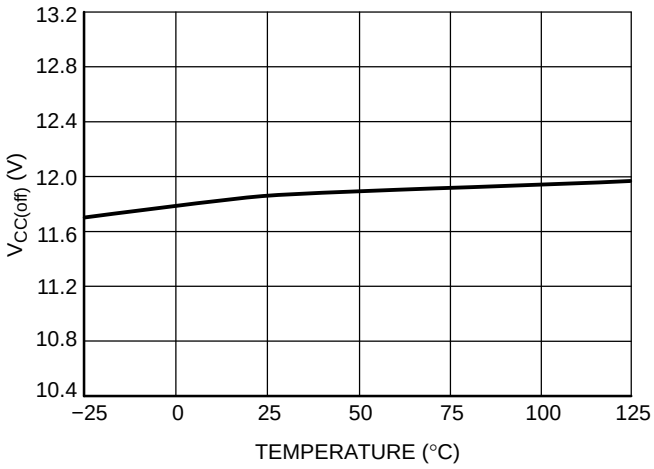


Figure 1. $V_{CC(off)}$ Threshold versus Temperature

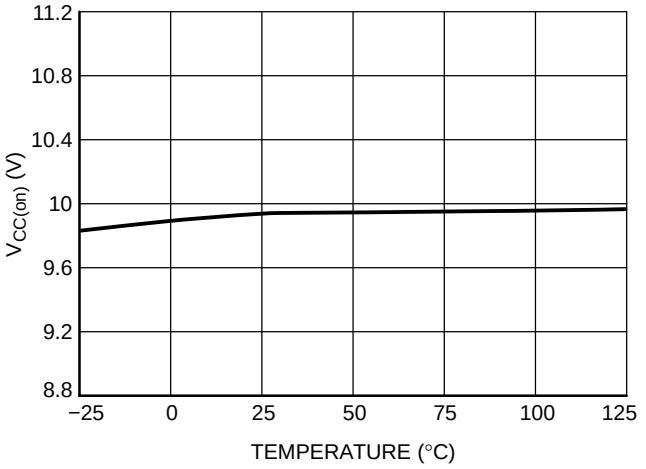


Figure 2. $V_{CC(on)}$ Threshold versus Temperature

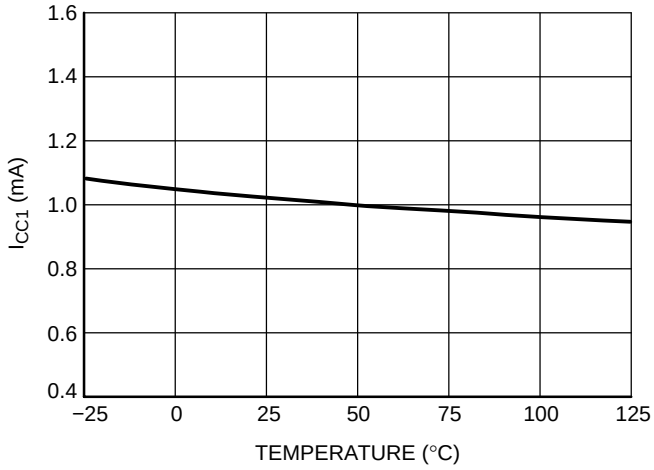


Figure 3. Current Consumption (No Load) versus Temperature

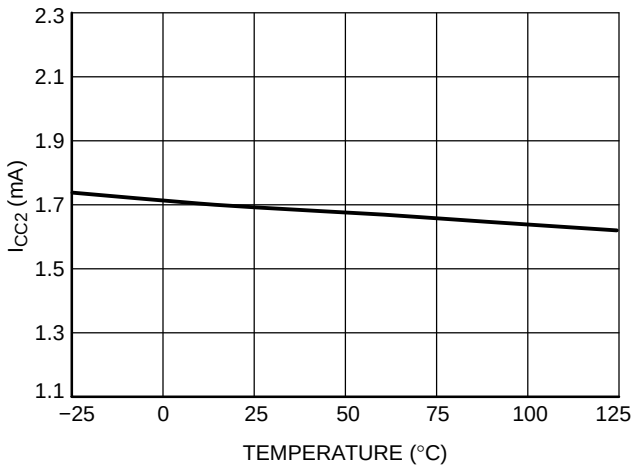


Figure 4. Current Consumption (Loaded by 1 nF) versus Temperature

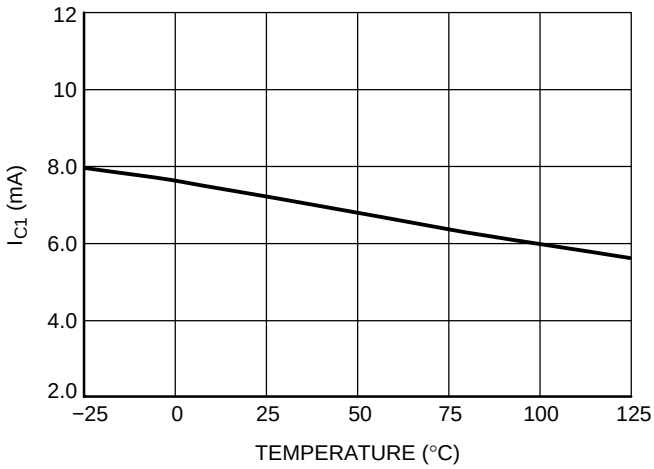


Figure 5. HV Current Source at V_{CC} = 10 V versus Temperature

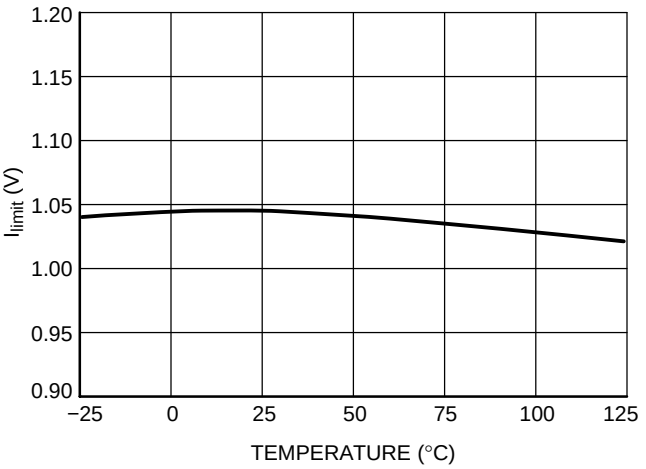


Figure 6. Maximum Current Setpoint versus Temperature

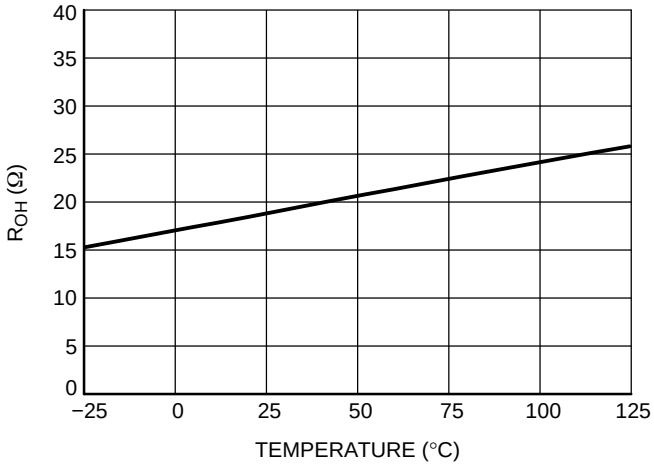


Figure 7. Drive Source Resistance versus Temperature

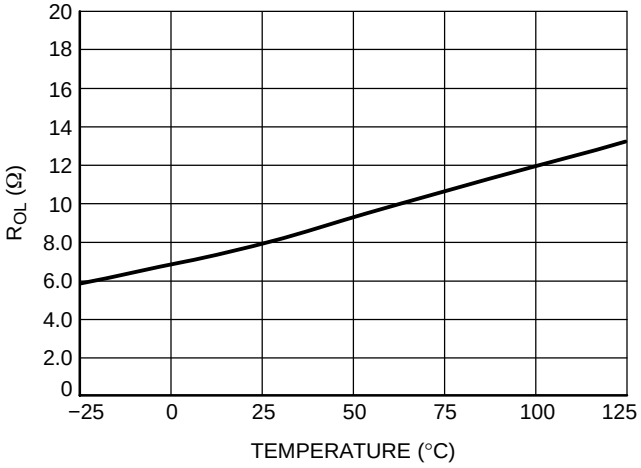


Figure 8. Drive Sink Resistance versus Temperature

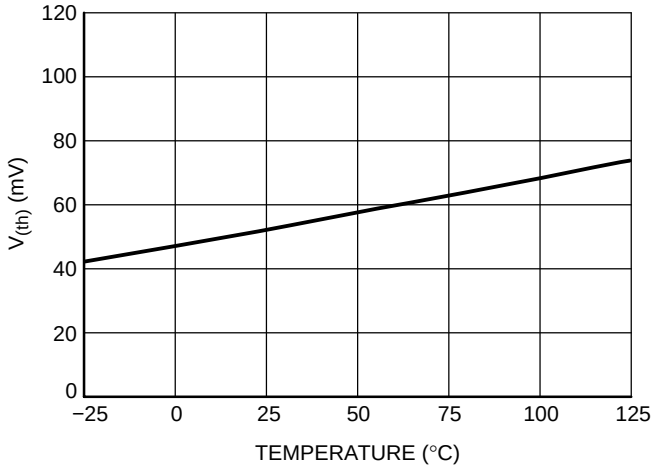


Figure 9. Demagnetization Detection Threshold versus Temperature

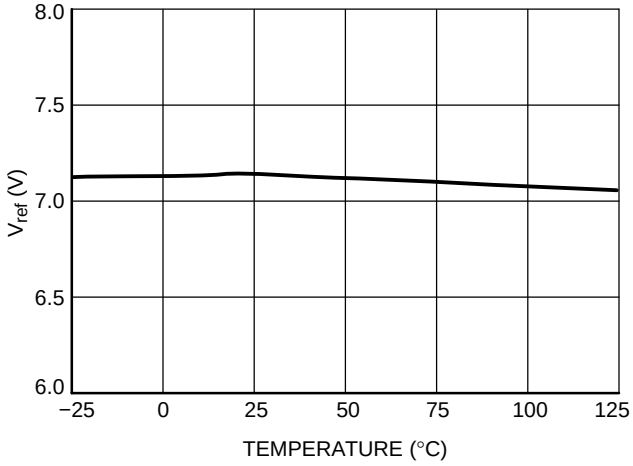


Figure 10. OVP Threshold versus Temperature

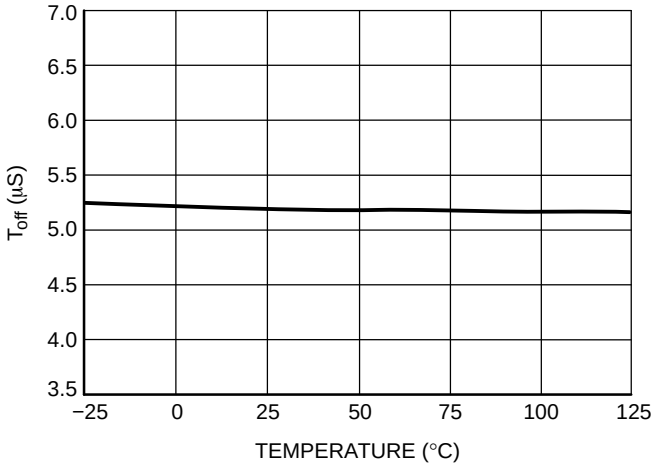


Figure 11. Minimum T_{off} versus Temperature

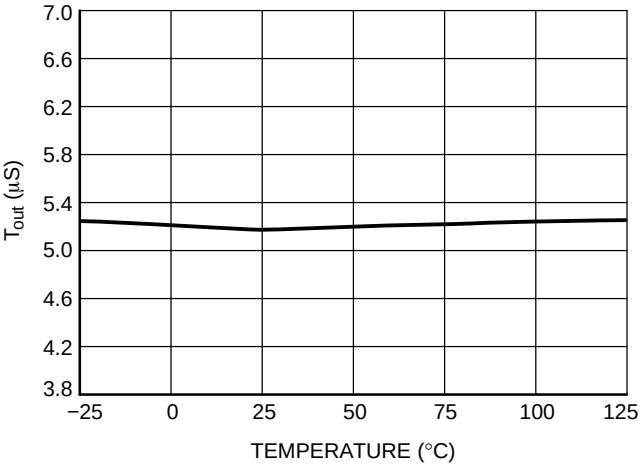


Figure 12. Demagnetization Detection Timeout versus Temperature

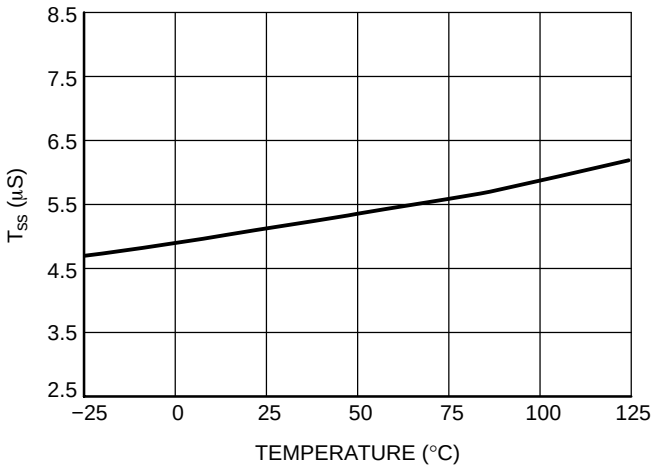


Figure 13. Internal Soft−start versus Temperature

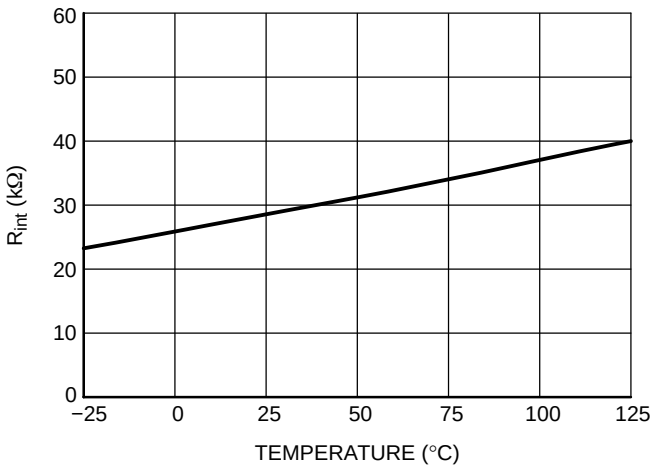


Figure 14. DMG Pin Internal Resistance versus Temperature

Application Information

Introduction

The DAP006 implements a standard current mode architecture where the switch−off time is dictated by the peak current setpoint whereas the core reset detection triggers the turn−on event. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC/DC adapters, consumer electronics, auxiliary supplies, etc. Thanks to its high−performance High−Voltage technology, the DAP006 incorporates all the necessary components / features needed to build a rugged and reliable Switch−Mode Power Supply (SMPS):

- *Transformer core reset detection:* borderline / critical operation is ensured whatever the operating conditions are. As a result, there are virtually no primary switch turn−on losses and no secondary diode recovery losses. The converter also stays a first−order system and accordingly eases the feedback loop design.
- *Quasi−resonant operation:* by delaying the turn−on event, it is possible to re−start the MOSFET in the minimum of the drain−source wave, ensuring reduced EMI / video noise perturbations. In nominal power conditions, the DAP006 operates in Borderline Conduction Mode (BCM) also called Critical Conduction Mode.
- *Dynamic Self−Supply (DSS):* due to its Very High Voltage Integrated Circuit (VHVIC) technology, ON Semiconductor's DAP006 allows for a direct pin connection to the high−voltage DC rail. A dynamic current source charges up a capacitor and thus provides a fully independent V_{CC} level to the DAP006. As a result, there is no need for an auxiliary winding whose management is always a problem in variable output voltage designs (e.g. battery chargers).
- *Overvoltage Protection (OVP):* by sampling the plateau voltage on the demagnetization winding, the DAP006 goes into latched fault condition whenever an over−voltage condition is detected. The controller stays fully latched in this position until the V_{CC} is cycled down 4.0 V, e.g. when the user un−plugs the power supply from the mains outlet and re−plugs it.
- *External latch trip point:* by externally forcing a level on the OVP greater than the internal setpoint, it is possible to latch−off the IC, e.g. with a signal coming from a temperature sensor.
- *Adjustable skip cycle level:* by offering the ability to tailor the level at which the skip cycle takes place, the designer can make sure that the skip operation only occurs at low peak current. This point guarantees a noise−free operation with cheap transformer. This option also offers the ability to fix the maximum switching frequency when entering light load conditions.
- *Over Current Protection (OCP):* by continuously monitoring the FB line activity, DAP006 enters burst mode as soon as the power supply undergoes an overload. The device enters a safe low power operation which prevents from any lethal thermal runaway. As soon as the default disappears, the power supply resumes operation. Unlike other controllers, overload detection is performed independently of any auxiliary winding level. In presence of a bad coupling between both power and auxiliary windings, the short circuit detection can be severely affected. The DSS naturally shields you against these troubles.

Dynamic Self−Supply

The DSS principle is based on the charge/discharge of the V_{CC} bulk capacitor from a low level up to a higher level. We can easily describe the current source operation with some simple logical equations:

POWER−ON: IF $V_{CC} < V_{CCH}$ THEN Current Source is ON, no output pulses

IF V_{CC} decreasing > V_{CCL} THEN Current Source is OFF, output is pulsing

IF V_{CC} increasing < V_{CCH} THEN Current Source is ON, output is pulsing

Typical values are: V_{CCH} = 12 V, V_{CCL} = 10 V

To better understand the operational principle, Figure 15's sketch offers the necessary light.

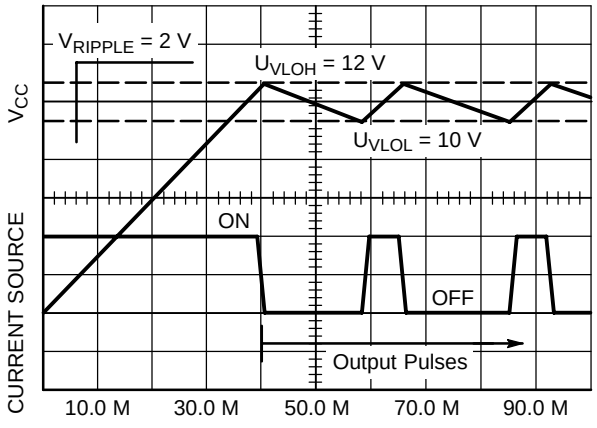


Figure 15. The Charge/Discharge Cycle Over a 10 μF V_{CC} Capacitor

The DSS behavior actually depends on the internal IC consumption and the MOSFET's gate charge Qg. If we select a MOSFET like the MTP2N60E, Qg equals 22 nC (max). With a maximum switching frequency selected at 75 kHz, the average power necessary to drive the MOSFET (excluding the driver efficiency and neglecting various voltage drops) is:

$Fsw \cdot Qg \cdot V_{CC}$ with:

Fsw = maximum switching frequency

Qg = MOSFET's gate charge

$V_{CC} = V_{GS}$ level applied to the gate

To obtain the output current, simply divide this result by V_{CC}: $I_{driver} = F_{SW} \cdot Qg = 1.6$ mA. The total standby power consumption at no−load will therefore heavily rely on the internal IC consumption plus the above driving current (altered by the driver's efficiency). Suppose that the IC is supplied from a 350 VDC line. The current flowing through pin 8 is a direct image of the DAP006 consumption (neglecting the switching losses of the HV current source). If I_{CC2} equals 2.3 mA @ T_J = 60°C, then the power dissipated (lost) by the IC is simply: 350 x 2.3 m = 805 mW. For design and reliability reasons, it would be interested to reduce this source of wasted power which increase the die temperature. This can be achieved by using different methods:

1. Use a MOSFET with lower gate charge Qg.
2. Connect pin through a diode (1N4007 typically) to one of the mains input. The average value on pin 8 becomes $\frac{V_{mainsPEAK} \cdot 2}{\pi}$. Our power contribution example drops to: 223 x 1.8 m = 512 mW. If a resistor is installed between the mains and the diode, you further force the dissipation to migrate from the package to the resistor. The resistor value should account for low−line startups.

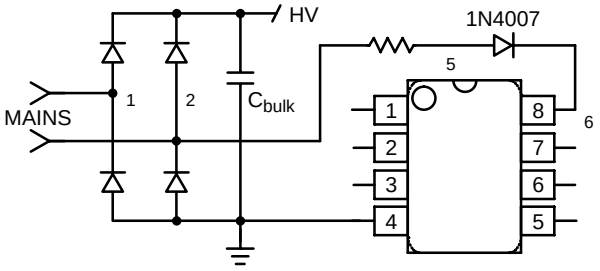


Figure 16. A simple diode naturally reduces the average voltage on pin 8

When using Figure 16 option, it is important to check the absence of any negative ringing that could occur on pin 8. The resistor in series should help to damp any parasitic LC network that would ring when suddenly applying the power to the IC. Also, since the power disappears during 20 ms (half−wave rectification), CV_{CC} should be calculated to supply the IC during these holes in the supply

3. Permanently force the V_{CC} level above V_{CCH} with an auxiliary winding. It will automatically disconnect the internal start−up source and the IC will be fully self−supplied from this winding. Again, the total power drawn from the mains will significantly decrease. Make sure the auxiliary voltage never exceeds the 16 V limit.

Skipping Cycle Mode

The DAP006 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so−called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 17) and follows the following formula:

$\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw \cdot D_{burst}$ with:

Lp = primary inductance

Fsw = switching frequency within the burst

Ip = peak current at which skip cycle occurs

D_{burst} = burst width / burst recurrence

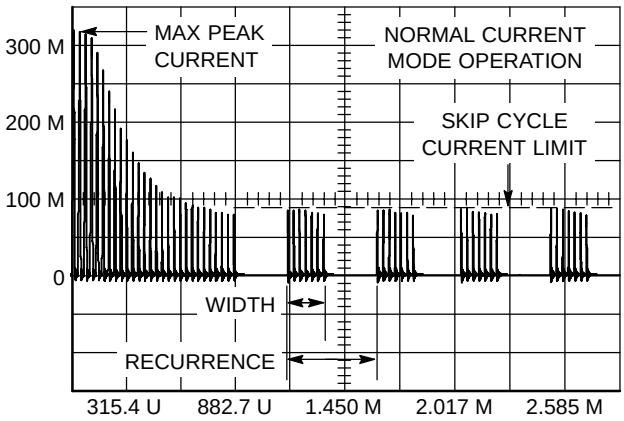


Figure 17. The skip cycle takes place at low peak currents which guaranties noise free operation

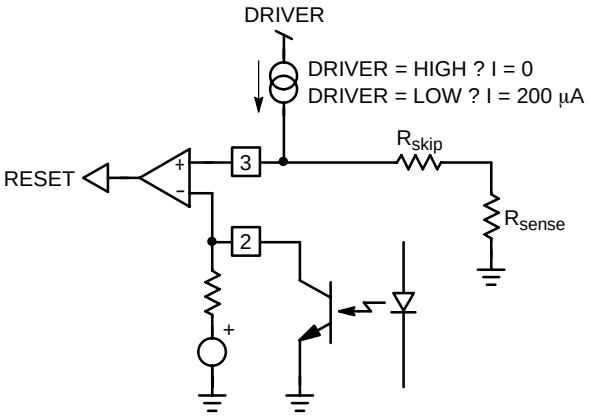


Figure 18. A patented method allows for skip level selection via a series resistor inserted in series with the current

The skip level selection is done through a simple resistor inserted between the current sense input and the sense element. Every time the DAP006 output driver goes low, a 200 μA source forces a current to flow through the sense pin (Figure 18): when the driver is high, the current source if off and the current sense information is normally processed. As soon as the driver goes low, the current source delivers 200 μA and develops a ground referenced voltage across R_{skip}. If this voltage is below the feedback voltage, the current sense comparator stays in the low state and the internal latch can be triggered by the next clock cycle. Now, if because of a low load mode the feedback voltage is below R_{skip} level, then the current sense comparator permanently resets the latch and the next clock cycle (given by the demagnetization detection) is ignored: we are skipping cycles as shown by Figure 17. As soon as the feedback voltage goes up again, there can be two situations: the recurrent period is small and a new demagnetization detection (next wave) signal triggers the DAP006. To the opposite, in low output power conditions, no more ringing waves are present on the drain and the toggling of the current sense comparator alone initiates a new cycle start. Figure 19 depicts these two different situations.

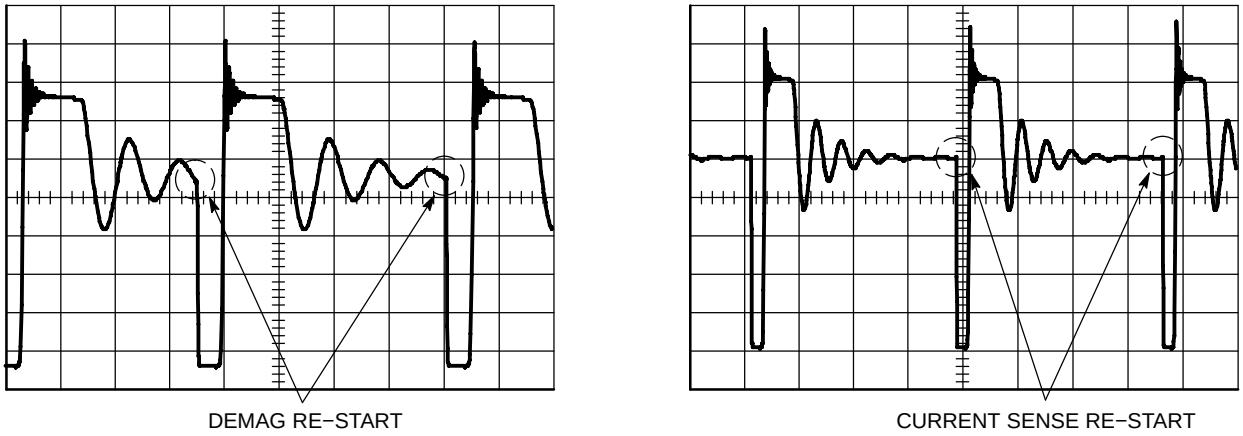


Figure 19. When the primary natural ringing becomes too low, the current sense initiates a new cycle when FB passes the skip level

Demagnetization Detection

The core reset detection is done by monitoring the voltage activity on the auxiliary winding. This voltage features a FLYBACK polarity. The typical detection level is fixed at 50 mV as exemplified by Figure 20.

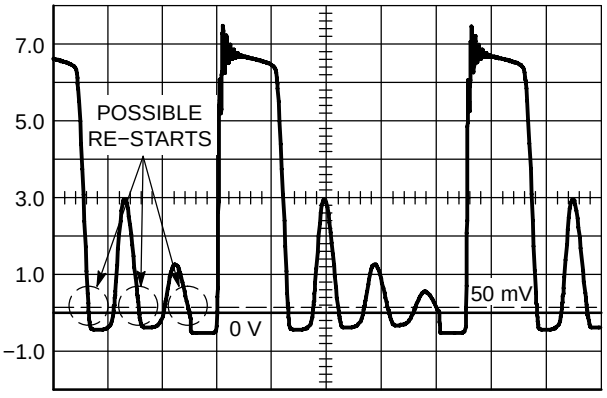


Figure 20. Core reset detection is done through a dedicated auxiliary winding monitoring

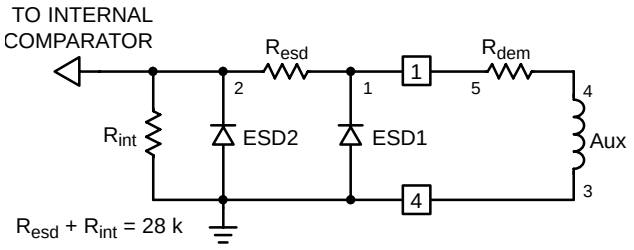


Figure 21. Internal Pad Implementation

An internal timer prevents any re−start within 5.0 μs further to the driver going−low transition. This prevents the switching frequency to exceed (1 / T_{ON} + 5.0 μs) but also avoid false leakage inductance tripping at turn−off. In some cases, the leakage inductance kick is so energetic, that a slight filtering is necessary.

The DAP006 demagnetization detection pad features a specific component arrangement as detailed by Figure 21. In this picture, the zener diodes network protect the IC against any potential ESD discharge that could appear on the pins. The first ESD diode connected to the pad, exhibits a parasitic capacitance. When this parasitic capacitance (10 pF typically) is combined with R_{dem}, a re−start delay is created and the possibility to switch right in the drain−source wave exists. This guarantees QR operation with all the associated benefits (low EMI, no turn−on losses etc.). R_{dem} should be calculated to limit the maximum current flowing through pin 1 to less than +3/−2 mA: If during turn−on, the auxiliary winding delivers 30 V (at the highest line level), then the minimum R_{dem} value is defined by: (30 + 0.7)/3 mA = 10.2 kΩ. This value will be further increased to introduce a re−start delay and also a slight filtering in case of high leakage energy.

Figure 22 portrays a typical V_{DS} shot at nominal output power.

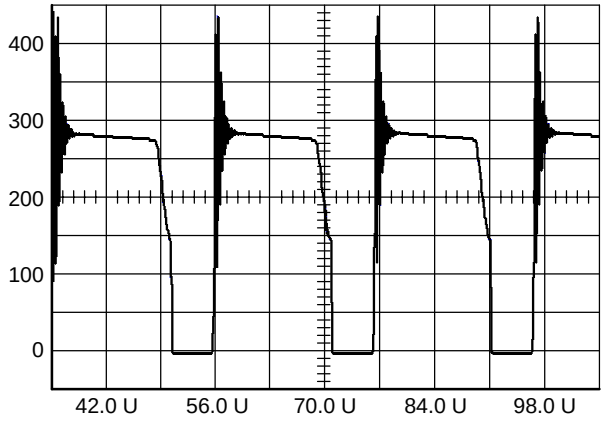


Figure 22. The DAP006 Operates in Borderline / Critical Operation

Overvoltage Protection

The overvoltage protection works by sampling the plateau voltage 4.5 μs after the turn−off sequence. This delay guarantees a clean plateau, providing that the leakage inductance ringing has been fully damped. If this would not be the case, the designer should install a small RC damper across the transformer primary inductance connections. Figure 23 shows where the sampling occurs on the auxiliary winding.

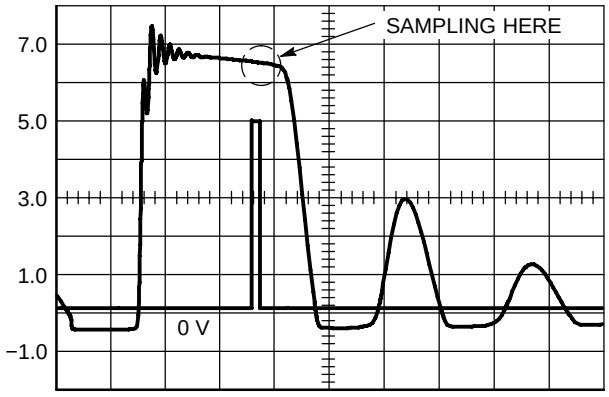


Figure 23. A voltage sample is taken 4.5 μs after the turn−off sequence

When an OVP condition has been detected, the DAP006 enters a latch−off phase and stops all switching operations. The controller stays fully latched in this position and the DSS is still active, keeping the V_{CC} between 10/12 V as in normal operations. This state lasts until the V_{CC} is cycled down 4.0 V, e.g. when the user un−plugs the power supply from the mains outlet.

By default, the OVP comparator is biased to a 2.6 V reference level and pin1 is routed via a divide by 2.77 network. As a result, when V_{pin1} reaches 7.2 V, the OVP comparator is triggered. The threshold can thus be adjusted by either modifying the power winding to auxiliary winding turn ratios to match this 7.2 V level or insert a resistor from pin1 to ground to cope with your design requirement.

Latching Off the DAP006

In certain cases, it can be very convenient to externally shut down permanently the DAP006 via a dedicated signal, e.g. coming from a temperature sensor. The reset occurs when the user un−plugs the power supply from the mains outlet. To trigger the latch−off, a simple PNP transistor can do the work, as Figure 24 shows.

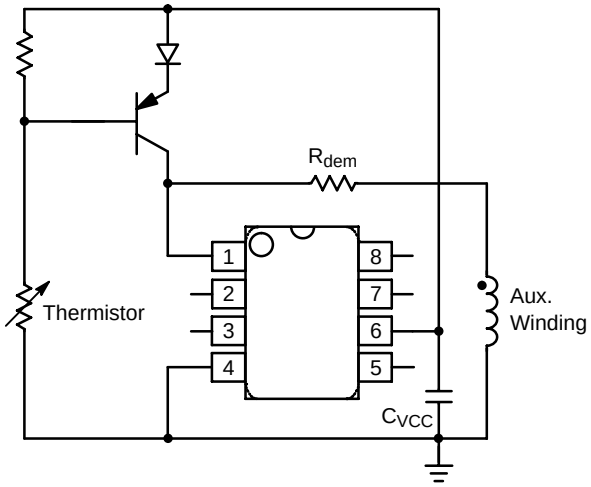


Figure 24. A simple transistor arrangement triggers the latch−off as soon as the temperature exceeds a given setpoint

Shutting Off the DAP006

Shutdown can easily be implemented through a simple NPN bipolar transistor as depicted by Figure 25. When OFF, Q1 is transparent to the operation. When forward biased, the transistor pulls the FB pin to ground ($V_{CE(sat)} \approx 200$ mV) and permanently disables the IC. A small time constant on the transistor base will avoid false triggering (Figure 25).

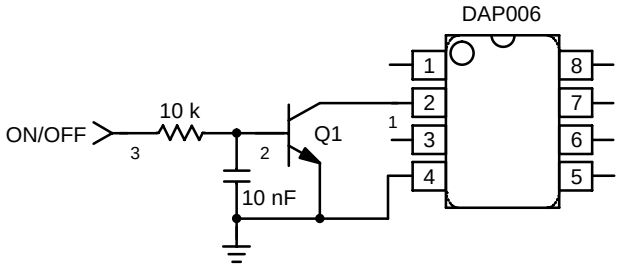


Figure 25. A simple bipolar transistor totally disables the IC

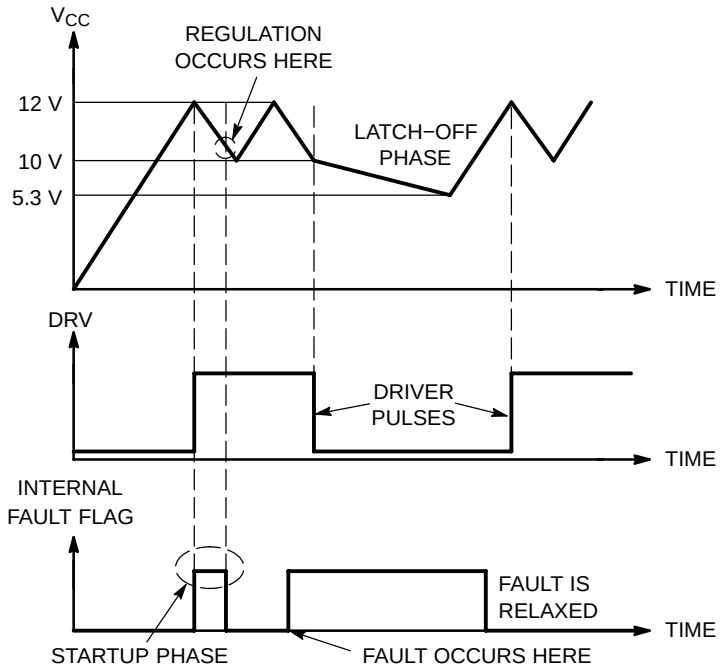
Power Dissipation

The SOIC package offers a $R_{\theta J-A}$ of 178°C/W when wired on a min pad area. Adding some copper surface around the PCB footprint will help decrease this number: 12 mm x 12 mm to drop $R_{\theta J-A}$ down to 100°C/W with 35 μ copper thickness (1 oz.) or 6.5 mm x 6.5 mm with 70 μ copper thickness (2 oz.). Care must be taken to not exceed the maximum dissipated power that can be computed using: $P_{max} = \frac{T_{Jmax} - T_{Amax}}{R_{\theta J-A}}$ which is 310 mW for T_{Jmax} = 125°C, T_A = 70°C and the min $R_{\theta J-A}$. The main power dissipation (excluding the ohmic discharge losses in the driver stage) is given by $P = I_{CC} \times V_{CC}$. I_{CC} corresponds to the internal IC consumption at a given switching frequency F_{sw-max} (the maximum is the worst case) plus the MOSFET driving current. If we assume that our system operates at 90 kHz from a 13 V V_{CC} level and considering an internal consumption of 1.0 mA, then the maximum gate charge Q_g shall be less than: $Q_g \leq \frac{\frac{P_{max}}{V_{CCmax}} - I_{CC1}}{F_{sw-max}}$ or a Q_{gmax} less than 250 nC. If larger MOSFETs are required, or if one wants to lower T_J, please refer to AND8069 available to download from www.onsemi.com/pub/ncp1200.

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short−circuit protection. A short−circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the FB pin level is pulled up to 4.2 V, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken optocoupler. To account for this situation, DAP006 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty−cycle. The system recovers when the fault condition disappears.

During the start−up phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time−out used by this IC works with the V_{CC} decoupling capacitor: as soon as the V_{CC} decreases from the U_{VLOH} level (typically 12 V) the device internally watches for an overload current situation. If this condition is still present when the U_{VLOL} level is reached, the controller stops the driving pulses, prevents the self−supply current source to restart and puts all the circuitry in standby, consuming as little as 330 μA typical (ICC3 parameter). As a result, the V_{CC} level slowly discharges toward 0. When this level crosses 5.3 V typical, the controller enters a new startup phase by turning the current source on: V_{CC} rises toward 12 V and again delivers output pulses at the U_{VLOH} crossing point. If the fault condition has been removed before U_{VLOL} approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 26 shows the evolution of the signals in presence of a fault.



If the fault is relaxed during the Vcc natural fall down sequence, the IC automatically resumes.
If the fault still persists when Vcc reached U_{VLOL}, then the controller cuts everything off until recovery.

Figure 26.

Soft−Start

The DAP006 features an internal 4 ms soft−start to soften the constraints occurring in the power supply during start−up. It is activated during the power on sequence. As soon as V_{CC} reaches $V_{CC(off)}$, the peak current is gradually increased from nearly zero up to the maximum clamping level (e.g. 1.0 V). The soft−start is also activated during the over current burst (OCP) sequence. Every restart attempt is followed by a soft−start activation. Generally speaking, the soft−start will be activated when V_{CC} ramps up either from zero (fresh power—on sequence) or 5.3 V, the latch—off voltage occurring during OCP.

Calculating the Vcc Capacitor

As the above section describes, the fall down sequence depends upon the V_{CC} level: how long does it take for the V_{CC} line to go from 12 V to 10 V? The required time depends on the start−up sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 12 V to 10 V, otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6.0 ms. Therefore a V_{CC} fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 1.6 mA (e.g. with a 10 nC Qg), we can calculate the required capacitor using the following formula: $\Delta t = \frac{\Delta V \cdot C}{i}$, with ΔV = 2.0 V. Then for a wanted Δt of 10 ms, C equals 9.0 μF or 22 μF for a standard value. When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to 330 μA typical. This happens at V_{CC} = 10 V and it remains stuck until V_{CC} reaches 5.3 V: we are in latch−off phase. Again, using the calculated 22 μF and 600 μA current consumption, this latch−off phase lasts: (10 − 5.3) x 22 μ/330 μ = 313 ms.

Protecting Pin 8 Against Negative Spikes

As any CMOS controller, DAP006 is sensitive to negative voltages that could appear on its pins. To avoid any adverse latch−up of the IC, we strongly recommend to insert a resistor in series with pin 8 or apply Figure 2 trick. This resistor (or this diode in case of Figure 2) prevents from adversely latching the controller in case of negative spikes appearing on the bulk capacitor during the power−off sequence. A typical value of 6.8 kΩ/0.5 W is suitable. When using an auxiliary winding, this resistor does not dissipate any power since it only sees current during the startup sequence and during overload.

Operation Shots

Below are some oscilloscope shots captured at V_{in} = 120 VDC with a transformer featuring an 800 μH primary inductance.

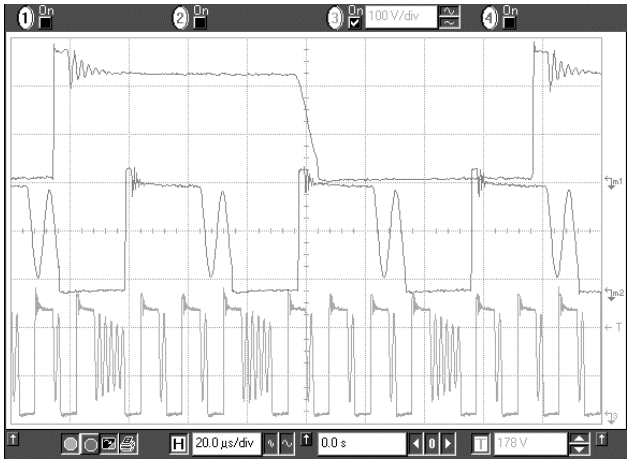


Figure 27.

This plot gathers waveforms captured at three different operating points:

1st upper plot: free run, valley switching operation, P_{out} = 26 W

2nd middle plot: min T_{off} clamps the switching frequency and selects the second valley

3rd lowest plot: the skip slices the second valley pattern and will further expand the burst as P_{out} goes low

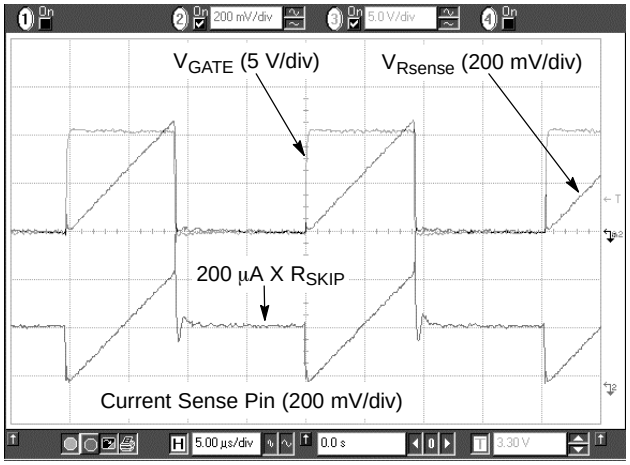


Figure 28.

This picture explains how the 200 μA internal offset current creates the skip cycle level.

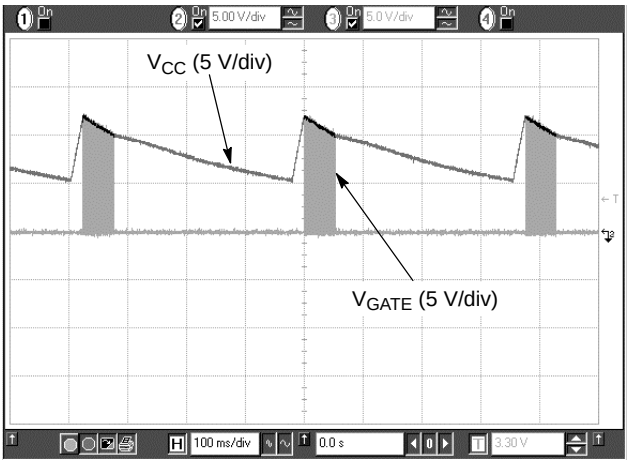


Figure 29.

The short−circuit protection forces the IC to enter burst in presence of a secondary overload.

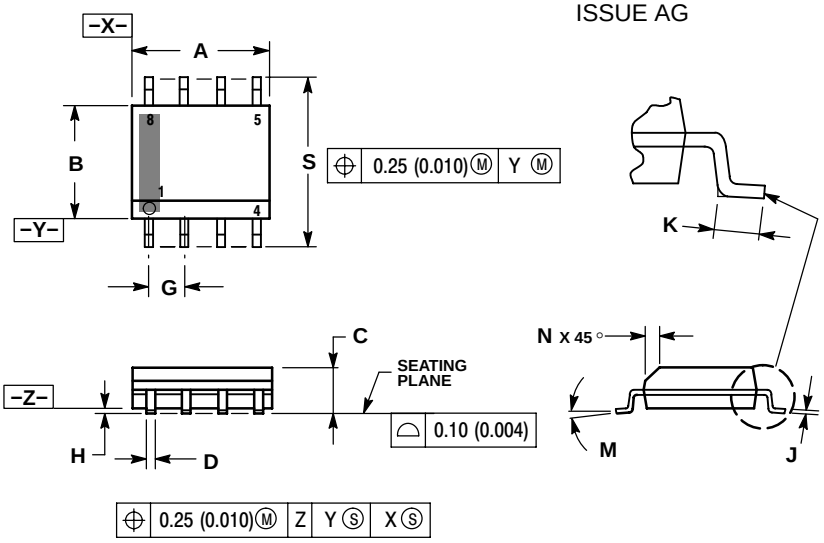
ORDERING INFORMATION

Device	Type	Marking	Package	Shipping
SCY99006R2	DAP006	DAP6	SOIC−8	2500/Tape & Reel

DAP006

PACKAGE DIMENSIONS

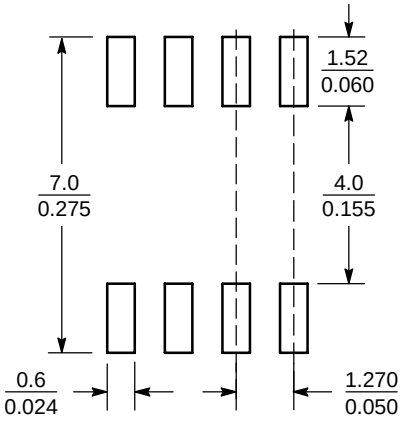
(SO−8)
D1, D2 SUFFIX
CASE 751−07
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The product described herein (DAP006), may be covered by one or more of the following U.S. patents: 6,385,060; 6,385,061. There may be other patents pending.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.