-100mA / -50V Digital transistors (with built-in resistors)

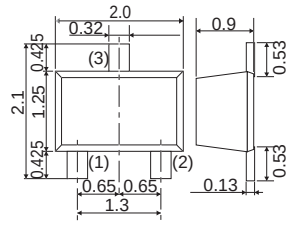
DTA114TUB

●Applications
Inverter, Interface, Driver

●Features
1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
2) The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
3) Only the on/off conditions need to be set for operation, making the device design easy.

●Dimensions (Unit : mm)

UMT3F



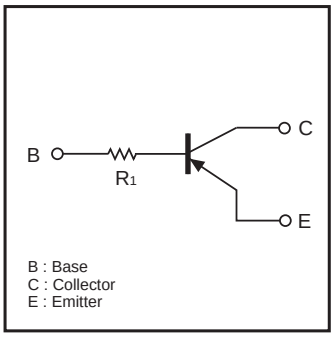
Each lead has same dimensions

(1) Base
(2) Emitter
(3) Collector

Abbreviated symbol : 94

●Structure
PNP silicon epitaxial planar transistor type
(Resistor built-in)

●Equivalent circuit



R_1=10kΩ

●Packaging specifications

Part No.	Package	UMT3F
	Packaging type	Taping
	Code	TL
	Basic ordering unit (pieces)	3000
DTA114TUB		○

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	–50	V
Collector-emitter voltage	V_{CEO}	–50	V
Emitter-base voltage	V_{EBO}	–5	V
Collector current	I_C	–100	mA
Power dissipation *	P_D	200	mW
Junction temperature	Tj	150	°C
Range of storage temperature	Tstg	–55 to +150	°C

* Each terminal mounted on a recommended land

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-emitter breakdown voltage	BV_{CEO}	–50	–	–	V	I_C=–1mA
Collector-base breakdown voltage	BV_{CBO}	–50	–	–	V	I_C=–50μA
Emitter-base breakdown voltage	BV_{EBO}	–5	–	–	V	I_E=–50μA
Collector cutoff current	I_{CBO}	–	–	–500	nA	V_{CB}=–50V
Emitter cutoff current	I_{EBO}	–	–	–500	nA	V_{EB}=–4V
Collector-emitter saturation voltage	$V_{CE(sat)}$	–	–	–0.3	V	I_C=–10mA, I_B=–1mA
DC current gain	h_{FE}	100	250	600	–	V_{CE}=–5V, I_C=–1mA
Transition frequency	f_T *	–	250	–	MHz	V_{CE}=–10V, I_E=5mA, f=100MHz
Input resistance	R_1	7	10	13	kΩ	–

* Characteristics of built-in transistor

●Electrical characteristic curves

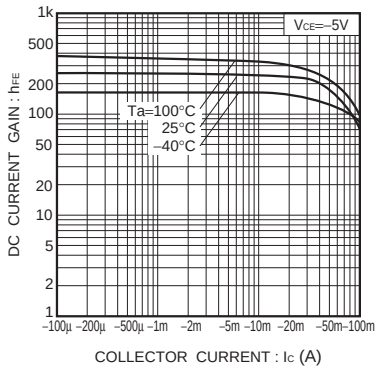


Fig.1 DC current gain vs. collector current

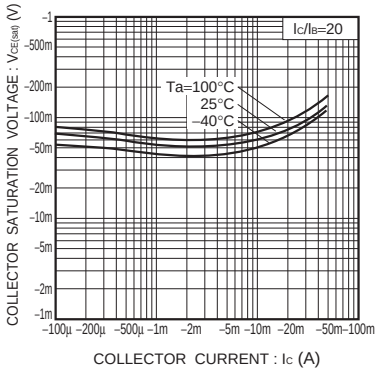


Fig.2 Collector-emitter saturation voltage vs. collector current

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