



## ICS1526

### Video Clock Synthesizer

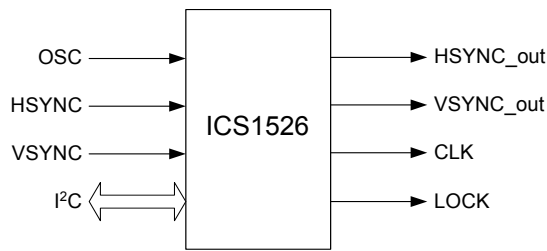
#### General Description

The ICS1526 is a low-cost, high-performance frequency generator. It is suited to general purpose phase controlled clock synthesis as well as line-locked and genlocked high-resolution video applications. Using ICS's advanced low-voltage CMOS mixed-mode technology, the ICS1526 is an effective clock synthesizer that supports video projectors and displays at resolutions from VGA to beyond XGA.

The ICS1526 offers single-ended clock outputs to 110 MHz. The HSYNC\_out, and VSYNC\_out pins provide the regenerated versions of the HSYNC and VSYNC inputs synchronous to the CLK output.

The advanced PLL uses its internal programmable feedback divider. The device is programmed by a standard I<sup>2</sup>C-bus™ serial interface and is available in a TSSOP16 package.

#### ICS1526 Functional Diagram



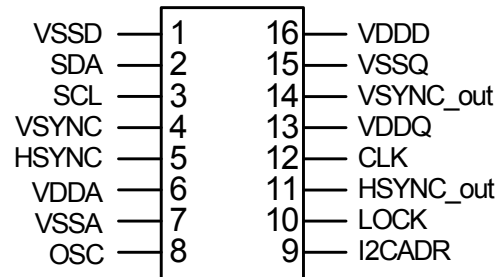
#### Features

- Lead-free packaging (Pb-free)
- Low jitter (typical 27 ps short term jitter)
- Wide input frequency range
  - 8 kHz to 100 MHz
- LVCMOS single-ended clock outputs
  - Up to 110 MHz
- Uses 3.3 V power supply
- 5 Volt tolerant Inputs (HSYNC, VSYNC)
- Coast (ignore HSYNC) capability via VSYNC pin
- Industry standard I<sup>2</sup>C-bus programming interface
- PLL Lock detection via I<sup>2</sup>C or LOCK output pin
- 16-pin TSSOP package

#### Applications

- Frequency synthesis
- LCD monitors, video projectors and plasma displays
- Genlocking multiple video subsystems

#### Pin Configuration (16-pin TSSOP)





## Section 1 Overview

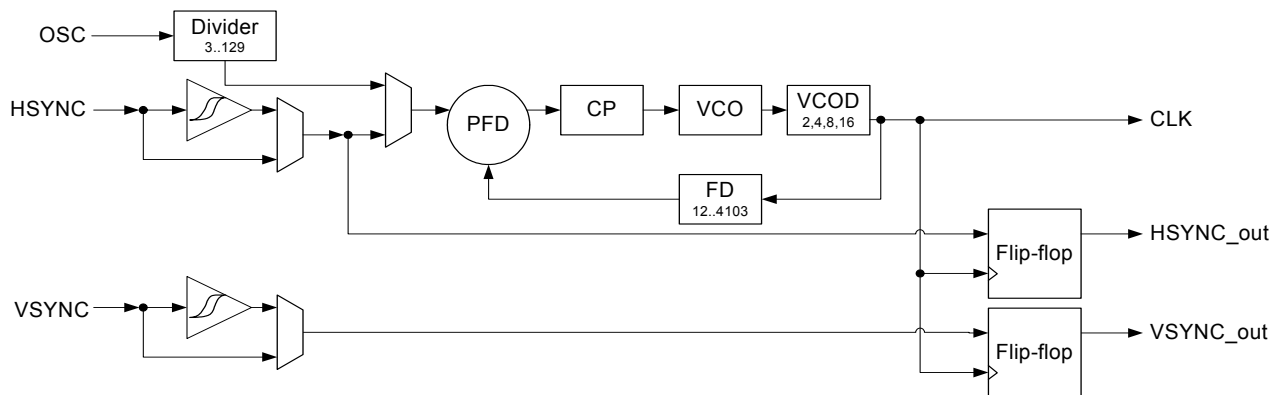
The ICS1526 is a user-programmable, high-performance general purpose clock generator. It is intended for graphics system line-locked and genlocked applications and provides the clock signals required by high-performance analog-to-digital converters.

The ICS1526 has the ability to operate in line-locked mode with the HSYNC input.

### 1.1 Phase-Locked Loop

The phase-locked loop has a very wide input frequency range (8 kHz to 100 MHz). Not only is the ICS1526 an excellent, general purpose clock synthesizer, but it is also capable of line-locked operation. Refer to the block diagram below.

**Figure 1-1 Simplified Block Diagram**



Note: Polarity controls and other circuit elements are not shown in above diagram for simplicity

The heart of the ICS1526 is a voltage controlled oscillator (VCO). The VCO's speed is controlled by the voltage on the loop filter. This voltage will be described later in this section.

The VCO's clock output is first passed through the VCO Divider (VCOD). The VCOD allows the VCO to operate at higher speeds than the required output clock.

**NOTE:** Under normal, locked operation the VCOD has no effect on the speed of the output clocks, just the VCO frequency.

The output of the VCOD is the full speed output frequency seen on the CLK. This clock is then sent through the 12-bit internal Feedback Divider (FD). The feedback divider controls how many clocks are seen during every cycle of the input reference.

The Phase Frequency Detector (PFD) then compares the feedback to the input and controls the filter voltage by enabling and disabling the charge pump. The charge pump has programmable current drive and will source and sink current as appropriate to keep the input and the clock output aligned.

The input HSYNC and VSYNC can be conditioned by a high-performance Schmitt-trigger by sharpening the rising/falling edge.

The HSYNC\_out and VSYNC\_out signals are aligned with the output clock (CLK) via a set of flip flops.

### 1.2 Output Drivers and Logic Inputs

The ICS1526 uses low-voltage TTL (LVTTTL) inputs and LVC MOS outputs, operating at the 3.3 V supply voltage. The LVTTTL inputs are 5 V tolerant.

The LVC MOS drive resistive terminations or transmission lines.

### 1.3 Automatic Power-On Reset Detection

The ICS1526 has automatic power-on reset detection (POR) circuitry and it resets itself if the supply voltage drops below threshold values. No external connection to a reset signal is required.



## 1.4 I<sup>2</sup>C Bus Serial Interface

The ICS1526 uses a 5 volt tolerant, industry-standard I<sup>2</sup>C-bus serial interface that runs at either low speed (100 kHz) or high speed (400 kHz). The interface uses 12 word addresses for control and status: one write-only, eight read/write, and three read-only addresses.

Two ICS1526 devices can sit on the same I<sup>2</sup>C bus, each selected by the Master according to the state of the I2CADR pin. The 7-bit device address is 0100110 (binary) when I2CADR is low. The device address is 0100111 (binary) when I2CADR is high. See [Section 4, "Programming"](#)



## Section 2 Pin Descriptions

Table 2-1 ICS1526 Pin Descriptions

PIN NO.	PIN NAME	TYPE	DESCRIPTION	COMMENTS	Notes
1	VSSD	POWER	Digital ground		
2	SDA	IN/OUT	Serial data	I <sup>2</sup> C-bus	1
3	SCL	IN	Serial clock	I <sup>2</sup> C-bus	1
4	VSYNC	IN	Vertical sync		1 & 2
5	HSYNC	IN	Horizontal sync	Clock input to PLL	1 & 2
6	VDDA	POWER	Analog supply	Power for analog circuitry	
7	VSSA	POWER	Analog ground	Ground for analog circuitry	
8	OSC	IN	Oscillator	Input from crystal oscillator package	1 & 2
9	I2CADR	IN	I <sup>2</sup> C device address	Chip I <sup>2</sup> C address select	
10	LOCK	LVC MOS OUT	Lock	PLL Lock detect	
11	HSYNC_out	LVC MOS OUT	HSYNC output	Schmitt-trigger filtered HSYNC realigned with the output pixel clock	
12	CLK	LVC MOS OUT	Pixel clock output	LVC MOS driver for full speed clock	
13	VDDQ	POWER	Output driver supply	Power for output drivers	
14	VSYNC_out	LVC MOS OUT	VSYNC output	Schmitt-trigger filtered VSYNC realigned with the output pixel clock	
15	VSSQ	POWER	Output driver ground	Ground for output drivers	
16	VDDD	POWER	Digital supply	Power for digital sections	

Notes: 1. These LVTTTL inputs are 5 V tolerant.  
2. Connect to ground if unused.



## Section 3 Register map summary

Word Address	Name	Access	Bit Name	Bit#	Reset Value	Description
00h	Input Control	R / W	CPen	0	1	Charge Pump Enable 0=External Enable via VSYNC, 1=Always Enabled
			VSYNC_Pol	1	0	VSYNC Polarity (Charge Pump Enable) Requires 00h:0=0 0=Coast (charge pump disabled) while VSYNC low, 1=Coast (charge pump disabled) while VSYNC high
			HSYNC_Pol	2	0	HSYNC Polarity 0=Rising Edge, 1=Falling Edge
			Reserved	3	0	Reserved
			Reserved	4	0	Part requires a 0 for correct operation
			Reserved	5	0	Reserved
			EnPLS	6	1	Enable PLL Lock Output 0=Disable, 1=Enable
			Reserved	7	0	Reserved
01h	Loop Control <sup>*</sup>	R / W	ICP0-2	0-2		ICP (Charge Pump Current) Bit 2,1,0 = {000 = 1 $\mu$ A, 001 = 2 $\mu$ A, 010 = 4 $\mu$ A... 110 = 64 $\mu$ A, 111 = 128 $\mu$ A}. Increasing the PF Detector Gain makes the loop respond faster, raising the loop bandwidth. The typical value when using the internal loop filter is 011.
			Reserved	3		Reserved
			VCOD0-1	4-5		VCO Divider Bit 5,4 = {00 = $\div$ 2, 01 = $\div$ 4, 10 = $\div$ 8, 11 = $\div$ 16}
			Reserved	6-7		Reserved
02h	FdBk Div 0 <sup>*</sup>	R / W	FBD0-7	0-7		Feedback Divider LSBs (bits 0-7)
03h	FdBk Div 1 <sup>*</sup>	R / W	FBD8-11	0-3		Feedback Divider MSBs (bits 8-11) Divider setting = 12-bit word + 8 Minimum 12 = 00000000100 Maximum 4103 = 111111111111
			Reserved	4-7		Reserved
04h	Reserved		Reserved	0-7	0	Reserved
05h	Schmitt-trigger	R / W	Schmitt control	0	1	Schmitt-trigger control 0=Schmitt-trigger, 1=No Schmitt-trigger
			Metal_Rev	1-7	0	Metal Mask Revision Number
06h	Output Enables	R / W	Reserved	0	0	Reserved
			OE	1	0	Output Enable for CLK, HSYNC_out, VSYNC_out 0=High Impedance (disabled), 1=Enabled
			Reserved	2-7	0	Reserved



Word Address	Name	Access	Bit Name	Bit#	Reset Value	Description
07h	Osc_Div	R / W	Osc_Div 0-6	0-6	0	Osc Divider modulus Minimum 3 = 0000001 binary, Maximum 129 = 1111111 binary Divider setting = 7-bit word + 2
			In-Sel	7	0	Input Select 0=HSYNC Input, 1=OSC Input OSC input clock must be present to select OSC input
08h	Reset	Write	PLL	0-7	x	Writing 5Ah resets PLL and commits values written to word addresses 01h-03h and 05h
09-0Fh	Reserved	Read	Reserved	0-7		Reserved
10h	Chip Ver	Read	Reserved	0-7		Reserved
11h	Chip Rev	Read	Chip Rev	0-7	01	Reserved
12h	Rd_Reg	Read	Reserved	0	N/A	Reserved
			PLL_Lock	1	N/A	PLL Lock Status 0=Unlocked, 1=Locked
			Reserved	2-7	0	Reserved

\*. Written values to these registers do not take effect immediately, but require a commit via register 08h

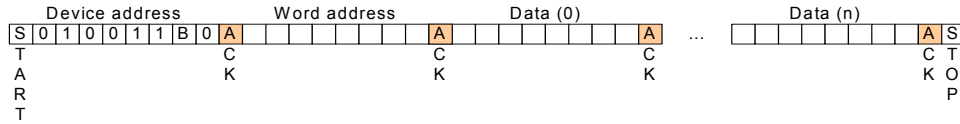


# Section 4 Programming

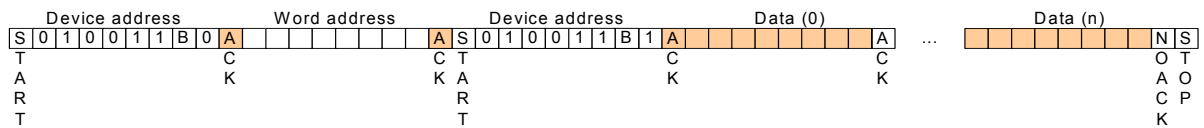
## 4.1 Industry-Standard I<sup>2</sup>C Serial Bus: Data Format

Figure 4-1 ICS1526 Data Format for I<sup>2</sup>C 2-Wire Serial Bus

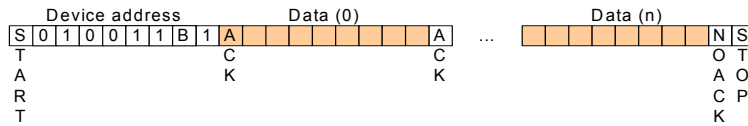
Single/multiple register write (page write)



Single/multiple register read



Sequential single/multiple register read



□ Master drives line      □ Slave drives line

Notes:

The ICS1526 uses 16-byte pages (00h-0Fh is the first page, 10h-1Fh is the second page). Writing or reading beyond the end of page yields undefined results.

The ICS1526 has a device address of 010011B, where B is the state of the I2CADR pin.



## Section 5 AC/DC Operating Conditions

### 5.1 Absolute Maximum Ratings

Table 5-1 lists absolute maximum ratings for the ICS1526. Stresses above these ratings can cause permanent damage to the device. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the ICS1526 at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 5-1 ICS1526 Absolute Maximum Ratings

Item	Rating
VDD, VDDA, VDDQ (measured to VSS)*	4.3 V
Digital Inputs	VSS -0.3 V to 5.5 V
Analog Inputs	VSS -0.3 V to 6.0 V
Analog Outputs	VSSA -0.3 V to VDDA +0.3 V
Digital Outputs	VSSQ -0.3 V to VDDQ +0.3 V
Storage Temperature	-65°C to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD Susceptibility*	> 2 kV**

\*. Measured with respect to VSS. During normal operations, the VDD supply voltage for the ICS1526 must remain within the recommended operating conditions.

\*\* Electrostatic-sensitive devices. Do not open or handle except in a static-free workstation.

Table 5-2 Environmental Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0	-	+70	°C
Power Supply Voltage	+3.0	+3.3	+3.6	V

Table 5-3 DC Characteristics

Parameter	Symbol	Conditions	Min.	Max.	Units
Digital Supply Current	IDDD	VDDD = 3.6 V	-	25	mA
Output Driver Supply Current	IDDQ	VDDD = 3.6 V No drivers enabled	-	6	mA
Analog Supply Current	IDDA	VDDA = 3.6 V	-	5	mA
Power consumption				300	mW
Power-On-Reset (POR) Threshold		VSS		1.8	V





Table 5-4 AC Characteristics

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
<b>General</b>						
VCO Frequency	$f_{VCO}$	40		400	MHz	
VCO Gain	K		165		MHz/V	
<b>AC Inputs</b>						
OSC Input Frequency	$f_{OSC}$	0.02		100	MHz	
<b>Analog Input (HSYNC/VSYNC)</b>						
HSYNC Input Frequency	$f_{HSYNC}$	8		10,000	kHz	
VSYNC Input Frequency	$f_{VSYNC}$	30		120	Hz	
Input High Voltage	$V_{IH}$	1.7		5.5	V	
Input Low Voltage	$V_{IL}$	VSS - 0.3		1.1	V	
Input Hysteresis		0.2		0.8	V	Schmitt trigger active
<b>SDA, SCL, OSC Digital Inputs</b>						
Input High Voltage	$V_{IH}$	2		5.5	V	
Input Low Voltage	$V_{IL}$	VSS - 0.3		0.8	V	
<b>I<sup>2</sup>CADDR Digital Input</b>						
Input High Voltage	$V_{IH}$	2		VDD+0.3	V	
Input Low Voltage	$V_{IL}$	VSS - 0.3		0.8	V	
<b>SDA Digital Output</b>						
SDA Output Low Voltage	$V_{OL}$			0.4	V	IOUT = 3 mA
SDA Output High Voltage	$V_{OH}$			6.0	V	Determined by external Rset resistor
<b>LVC MOS Outputs (CLK, HSYNC_out, VSYNC_out, LOCK)</b>						
Output Frequency	$F_s$	2.5		110	MHz	VDDD = 3.3 V
Duty Cycle	$S_{DC}$	45	50	55	%	2
Jitter, STJ, RMS	STJ		0.027		ns	30 kHz input to 50 MHz output
Jitter, STJ, pk-pk	STJ		0.200		ns	
Jitter, Input-Output	IOJ		2.500		ns	HSYNC in to CLK out
HSYNC to HSYNC_out propagation delay (without Schmitt trigger)			2	9	ns	1
HSYNC to HSYNC_out propagation delay (with Schmitt-trigger)			6	10	ns	1
CLK to HSYNC_out/ VSYNC_out skew				1.0	ns	
Clock/ HSYNC_out/ VSYNC_out Transition Time - Rise	$T_{CR}$		1.0	1.5	ns	2



Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Clock/ HSYNC_out/ VSYNC_out Transition Time - Fall	$T_{CF}$		1.0	1.5	ns	2
LOCK Transition Time - Rise	$T_{LR}$			3.0	ns	2
LOCK Transition Time - Fall	$T_{LF}$			2.0	ns	2

Note 1—Measured between chosen edge of HSYNC (00h:2) and rising edge of output

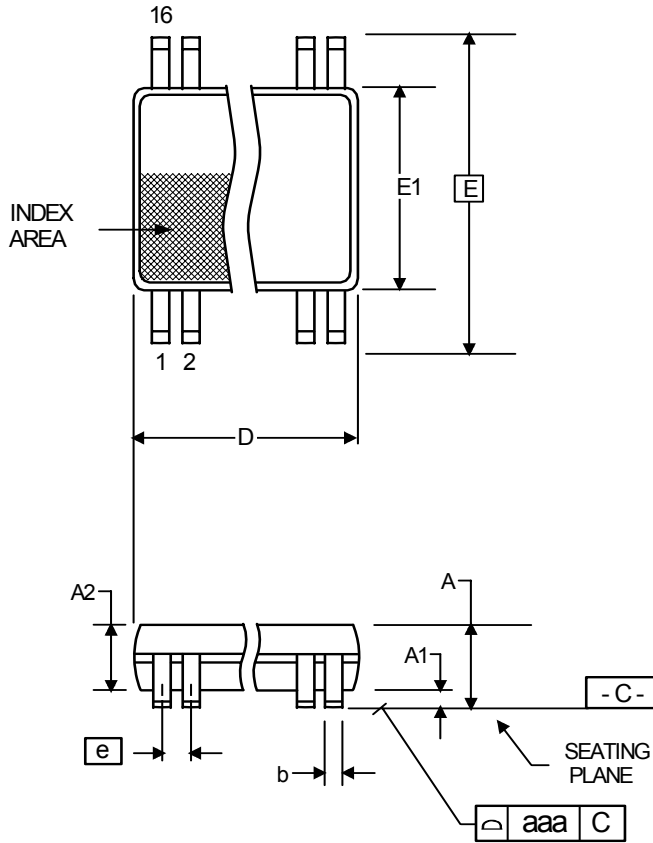
Note 2—Measured at 110 MHz, 3.3 VDC, 25°C, 15 pF, unterminated



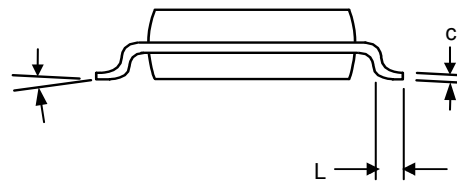
## Section 6 Package Outline and Package Dimensions

### 16-pin TSSOP 4.40 mm body, 0.65 mm pitch

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
$\alpha$	0°	8°	0°	8°
aaa	--	0.10	--	0.004



## Section 7 Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS1526GLF	1526GLF	Tubes	16-pin TSSOP	0 to +70° C
ICS1526GLFTR	1526GLF	Tape & Reel	16-pin TSSOP	0 to +70° C

“LF” denotes Pb (lead) free package.

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