27 MHZ FIXED AND SPREAD CLOCK GENERATOR ICS8OSK270

Description

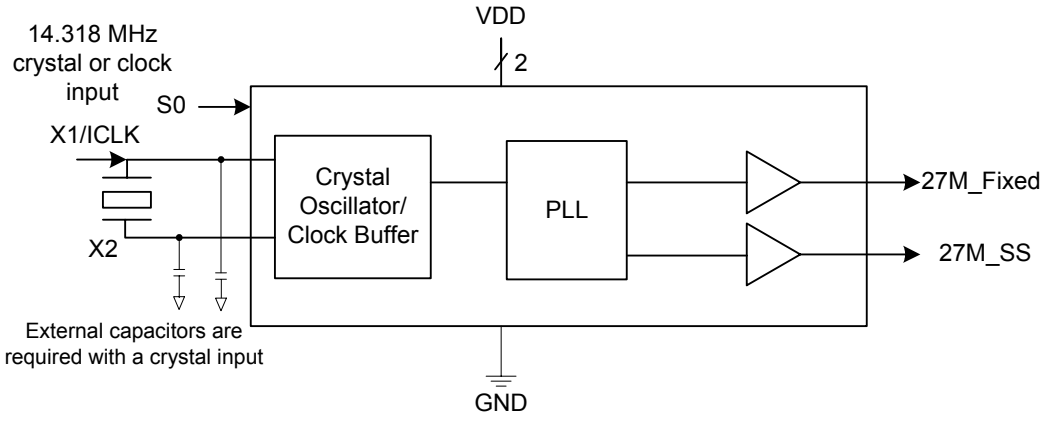
The ICS8OSK270 is a low cost integrated clock synthesizer solution replacing crystals and crystal oscillators.

The ICS8OSK270 generates a very accurate 27.00 MHz fixed clock output, and a 27.00 MHz spread spectrum clock output from a 14.31818 MHz reference clock or crystal input.

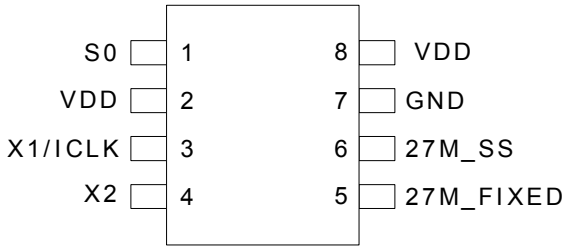
Features

- 14.31818 MHz crystal or clock input
- The 27 MHz_Fixed clock output is non-spread with <10 ppm synthesis error
- 27 MHz_SS clock output with selectable spread spectrum for EMI reduction
- Output duty cycle 45/55% (worst case)
- Advanced, low-power CMOS process
- Industrial temperature range (-40 to 85°C)
- Packaged in 8-pin MSOP (3.00 mm body)
- RoHS 5 (green) or RoHS 6 (green and lead free) compliant packaging

Block Diagram



Pin Assignment



Spread Spectrum Percentage Selection Table

S0	27M_SS Down Spread
0	-0.5%
1	-1.5%

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	S0	Input	Spread Spectrum percentage select 0. See table above.
2	VDD	Power	Connect to +3.3 V.
3	X1/ICLK	Input	Crystal connection. Connect to14.31818 MHz crystal or clock input.
4	X2	Output	Crystal connection. Connect to14.31818 MHz crystal.
5	27M_FIXED	Output	27 MHz fixed clock output at 3.3 V.
6	27M_SS	Output	27 MHz spread spectrum clock output at 3.3 V.
7	GND	Power	Connect to ground.
8	VDD	Power	Connect to +3.3 V.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS8OSK270 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20].

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS8OSK270. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS8OSK270. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 V to 7 V
All Inputs	-0.5 V to VDD+0.5 V
All Outputs	-0.5 V to 2.5V+0.5 V
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD (HBM)	2000V min.
MSL (Moisture Sensitivity Level)	3

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135		+3.465	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%,** Ambient Temp -40°C to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Supply Current	IDD	No load			30	mA
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = +25 mA			0.4	V
Load Capacitance, X1 and X2	C_L	No internal load capacitance		5		pF

AC Electrical Characteristics

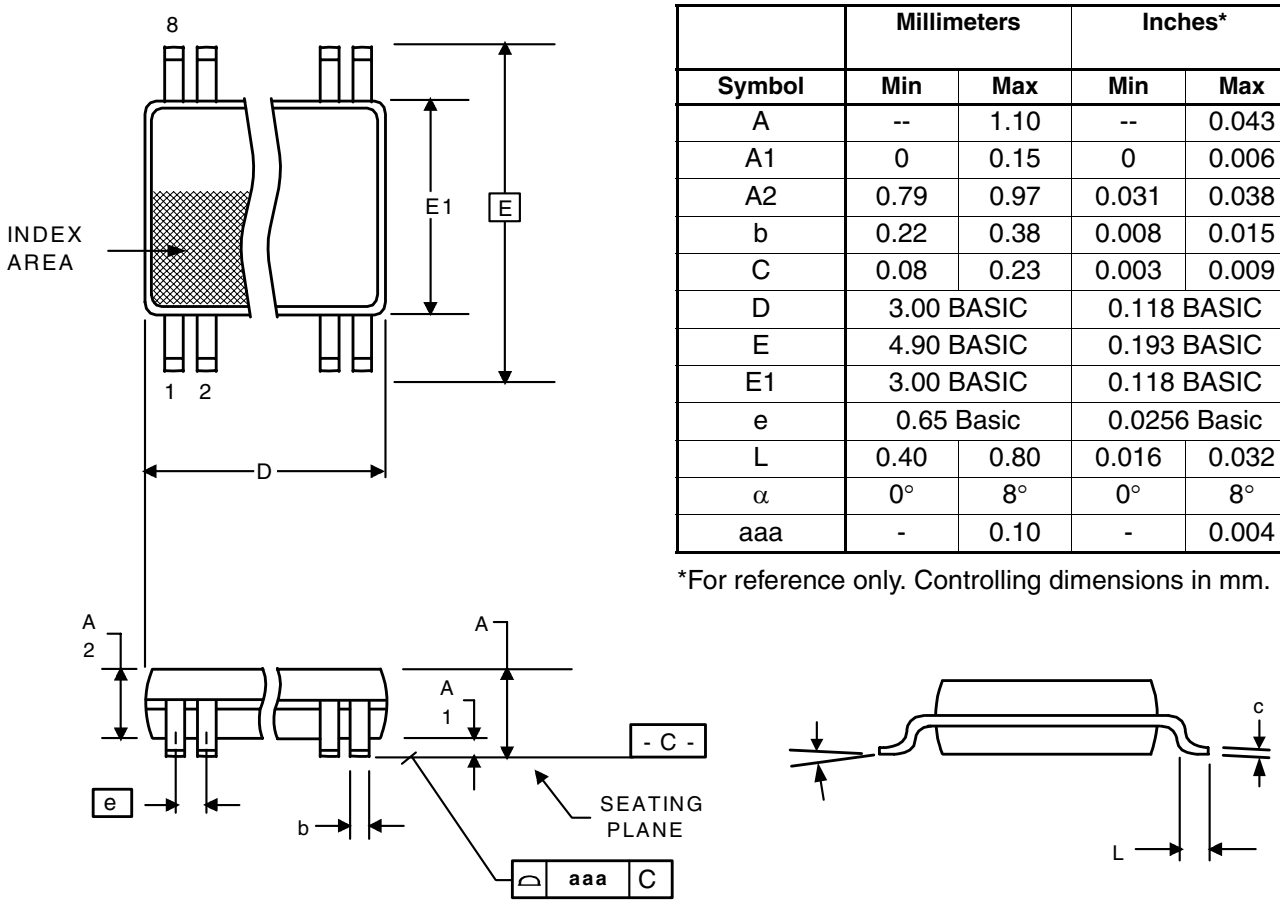
Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40°C to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}			14.31818		MHz
Output Rise Time	t_{OR}	20% to 80%, Note 1	0.7	1.0	2.2	ns
Output Fall Time	t_{OF}	80% to 20%, Note 1	0.7	1.0	2.2	ns
Output Impedance	R_O	VO=VDD/2		20		Ω
Output Clock Duty Cycle		VDD/2, Note 1	45	50	55	%
Frequency Synthesis Error		27M_FIXED			10	ppm
Short Term Jitter		Cycle-to-Cycle		100	200	ps
Long Term Jitter		27M_FIXED, n=1000		200	400	ps
Power-up Time	t_{PU}	From minimum VDD to outputs stable		1	3	ms

Note 1: Measured with a 15 pF load.

Package Outline and Package Dimensions (8-pin MSOP, 3.00 mm Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.10	--	0.043
A1	0	0.15	0	0.006
A2	0.79	0.97	0.031	0.038
b	0.22	0.38	0.008	0.015
C	0.08	0.23	0.003	0.009
D	3.00 BASIC		0.118 BASIC	
E	4.90 BASIC		0.193 BASIC	
E1	3.00 BASIC		0.118 BASIC	
e	0.65 Basic		0.0256 Basic	
L	0.40	0.80	0.016	0.032
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS8OSK270GILF	TBD	Tubes	8-pin MSOP	-40 to +85° C
ICS8OSK270GILFT		Tape and Reel	8-pin MSOP	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	J.Sarma	03/02/06	Released from Proposal to Preliminary; added TSSOP package information.
B	J.Sarma	03/08/06	Corrected the part number. The 8MSOP package part is the ICS8OSK270AGILF and the 8TSSOP package part is the ICS8OSK270GILF.
C	J.Sarma	05/04/06	Deleted the TSSOP package availability–8MSOP package only.

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