

Multiphase PWM Regulator for IMVP-6.5™ Mobile CPUs and GPUs

ISL62883C

The ISL62883C is a multiphase PWM buck regulator for microprocessor or graphics processor core power supply. The multiphase buck converter uses interleaved phase to reduce the total output voltage ripple with each phase carrying a portion of the total load current, providing better system performance, superior thermal management, lower component cost, reduced power dissipation, and smaller implementation area. The ISL62883C uses two integrated gate drivers and an external gate driver to provide a complete solution. The PWM modulator is based on Intersil's Robust Ripple Regulator (R³) technology™. Compared with traditional modulators, the R³™ modulator commands variable switching frequency during load transients, achieving faster transient response. With the same modulator, the switching frequency is reduced at light load, increasing the regulator efficiency.

The ISL62883C can be configured as CPU or graphics Vcore controller and is fully compliant with IMVP-6.5™ specifications. It responds to PSI# and DPRSLPVR signals by adding or dropping PWM3 and Phase 2 respectively, adjusting overcurrent protection threshold accordingly, and entering/exiting diode emulation mode. It reports the regulator output current through the IMON pin. It senses the current by using either discrete resistor or inductor DCR whose variation over temperature can be thermally compensated by a single NTC thermistor. It uses differential remote voltage sensing to accurately regulate the processor die voltage. The adaptive body diode conduction time reduction function minimizes the body diode conduction loss in diode emulation mode. User-selectable overshoot reduction function offers an option to aggressively reduce the output capacitors as well as the option to disable it for users concerned about increased system thermal stress. In 2-Phase configuration, the ISL62883C offers the FB2 function to optimize 1-Phase performance.

Features

- Programmable 1, 2- or 3-Phase CPU or GPU Mode of Operation
- Precision Multiphase Core Voltage Regulation
 - 0.5% System Accuracy Over-Temperature
 - Enhanced Load Line Accuracy
- Microprocessor Voltage Identification Input
 - 7-Bit VID Input, 0V to 1.500V in 12.5mV Steps
 - Supports VID Changes On-The-Fly
- Supports Multiple Current Sensing Methods
 - Lossless Inductor DCR Current Sensing
 - Precision Resistor Current Sensing
- Supports PSI# and DPRSLPVR modes
- Superior Noise Immunity and Transient Response
- Current Monitor and Thermal Monitor
- Differential Remote Voltage Sensing
- High Efficiency Across Entire Load Range
- Two Integrated Gate Drivers
- Excellent Dynamic Current Balance
- FB2 Function Optimizes 1-Phase Mode Performance
- Adaptive Body Diode Conduction Time Reduction
- User-selectable Overshoot Reduction Function
- Small Footprint 40 Ld 5x5 TQFN Packages
- Pb-Free (RoHS Compliant)

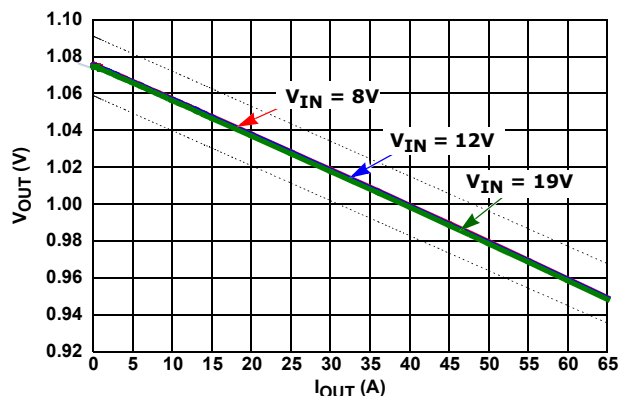
Applications* (see page 42)

- Notebook Core Voltage Regulator
- Notebook GPU Voltage Regulator

Related Literature* (see page 42)

- See [AN1460](#) for ISL62883/ISL62883C Evaluation Board Application Note "ISL62883EVAL2Z User Guide"

Load Line Regulation



ISL62883C

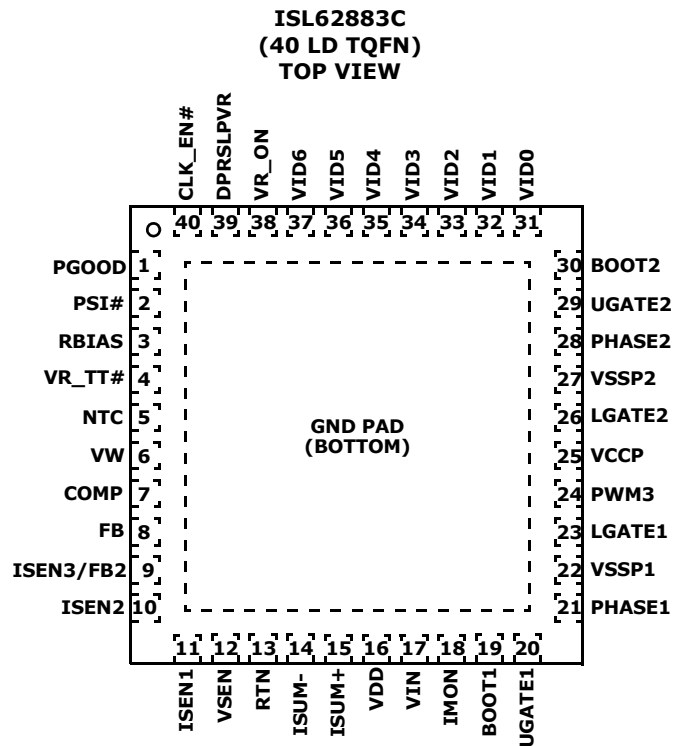
Ordering Information

PART NUMBER (Note 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL62883CIRTZ (Note 2)	62883C IRTZ	-40 to +100	40 Ld 5x5 TQFN	L40.5x5
ISL62883CIRTZ-T (Notes 1, 2)	62883C IRTZ	-40 to +100	40 Ld 5x5 TQFN	L40.5x5
ISL62883CHRTZ (Note 2)	62883C HRTZ	-10 to +100	40 Ld 5x5 TQFN	L40.5x5
ISL62883CHRTZ-T (Notes 1, 2)	62883C HRTZ	-10 to +100	40 Ld 5x5 TQFN	L40.5x5

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL62883C](#). For more information on MSL please see techbrief [TB363](#).

Pin Configuration



Functional Pin Descriptions

ISL62883C	SYMBOL	DESCRIPTION
-	GND	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.
1	PGOOD	Power-Good open-drain output indicating when the regulator is able to supply regulated voltage. Pull up externally with a 680Ω resistor to VCCP or 1.9kΩ to 3.3V.
2	PSI#	Low load current indicator input. When asserted low, indicates a reduced load-current condition.
3	RBIAS	A resistor to GND sets internal current reference. Use 147kΩ or 47kΩ. The choice of Rbias value, together with the ISEN2 pin configuration and the external resistance from the COMP pin to GND, programs the controller to enable/disable the overshoot reduction function and to select the CPU/GPU mode.
4	VR_TT#	Thermal overload output indicator.
5	NTC	Thermistor input to VR_TT# circuit.
6	VW	A resistor from this pin to COMP programs the switching frequency (8kΩ gives approximately 300kHz).
7	COMP	This pin is the output of the error amplifier. Also, a resistor across this pin and GND adjusts the overcurrent threshold.
8	FB	This pin is the inverting input of the error amplifier.
9	INSE3/FB2	When the ISL62883C is configured in 3-phase mode, this pin is ISEN3. ISEN3 is the individual current sensing for phase 3. When the ISL62883C is configured in 2-phase mode, this pin is FB2. There is a switch between the FB2 pin and the FB pin. The switch is on in 2-phase mode and is off in 1-phase mode. The components connecting to FB2 are used to adjust the compensation in 1-phase mode to achieve optimum performance.
10	ISEN2	Individual current sensing for Phase 2. When ISEN2 is pulled to 5V VDD, the controller will disable Phase 2.
11	ISEN1	Individual current sensing for phase 1.
12	VSEN	Remote core voltage sense input. Connect to microprocessor die.
13	RTN	Remote voltage sensing return. Connect to ground at microprocessor die.
14, 15	ISUM- and ISUM+	Droop current sense input.
16	VDD	5V bias power.
17	VIN	Battery supply voltage, used for feed-forward.
18	IMON	An analog output. IMON outputs a current proportional to the regulator output current.
19	BOOT1	Connect an MLCC capacitor across the BOOT1 and the PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT1 pin, each time the PHASE1 pin drops below VCCP minus the voltage dropped across the internal boot diode.
20	UGATE1	Output of the Phase-1 high-side MOSFET gate driver. Connect the UGATE1 pin to the gate of the Phase-1 high-side MOSFET.
21	PHASE1	Current return path for the Phase-1 high-side MOSFET gate driver. Connect the PHASE1 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase-1.
22	VSSP1	Current return path for the Phase-1 low-side MOSFET gate driver. Connect the VSSP1 pin to the source of the Phase-1 low-side MOSFET through a low impedance path, preferably in parallel with the traces connecting the LGATE1a and the LGATE1b pins to the gates of the Phase-1 low-side MOSFETs.
23	LGATE1	Output of the Phase-1 low-side MOSFET gate driver. Connect the LGATE1 pin to the gate of the Phase-1 low-side MOSFET.
24	PWM3	PWM output for Phase 3. When PWM3 is pulled to 5V VDD, the controller will disable Phase-3 and allow other phases to operate.

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Functional Pin Descriptions (Continued)

ISL62883C	SYMBOL	DESCRIPTION
25	VCCP	Input voltage bias for the internal gate drivers. Connect +5V to the VCCP pin. Decouple with at least 1 μ F of an MLCC capacitor to VSSP1 and VSSP2 pins respectively.
26	LGATE2	Output of the Phase-2 low-side MOSFET gate driver. Connect the LGATE2 pin to the gate of the Phase-2 low-side MOSFET.
27	VSSP2	Current return path for the Phase-2 converter low-side MOSFET gate driver. Connect the VSSP2 pin to the source of the Phase-2 low-side MOSFET through a low impedance path, preferably in parallel with the trace connecting the LGATE2 pin to the gate of the Phase-2 low-side MOSFET.
28	PHASE2	Current return path for the Phase-2 high-side MOSFET gate driver. Connect the PHASE2 pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase-2.
29	UGATE2	Output of the Phase-2 high-side MOSFET gate driver. Connect the UGATE2 pin to the gate of the Phase-2 high-side MOSFET.
30	BOOT2	Connect an MLCC capacitor across the BOOT2 and the PHASE2 pins. The boot capacitor is charged through an internal boot diode connected from the VCCP pin to the BOOT2 pin, each time the PHASE2 pin drops below VCCP minus the voltage dropped across the internal boot diode.
31 thru 37	VID0 thru VID6	VID input with VID0 = LSB and VID6 = MSB.
38	VR_ON	Voltage regulator enable input. A high level logic signal on this pin enables the regulator.
39	DPRSLPVR	Deeper sleep enable signal. A high level logic signal on this pin indicates that the microprocessor is in deeper sleep mode.
40	CLK_EN#	Open drain output to enable system PLL clock. It goes low 13 switching cycles after Vcore is within 10% of Vboot.
pad	BOTTOM	The bottom pad of ISL62883C is electrically connected to the GND pin inside the IC. It should also be used as the thermal pad for heat removal.

Block Diagram

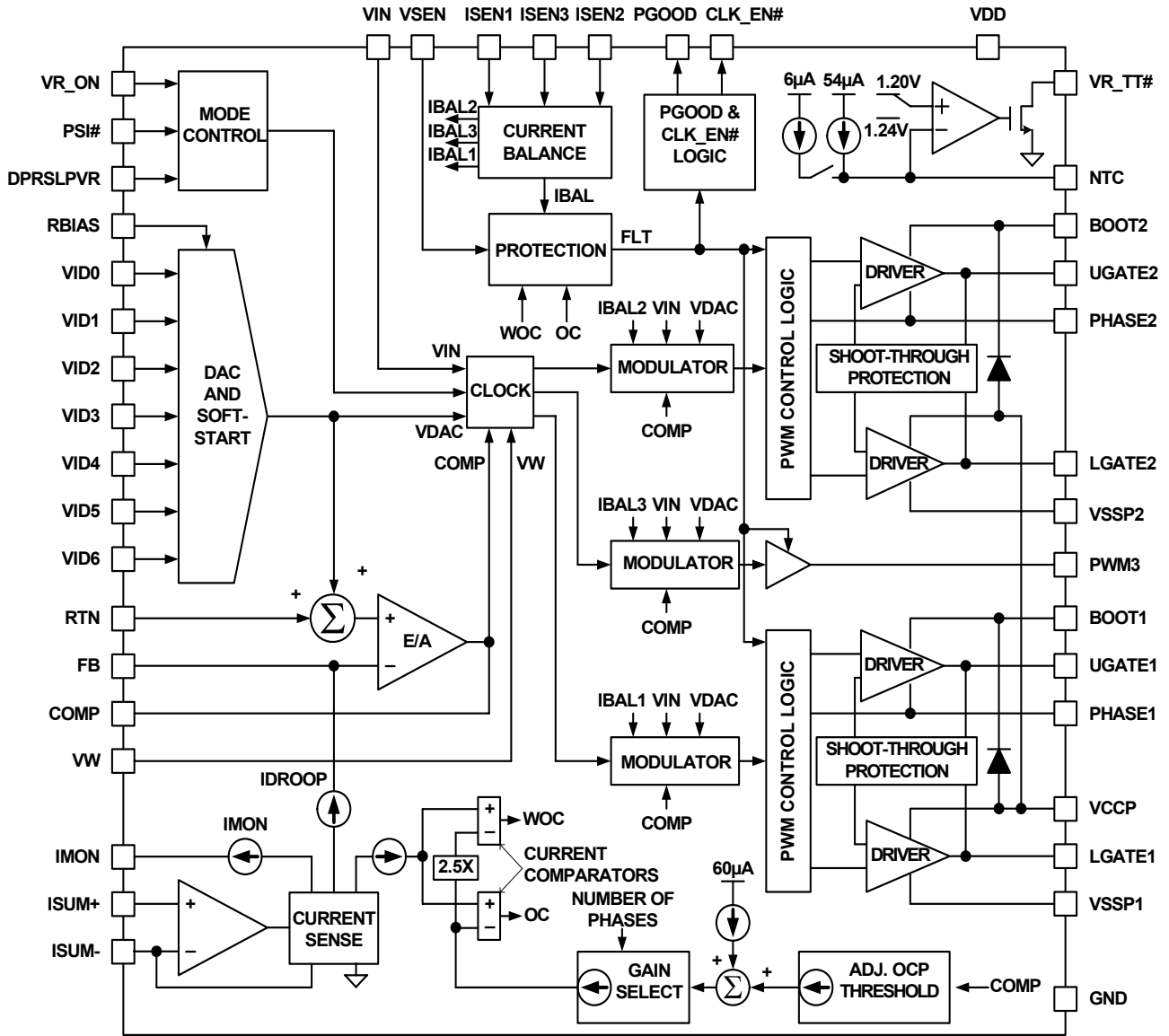


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Absolute Maximum Ratings

Supply Voltage, VDD	-0.3V to +7V
Battery Voltage, VIN	+28V
Boot Voltage (BOOT)	-0.3V to +33V
Boot to Phase Voltage (BOOT-PHASE)	-0.3V to +7V(DC) -0.3V to +9V(<10ns)
Phase Voltage (PHASE)	-7V (<20ns Pulse Width, 10μJ)
UGATE Voltage (UGATE)	PHASE-0.3V (DC) to BOOT PHASE-5V (<20ns Pulse Width, 10μJ) to BOOT
LGATE Voltage	-2.5V (<20ns Pulse Width, 5μJ) to VDD+0.3V
All Other Pins	-0.3V to (VDD +0.3V)
Open Drain Outputs, PGOOD, VR_TT#, CLK_EN#	-0.3V to +7V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld TQFN Package (Notes 4, 5)	31	2
Maximum Junction Temperature	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Maximum Junction Temperature (Plastic Package)	+150°C	
Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

Recommended Operating Conditions

Supply Voltage, VDD	+5V ±5%
Battery Voltage, VIN	+4.5V to 25V
Ambient Temperature	
ISL62883CHRTZ	-10°C to +100°C
ISL62883CIRTZ	-40°C to +100°C
Junction Temperature	
ISL62883CHRTZ	-10°C to +125°C
ISL62883CIRTZ	-40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VDD = 5V, TA = -40°C to +100°C, f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT POWER SUPPLY						
+5V Supply Current	I _{VDD}	VR_ON = 1V		4	4.6	mA
		VR_ON = 0V			1	μA
Battery Supply Current	I _{VIN}	VR_ON = 0V			1	μA
V _{IN} Input Resistance	R _{VIN}	VR_ON = 1V		900		kΩ
Power-On-Reset Threshold	POR _r	V _{DD} rising		4.35	4.5	V
	POR _f	V _{DD} falling	4.00	4.15		V
SYSTEM AND REFERENCES						
System Accuracy	HRTZ %Error (V _{CC_CORE})	No load; closed loop, active mode range VID = 0.75V to 1.50V,	-0.5		+0.5	%
		VID = 0.5V to 0.7375V	-8		+8	mV
		VID = 0.3V to 0.4875V	-15		+15	mV
	IRTZ %Error (V _{CC_CORE})	No load; closed loop, active mode range VID = 0.75V to 1.50V	-0.8		+0.8	%
		VID = 0.5V to 0.7375V	-10		+10	mV
		VID = 0.3V to 0.4875V	-18		+18	mV
V _{BOOT}		ISL62883CHRTZ	1.0945	1.100	1.1055	V
		ISL62883CIRTZ	1.0912	1.100	1.1088	V
Maximum Output Voltage	V _{CC_CORE(max)}	VID = [0000000]		1.500		V
Minimum Output Voltage	V _{CC_CORE(min)}	VID = [1100000]		0.300		V
R _{BIAS} Voltage		R _{BIAS} = 147kΩ	1.45	1.47	1.49	V

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Electrical Specifications Operating Conditions: VDD = 5V, T_A = -40°C to +100°C, f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
CHANNEL FREQUENCY						
Nominal Channel Frequency	f _{SW(nom)}	R _{fset} = 7kΩ, 3-channel operation, V _{COMP} = 1V	285	300	315	kHz
Adjustment Range			200		500	kHz
AMPLIFIERS						
Current-Sense Amplifier Input Offset		I _{FB} = 0A	-0.15		+0.15	mV
Error Amp DC Gain (Note 7)	A _{V0}			90		dB
Error Amp Gain-Bandwidth Product (Note 7)	GBW	C _L = 20pF		18		MHz
ISEN						
Imbalance Voltage		Maximum of ISENs - Minimum of ISENs			1	mV
Input Bias Current				20		nA
POWER-GOOD AND PROTECTION MONITORS						
PGOOD Low Voltage	V _{OL}	I _{PGOOD} = 4mA		0.26	0.4	V
PGOOD Leakage Current	I _{OH}	PGOOD = 3.3V	-1		1	μA
PGOOD Delay	tpgd	CLK_ENABLE# LOW to PGOOD HIGH	6.3	7.6	8.9	ms
GATE DRIVER						
UGATE Pull-Up Resistance (Note 7)	R _{UGPU}	200mA Source Current		1.0	1.5	Ω
UGATE Source Current (Note 7)	I _{UGSRC}	UGATE - PHASE = 2.5V		2.0		A
UGATE Sink Resistance (Note 7)	R _{UGPD}	250mA Sink Current		1.0	1.5	Ω
UGATE Sink Current (Note 7)	I _{UGSNK}	UGATE - PHASE = 2.5V		2.0		A
LGATE Pull-Up Resistance (Note 7)	R _{LGPU}	250mA Source Current		1.0	1.5	Ω
LGATE Source Current (Note 7)	I _{LGSRC}	LGATE - VSSP = 2.5V		2.0		A
LGATE Sink Resistance (Note 7)	R _{LGPD}	250mA Sink Current		0.5	0.9	Ω
LGATE Sink Current (Note 7)	I _{LGSNK}	LGATE - VSSP = 2.5V		4.0		A
UGATE to LGATE Deadtime	t _{UGFLGR}	UGATE falling to LGATE rising, no load		23		ns
LGATE to UGATE Deadtime	t _{LGUFGR}	LGATE falling to UGATE rising, no load		28		ns
BOOTSTRAP DIODE						
Forward Voltage	V _F	PVCC = 5V, I _F = 2mA		0.58		V
Reverse Leakage	I _R	V _R = 25V		0.2		μA
PROTECTION						
Overvoltage Threshold	OV _H	VSEN rising above setpoint for >1ms	150	195	240	mV
Severe Overvoltage Threshold	OV _{HS}	VSEN rising for >2μs	1.525	1.55	1.575	V
OC Threshold Offset at Rcomp = Open Circuit		3-phase configuration, ISUM- pin current	28.4	30.3	32.2	μA
		2-phase configuration, ISUM- pin current	18.3	20.2	22.1	μA
		1-phase configuration, ISUM- pin current	8.2	10.1	12.0	μA
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		9		mV
Undervoltage Threshold	UV _f	VSEN falling below setpoint for >1.2ms	-355	-295	-235	mV

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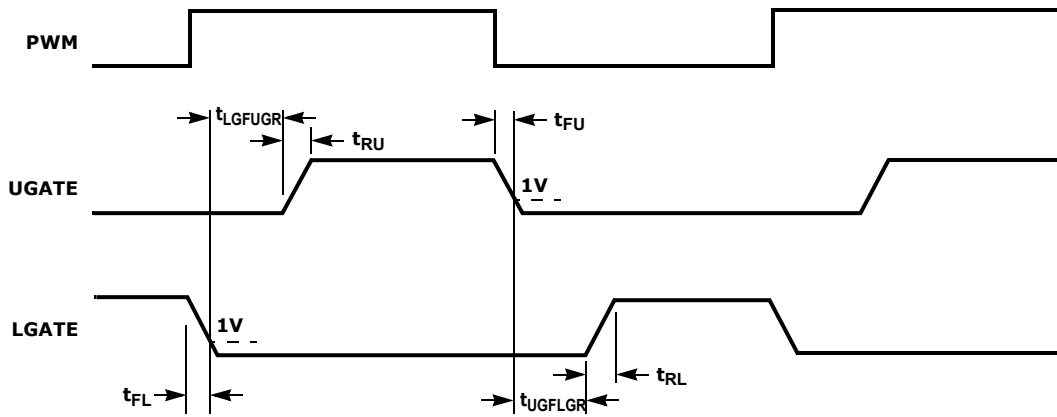
Electrical Specifications Operating Conditions: VDD = 5V, T_A = -40°C to +100°C, f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
LOGIC THRESHOLDS						
VR_ON Input Low	V _{IL}				0.3	V
VR_ON Input High	V _{IH}	ISL62883CHRTZ	0.7			V
	V _{IH}	ISL62883CIRTZ	0.75			V
VID0-VID6, PSI#, and DPRSLPVR Input Low	V _{IL}				0.3	V
VID0-VID6, PSI#, and DPRSLPVR Input High	V _{IH}		0.7			V
PWM						
PWM3 Output Low	V _{OL}	Sinking 5mA			1.0	V
PWM3 Output High	V _{OH}	Sourcing 5mA	3.5			V
PWM Tri-State Leakage		PWM = 2.5V		2		μA
THERMAL MONITOR						
NTC Source Current		NTC = 1.3V	53	60	67	μA
Over-Temperature Threshold		V (NTC) falling	1.18	1.2	1.22	V
VR_TT# Low Output Resistance	R _{TT}	I = 20mA		6.5	9	Ω
CLK_EN# OUTPUT LEVELS						
CLK_EN# Low Output Voltage	V _{OL}	I = 4mA		0.26	0.4	V
CLK_EN# Leakage Current	I _{OH}	CLK_EN# = 3.3V	-1		1	μA
CURRENT MONITOR						
IMON Output Current	I _{IMON}	ISUM- pin current = 20μA	114	120	126	μA
		ISUM- pin current = 10μA	54	60	66	μA
		ISUM- pin current = 5μA	25.5	30	34.5	μA
IMON Clamp Voltage	V _{IMONCLAMP}			1.1	1.15	V
Current Sinking Capability				275		μA
INPUTS						
VR_ON Leakage Current	I _{VR_ON}	VR_ON = 0V	-1	0		μA
		VR_ON = 1V		0	1	μA
VIDx Leakage Current	I _{VIDX}	VIDx = 0V	-1	0		μA
		VIDx = 1V		0.45	1	μA
PSI# Leakage Current	I _{PSI#}	PSI# = 0V	-1	0		μA
		PSI# = 1V		0.45	1	μA
DPRSLPVR Leakage Current	I _{DPRSLPVR}	DPRSLPVR = 0V	-1	0		μA
		DPRSLPVR = 1V		0.45	1	μA
SLEW RATE						
Slew Rate (For VID Change)	SR		5		6.5	mV/μs

NOTES:

- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Limits established by characterization and are not production tested.

Gate Driver Timing Diagram



Simplified Application Circuits

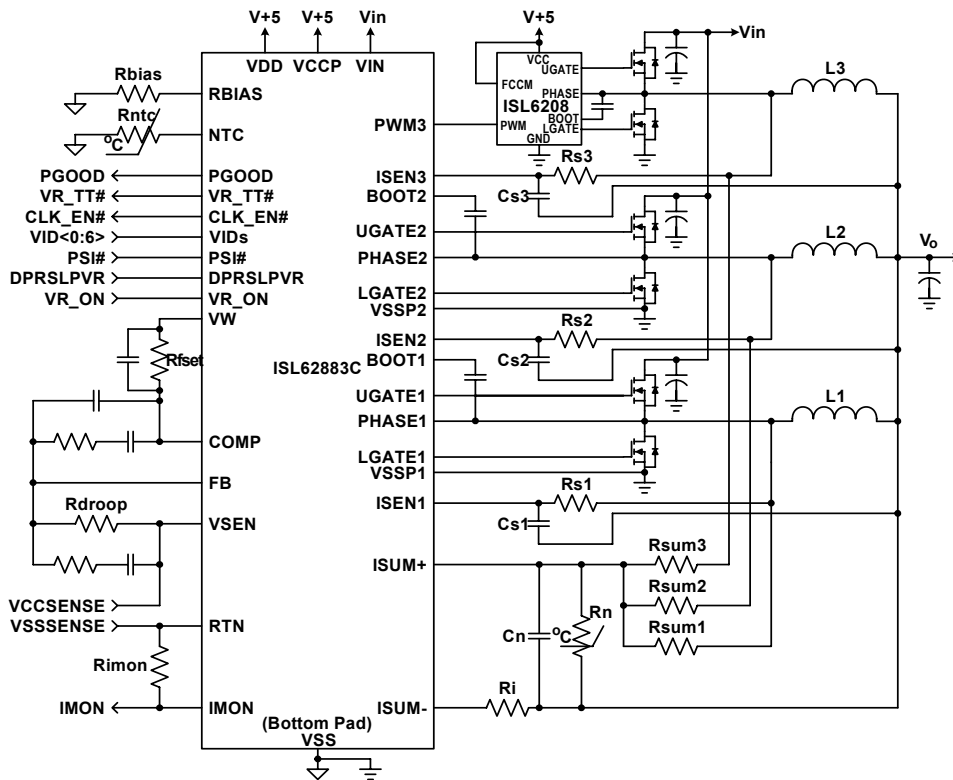


FIGURE 1. TYPICAL 3-PHASE APPLICATION CIRCUIT USING DCR SENSING

Simplified Application Circuits (Continued)

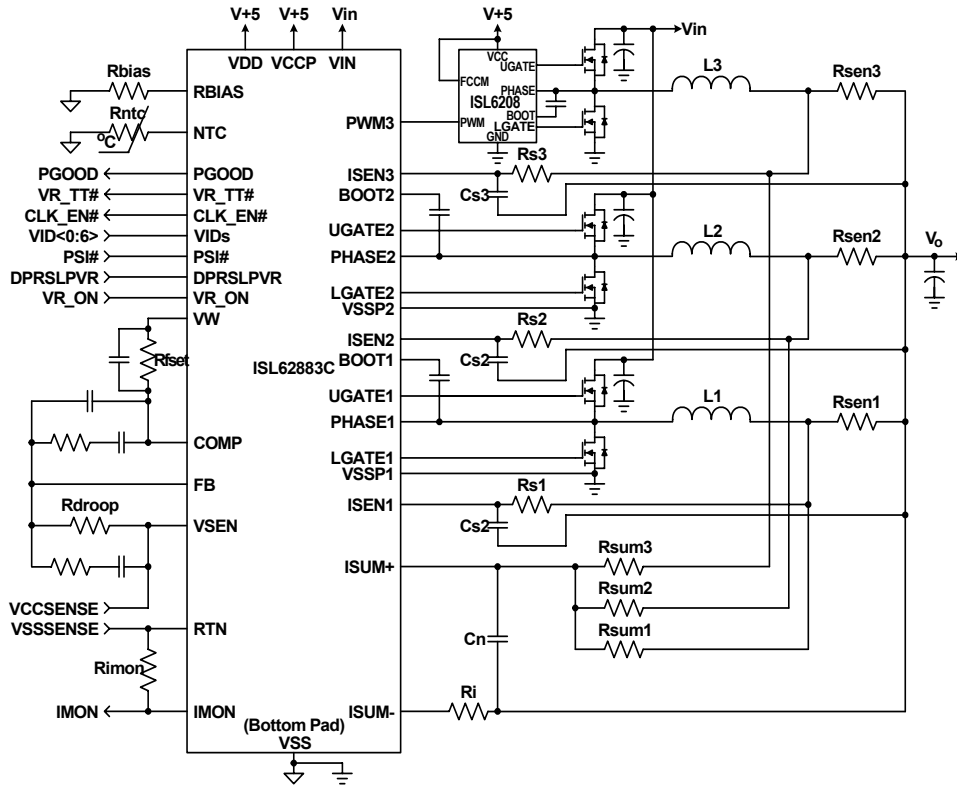


FIGURE 2. TYPICAL 3-PHASE APPLICATION CIRCUIT USING RESISTOR SENSING

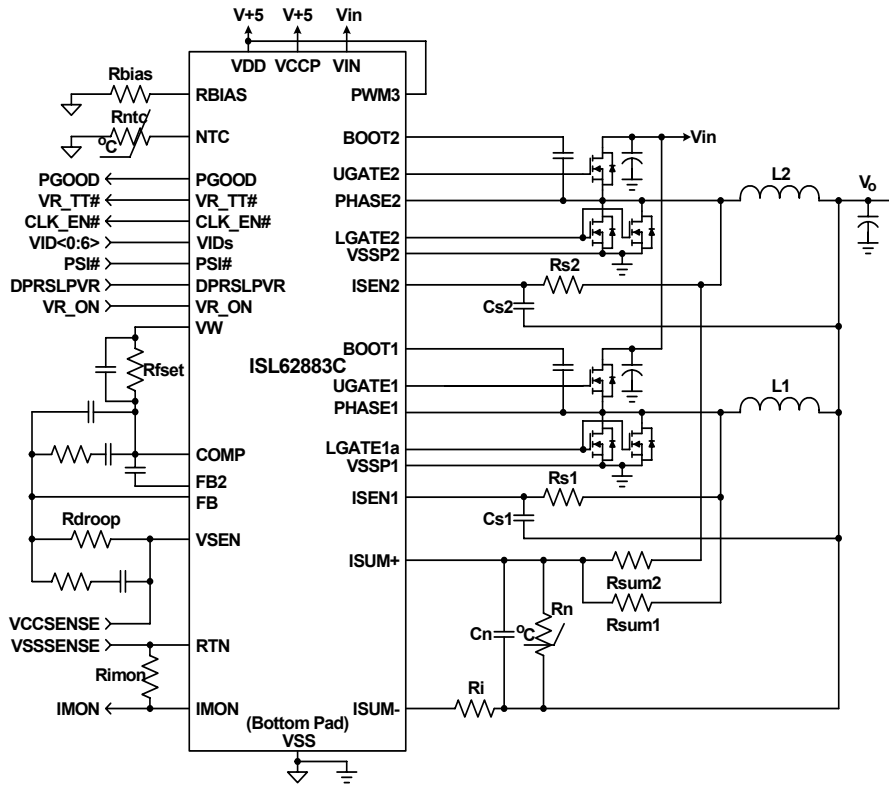


FIGURE 3. TYPICAL 2-PHASE APPLICATION CIRCUIT USING DCR SENSING

Simplified Application Circuits (Continued)

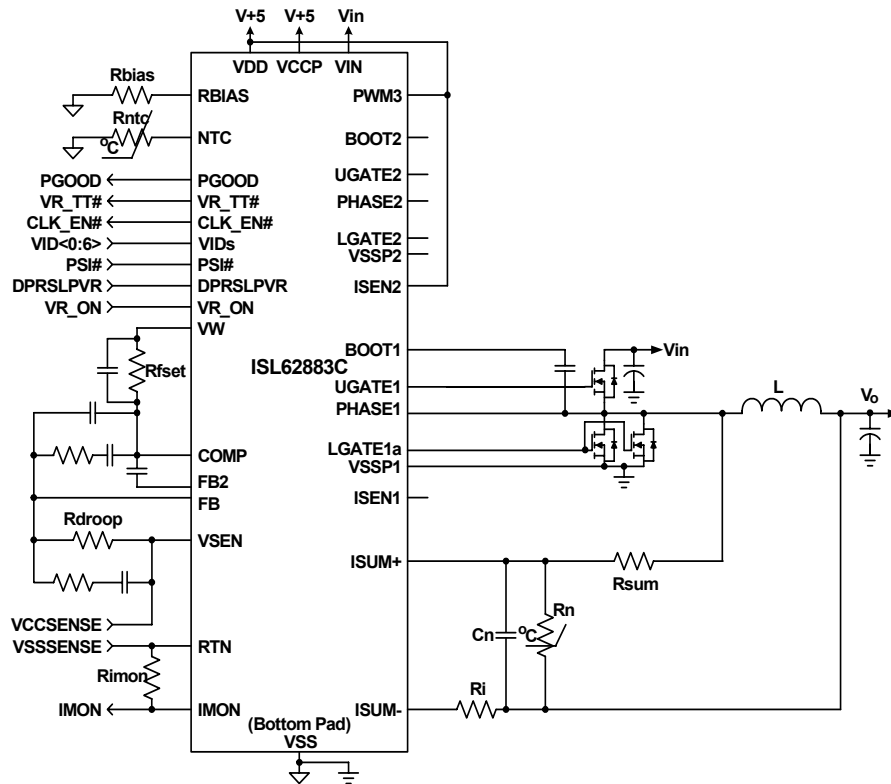


FIGURE 4. TYPICAL 1-PHASE APPLICATION CIRCUIT USING DCR SENSING

Theory of Operation

Multiphase R³™ Modulator

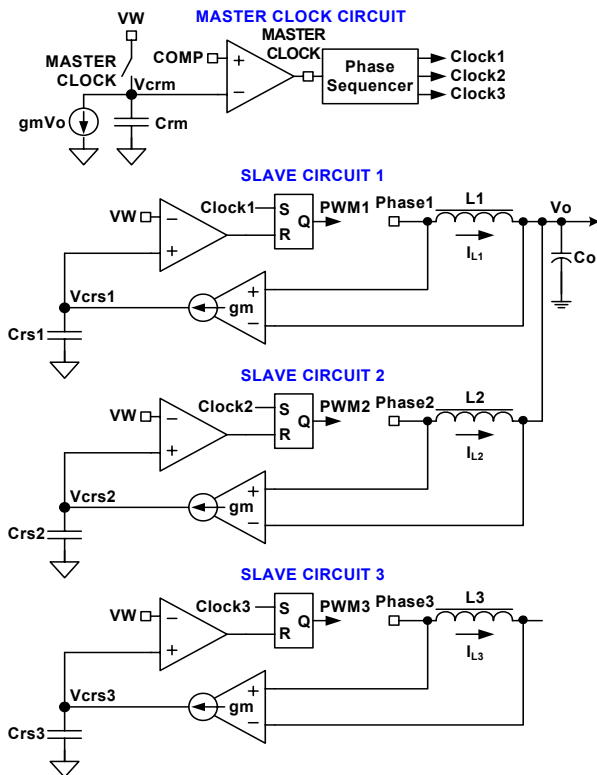


FIGURE 5. R³™ MODULATOR CIRCUIT

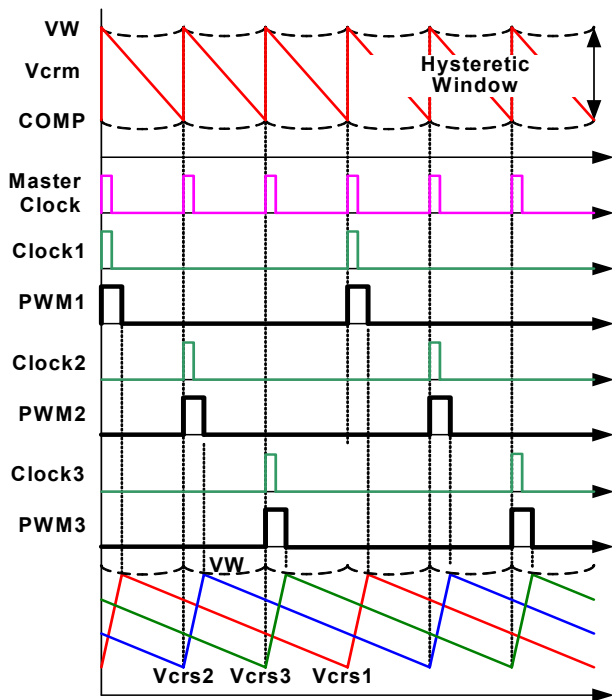


FIGURE 6. R³™ MODULATOR OPERATION PRINCIPLES IN STEADY STATE

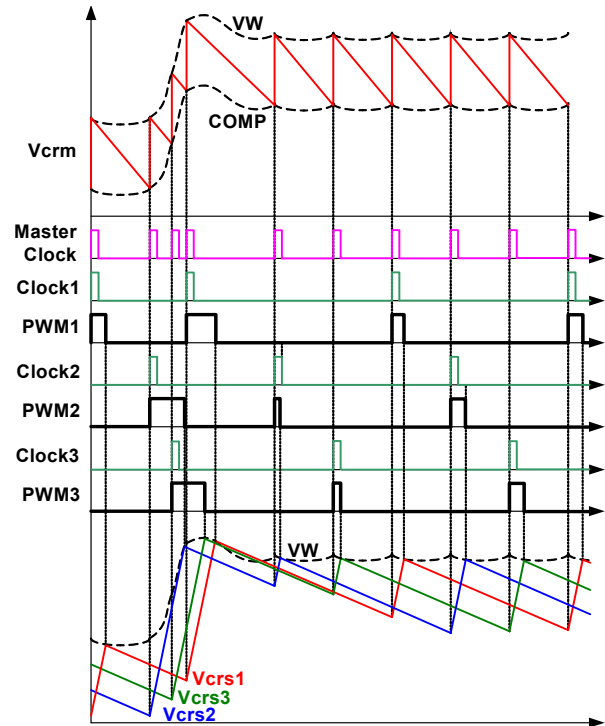


FIGURE 7. R³™ MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

The ISL62883C is a multiphase regulators implementing Intel™ IMVP-6.5™ protocol. It can be programmed for 1-, 2- or 3-phase operation. It uses Intersil patented R³™ (Robust Ripple Regulator™) modulator. The R³™ modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 5 conceptually shows the ISL62883C multiphase R³™ modulator circuit, and Figure 6 shows the operation principles.

A current source flows from the VW pin to the COMP pin, creating a voltage window set by the resistor between the two pins. This voltage window is called VW window in the following discussion.

Inside the IC, the modulator uses the master clock circuit to generate the clocks for the slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to $g_m V_o$, where g_m is a gain factor. C_{rm} voltage V_{crm} is a sawtooth waveform traversing between the VW and COMP voltages. It resets to VW when it hits COMP, and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits. If the ISL62883C is in 3-phase mode, the master clock signal will be distributed to the three phases, and the Clock1~3 signals will be 120° out-of-phase. If the ISL62883C is in 2-phase mode, the master clock signal will be distributed to Phases 1 and 2, and the Clock1 and Clock2 signals will be 180° out-of-phase. If the

ISL62883C is in 1-phase mode, the master clock signal will be distributed to Phases 1 only and be the Clock1 signal.

Each slave circuit has its own ripple capacitor C_{RS} , whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{RS} . The slave circuit turns on its PWM pulse upon receiving the clock signal, and the current source charges C_{RS} . When C_{RS} voltage V_{CRS} hits VW , the slave circuit turns off the PWM pulse, and the current source discharges C_{RS} .

Since the ISL62883C works with V_{CRS} , which are large-amplitude and noise-free synthesized signals, the ISL62883C achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the ISL62883C has an error amplifier that allows the controller to maintain a 0.5% output voltage accuracy.

Figure 7 shows the operation principles during load insertion response. The COMP voltage rises during load insertion, generating the master clock signal more quickly, so the PWM pulses turn on earlier, increasing the effective switching frequency, which allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls as the COMP voltage falls, reducing the current PWM pulse width. This kind of behavior gives the ISL62883C excellent response speed.

The fact that all the phases share the same VW window voltage also ensures excellent dynamic current balance among phases.

Diode Emulation and Period Stretching

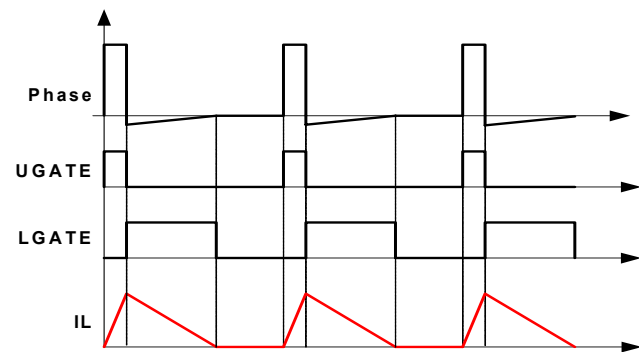


FIGURE 8. DIODE EMULATION

ISL62883C can operate in diode emulation (DE) mode to improve light load efficiency. In DE mode, the low-side MOSFET conducts when the current is flowing from source to drain and doesn't allow reverse current, emulating a diode. As Figure 8 shows, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The ISL62883C monitors the current through monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

If the load current is light enough, as Figure 8 shows, the inductor current will reach and stay at zero before the next phase node pulse, and the regulator is in discontinuous conduction mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A, and the regulator is in CCM although the controller is in DE mode.

Figure 9 shows the operation principle in diode emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, therefore is the same, making the inductor current triangle the same in the three cases. The ISL62883C clamps the ripple capacitor voltage V_{CRS} in DE mode to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{CRS} , naturally stretching the switching period. The inductor current triangles move further apart from each other such that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light load efficiency.

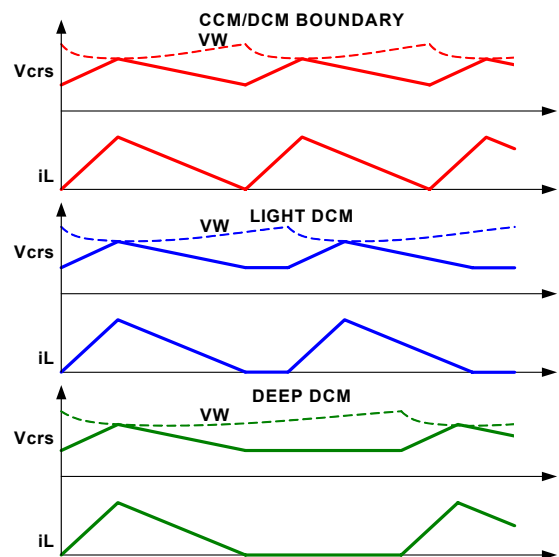


FIGURE 9. PERIOD STRETCHING

Start-up Timing

With the controller's V_{DD} voltage above the POR threshold, the start-up sequence begins when VR_ON exceeds the 1.1V logic high threshold. Figure 10 shows the typical start-up timing when the ISL62883C is configured for CPU VR application. The ISL62883C uses digital soft-start to ramp-up DAC to the boot voltage of 1.1V at about $2.5mV/\mu s$. Once the output voltage is within 10% of the boot voltage for 13 PWM cycles ($43\mu s$ for frequency = 300kHz), $CLK_EN\#$ is pulled low and DAC slews at $5mV/\mu s$ to the voltage set by the VID pins. PGOOD is asserted high in approximately 7ms. Similar results occur if VR_ON is tied to V_{DD} , with the soft-start sequence starting $120\mu s$ after V_{DD} crosses the POR threshold.

Figure 11 shows the typical start-up timing when the ISL62883C is configured for GPU VR application. The ISL62883C uses digital soft start to ramp up DAC to the voltage set by the VID pins. The slew rate is $5mV/\mu s$ when there is $DPRSLPVR = 0$, and is doubled when there is $DPRSLPVR = 1$. Once the output voltage is within 10% of the target voltage for 13 PWM cycles ($43\mu s$ for frequency = 300kHz), $CLK_EN\#$ is pulled low. PGOOD is asserted high in approximately 7ms. Similar results occur if VR_ON is tied to V_{DD} , with the soft-start sequence starting $120\mu s$ after V_{DD} crosses the POR threshold.

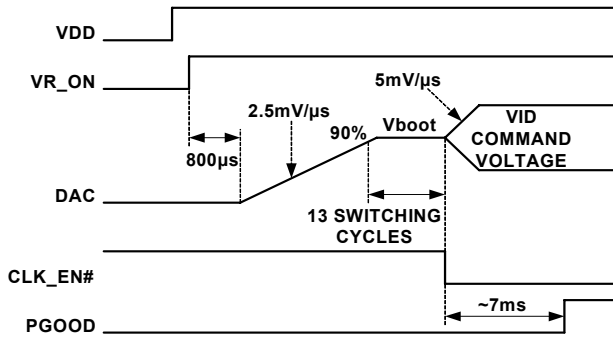


FIGURE 10. SOFT-START WAVEFORMS FOR CPU VR APPLICATION

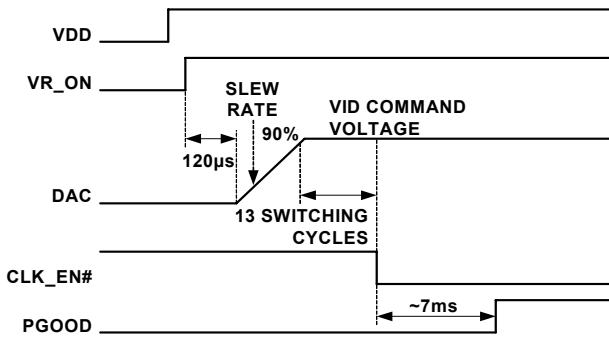


FIGURE 11. SOFT-START WAVEFORMS FOR GPU VR APPLICATION

Voltage Regulation and Load Line Implementation

After the start sequence, the ISL62883C regulates the output voltage to the value set by the VID inputs per Table 1. The ISL62883C will control the no-load output voltage to an accuracy of $\pm 0.5\%$ over the range of 0.75V to 1.5V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

TABLE 1. VID TABLE

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_o (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125

ISL62883C

TABLE 1. VID TABLE (Continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V _O (V)
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250

TABLE 1. VID TABLE (Continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V _O (V)
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375

TABLE 1. VID TABLE (Continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V _O (V)
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

load line implementation, current monitor and overcurrent protection.

Figure 12 shows the load line implementation. The ISL62883C drives a current source I_{droop} out of the FB pin, described by Equation 1.

$$I_{droop} = \frac{2xV_{Cn}}{R_i} \tag{EQ. 1}$$

When using inductor DCR current sensing, a single NTC element is used to compensate the positive temperature coefficient of the copper winding thus sustaining the load line accuracy with reduced cost.

I_{droop} flows through resistor R_{droop} and creates a voltage drop as shown in Equation 2.

$$V_{droop} = R_{droop} \times I_{droop} \tag{EQ. 2}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can both change the load line slope. Since I_{droop} also sets the overcurrent protection level, it is recommended to first scale I_{droop} based on OCP requirement, then select an appropriate R_{droop} value to obtain the desired load line slope.

Differential Sensing

Figure 12 also shows the differential voltage sensing scheme. V_{CCSENSE} and V_{VSSSENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the V_{VSSSENSE} voltage and add it to the DAC output. The error amplifier regulates the inverting and the non-inverting input voltages to be equal as shown in Equation 3:

$$V_{CCSENSE} + V_{droop} = V_{DAC} + V_{VSSSENSE} \tag{EQ. 3}$$

Rewriting Equation 3 and substitution of Equation 2 gives

$$V_{CCSENSE} - V_{VSSSENSE} = V_{DAC} - R_{droop} \times I_{droop} \tag{EQ. 4}$$

Equation 4 is the exact equation required for load line implementation.

The V_{CCSENSE} and V_{VSSSENSE} signals come from the processor die. The feedback will be open circuit in the absence of the processor. As Figure 12 shows, it is recommended to add a "catch" resistor to feed the VR local output voltage back to the compensator, and add another "catch" resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, will provide voltage feedback if the system is powered up without a processor installed.

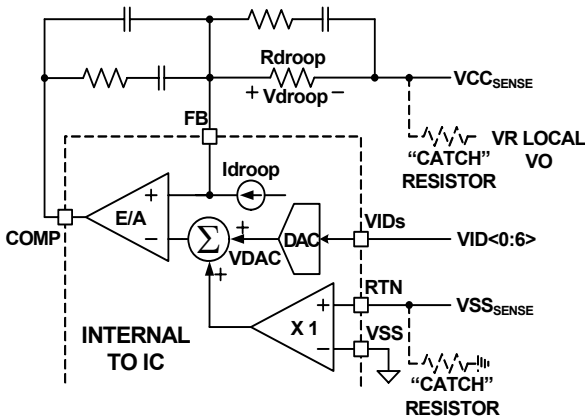


FIGURE 12. DIFFERENTIAL SENSING AND LOAD LINE IMPLEMENTATION

As the load current increases from zero, the output voltage will droop from the VID table value by an amount proportional to the load current to achieve the load line. The ISL62883C can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors as shown in Figure 1 on page 10 or through resistors in series with the inductors as shown in Figure 2 on page 11. In both methods, capacitor C_n voltage represents the inductor total currents. A droop amplifier converts C_n voltage into an internal current source with the gain set by resistor R_i. The current source is used for

Phase Current Balancing

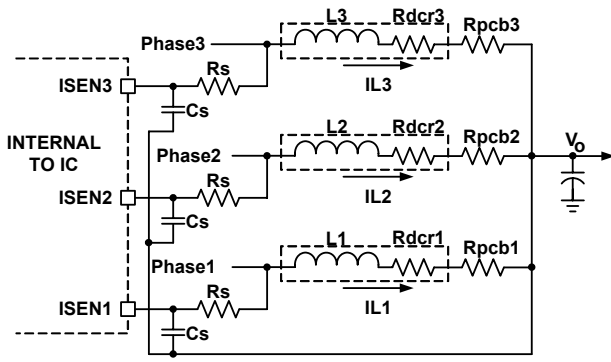


FIGURE 13. CURRENT BALANCING CIRCUIT

The ISL62883C monitors individual phase average current by monitoring the ISEN1, ISEN2, and ISEN3 voltages. Figure 13 shows the current balancing circuit recommended for ISL62883C. Each phase node voltage is averaged by a low-pass filter consisting of R_s and C_s , and presented to the corresponding ISEN pin. R_s should be routed to inductor phase-node pad in order to eliminate the effect of phase node parasitic PCB DCR. Equations 5 thru 7 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} \quad (EQ. 5)$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} \quad (EQ. 6)$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} \quad (EQ. 7)$$

where R_{dcr1} , R_{dcr2} and R_{dcr3} are inductor DCR; R_{pcb1} , R_{pcb2} and R_{pcb3} are parasitic PCB DCR between the inductor output side pad and the output voltage rail; and I_{L1} , I_{L2} and I_{L3} are inductor average currents.

The ISL62883C will adjust the phase pulse-width relative to the other phases to make

$V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus to achieve $I_{L1} = I_{L2} = I_{L3}$, when there are $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Using same components for L1, L2 and L3 will provide a good match of R_{dcr1} , R_{dcr2} and R_{dcr3} . Board layout will determine R_{pcb1} , R_{pcb2} and R_{pcb3} . It is recommended to have symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

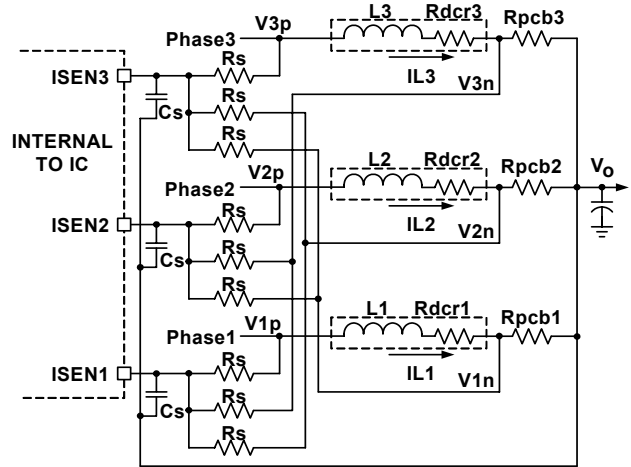


FIGURE 14. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Sometimes, it is difficult to implement symmetrical layout. For the circuit shown in Figure 13, asymmetric layout causes different R_{pcb1} , R_{pcb2} and R_{pcb3} thus current imbalance. Figure 14 shows a differential-sensing current balancing circuit recommended for ISL62883C. The current sensing traces should be routed to the inductor pads so they only pick up the inductor DCR voltage. Each ISEN pin sees the average voltage of three sources: its own phase inductor phase-node pad, and the other two phases inductor output side pads. Equations 8 thru 10 give the ISEN pin voltages:

$$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n} \quad (EQ. 8)$$

$$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n} \quad (EQ. 9)$$

$$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p} \quad (EQ. 10)$$

The ISL62883C will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$ as shown in Equations 11 and 12:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad (EQ. 11)$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad (EQ. 12)$$

Rewriting Equation 11 gives Equation 13:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad (EQ. 13)$$

and rewriting Equation 12 gives Equation 14:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad (EQ. 14)$$

Combining Equations 13 and 14 gives:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad (EQ. 15)$$

Therefore:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad (EQ. 16)$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) will be achieved when there is $R_{dcr1} = R_{dcr2} = R_{dcr3} \cdot R_{pcb1}$, R_{pcb2} and R_{pcb3} will not have any effect.

Since the slave ripple capacitor voltages mimic the inductor currents, R^3 ™ modulator can naturally achieve excellent current balancing during steady state and dynamic operations. Figure 15 shows current balancing performance of the ISL62883C evaluation board with load transient of 12A/51A at different rep rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at low rep rate, but cannot keep up when the rep rate gets into the hundred-kHz range, where it's out of the control loop bandwidth. The controller achieves excellent current balancing in all cases installed.

CCM Switching Frequency

The R_{fset} resistor between the COMP and the VW pins sets the sets the VW windows size, therefore sets the switching frequency. When the ISL62883C is in continuous conduction mode (CCM), the switching frequency is not absolutely constant due to the nature of the R^3 ™ modulator. As explained in the Multiphase R^3 ™ Modulator section, the effective switching frequency will increase during load insertion and will decrease during load release to achieve fast response. On the other hand, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 15% and doesn't have any significant effect on output voltage ripple magnitude. Equation 17 gives an estimate of the frequency-setting resistor R_{fset} value. $8k\Omega$ R_{fset} gives approximately 300kHz switching frequency. Lower resistance gives higher switching frequency.

$$R_{fset}(k\Omega) = (\text{Period}(\mu\text{s}) - 0.29) \times 2.65 \quad (\text{EQ. 17})$$

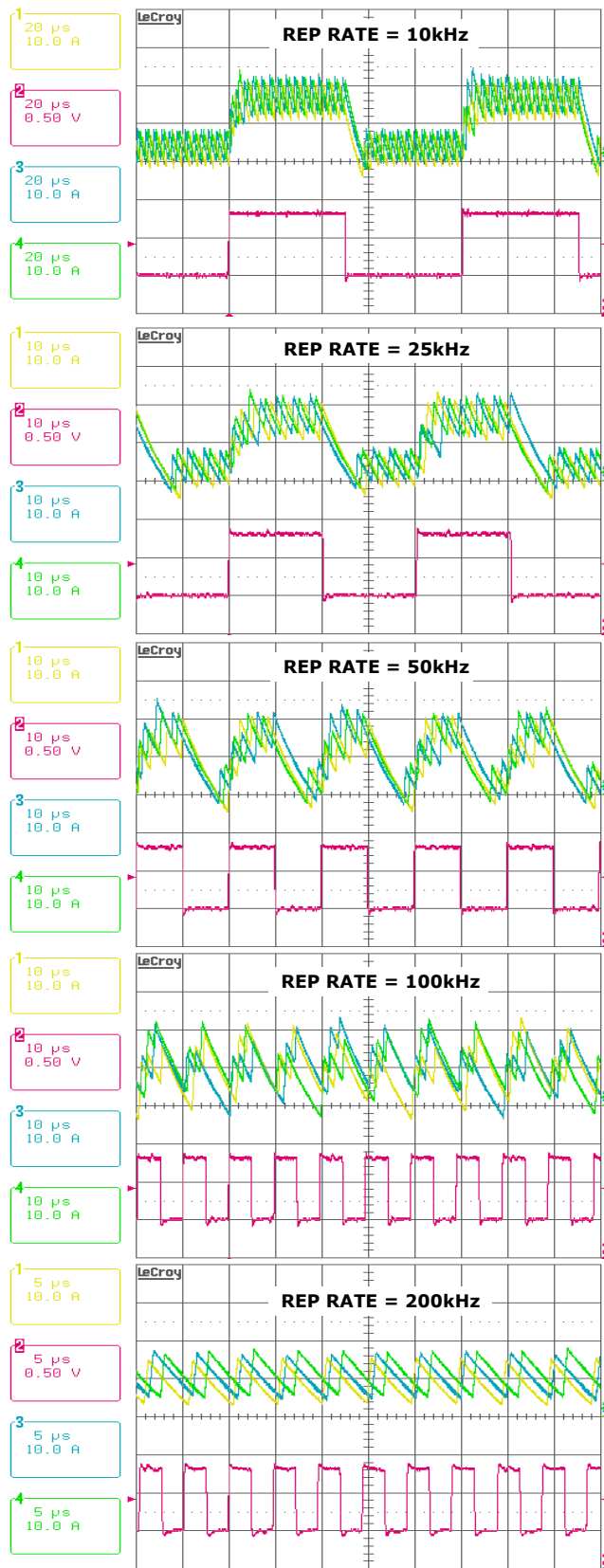


FIGURE 15. ISL62883 EVALUATION BOARD CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: I_{L1} , CH2: I_{LOAD} , CH3: I_{L2} , CH4: I_{L3}

Modes of Operation

TABLE 2. ISL62883C CONFIGURATIONS

PWM3	ISEN2	CLK_EN#	R _{BIAS} (kΩ)	CONFIG.	OVERSHOOT REDUCTION FUNCTION
To External Driver	To Power Stage	External pull-up	147	3-phase CPU VR	Disabled
			47		Enabled
		Tied to GND or floating	147	3-phase GPU VR	Disabled
			47		Enabled
Tied to 5V	External pull-up	147	2-phase CPU VR	Disabled	
				47	Enabled
		Tied to GND or floating	147	2-phase GPU VR	Disabled
			47		Enabled
	Tied to 5V	x	147	1-phase CPU	See Table 4
			47	1-phase GPU	

TABLE 3. ISL62883C MODES OF OPERATION

CONFIG.	PSI#	DPRSLPVR	OPERATIONAL MODE	SLEW RATE
3-phase CPU Config.	0	0	2-phase CCM	5mV/μs
	1	0	3-phase CCM	
	0	1	1-phase DE	
	1	1	1-phase DE	
3-phase GPU Config.	0	0	2-phase CCM	10mV/μs
	1	0	3-phase CCM	
	0	1	1-phase DE	
	1	1	1-phase DE	
2-phase CPU Config.	0	0	1-phase CCM	5mV/μs
	1	0	2-phase CCM	
	0	1	1-phase DE	
	1	1	1-phase DE	
2-phase GPU Config.	0	0	1-phase CCM	10mV/μs
	1	0	2-phase CCM	
	0	1	1-phase DE	
	1	1	1-phase DE	
1-phase CPU Config.	x	0	1-phase CCM	5mV/μs
		1	1-phase DE	
1-phase GPU Config.	x	0	1-phase CCM	10mV/μs
		1	1-phase DE	

The ISL62883C can be configured for 3, 2 or 1-phase operation.

For 2-phase configuration, tie the PWM3 pin to 5V. In this configuration, phases 1 and 2 are active. For 1-phase configuration, tie the ISEN2 pin to 5V. In this configuration, only phase-1 is active.

Table 2 shows the ISL62883C configurations, programmed by the PWM3 pin, the ISEN2 pin, the CLK_EN# pin status and the R_{BIAS} value.

When the ISL62883C is in 3- or 2-phase configuration, external pull-up on the CLK_EN# pin puts the ISL62883C in CPU VR configuration; Tying the CLK_EN# pin to GND or leaving it floating puts the ISL62883C in GPU VR configuration. In 3- or 2-phase configuration, R_{BIAS} = 147kΩ disables the overshoot reduction function and R_{BIAS} = 47kΩ enables it.

If the PWM3 pin and the ISEN2 pin are both tied to 5V, the ISL62883C is in 1-phase configuration. The CLK_EN# pin status has no effect. R_{BIAS} = 147kΩ puts the ISL62883C in CPU VR configuration and R_{BIAS} = 47kΩ puts the ISL62883C in GPU configuration. In 1-phase configuration, the enabling and disabling of the overshoot reduction function are programmed by the resistance from COMP to GND, as Table 4 shows.

Table 3 shows the ISL62883C operational modes, programmed by the logic status of the PSI# and the DPRSLPVR pins.

In 3-phase configuration, the ISL62883C enters 2-phase CCM for (PSI# = 0 and DPRSLPVR = 0). It drops phase 3 and operates phases 1 and 2 180° out-of-phase. It also reduces the overcurrent and the way-overcurrent protection levels to 2/3 of the initial values. The ISL62883C enters 1-phase DE mode for DPRSLPVR = 1 by dropping phase 2 and reduces the overcurrent and the way-overcurrent protection levels to 1/3 of the initial values.

In 2-phase configuration, the ISL62883C enters 1-phase CCM for (PSI# = 0 and DPRSLPVR = 0). It drops phase 2 and reduces the overcurrent and the way-overcurrent protection levels to 1/2 of the initial values. The ISL62883C enters 1-phase DE mode for DPRSLPVR = 1 by dropping phase 2 and reduces the overcurrent and the way-overcurrent protection levels to 1/3 of the initial values.

In 1-phase configuration, the ISL62883C does not change the operational mode when the PSI# signal changes status. It enters 1-phase DE mode when DLPRSLPVR = 1.

Dynamic Operation

When the ISL62883C is configured for CPU VR application, it responds to VID changes by slewing to the new voltage at 5mV/μs slew rate. As the output approaches the VID command voltage, the dv/dt moderates to prevent overshoot. Geyserville-III transitions commands one LSB VID step (12.5mV) every 2.5μs, controlling the effective dv/dt at 5mV/μs. The ISL62883C is capable of 5mV/μs slew rate.

When the ISL62883C is configured for GPU VR application, it responds to VID changes by slewing to the new voltage at a slew rate set by the logic status on the DPRSLPVR pin. The slew rate is 5mV/μs when DPRSLPVR=0 and is doubled when DPRSLPVR = 1.

When the ISL62883C is in DE mode, it will actively drive the output voltage up when the VID changes to a higher value. The DE mode operation will resume after reaching the new voltage level. If the load is light enough to warrant DCM, it will enter DCM after the inductor current has crossed zero for four consecutive cycles. The ISL62883C will remain in DE mode when the VID changes to a lower value. The output voltage will decay to the new value and the load will determine the slew rate. Overvoltage protection is blanked during VID down transition in DE mode until the output voltage is within 60mV of the VID value.

During load insertion response, the Fast Clock function increases the PWM pulse response speed. The ISL62883C monitors the VSEN pin voltage and compares it to 100ns-filtered version. When the unfiltered version is 20mV below the filtered version, the controller knows there is a fast voltage dip due to load insertion, hence issues an additional master clock signal to deliver a PWM pulse immediately.

The R³™ modulator intrinsically has voltage feed-forward. The output voltage is insensitive to a fast slew rate input voltage change.

Protections

The ISL62883C provides overcurrent, current-balance, undervoltage, overvoltage, and over-temperature protections.

The ISL62883C determines overcurrent protection (OCP) by comparing the average value of the droop current I_{droop} with an internal current source threshold. It declares OCP when I_{droop} is above the threshold for 120μs. A resistor R_{comp} from the COMP pin to GND programs the OCP current source threshold, as well as the overshoot reduction function in 1-phase configuration, as Table 4 shows. It is recommended to use the nominal R_{comp} value. The ISL62883C detects the R_{comp} value at the beginning of start-up, and sets the internal OCP threshold accordingly. It remembers the R_{comp} value until the VR_ON signal drops below the POR threshold.

TABLE 4. ISL62883C R_{comp} PROGRAMMABILITY

R_{comp}			3-PHASE CONFIG.	2-PHASE CONFIG.	1-PHASE CONFIG.	OVERSHOOT REDUCTION FUNCTION
MIN (kΩ)	NOM (kΩ)	MAX (kΩ)	OCP THRESHOLD (μA)			
	none	none	60	40	60	Disabled
320	400	480	68	45.3	68	
210	235	260	62	41.3	62	
155	165	175	54	36	54	Enabled
104	120	136	56	37.33	60	
78	85	92	58	38.7	68	
62	66	70	64	42.7	62	
45	50	55	66	44	54	

The default OCP threshold is the value when R_{comp} is not populated. It is recommended to scale the droop current I_{droop} such that the default OCP threshold gives approximately the desired OCP level, then use R_{comp} to fine tune the OCP level if necessary.

For overcurrent conditions above 2.5x the OCP level, the PWM outputs will immediately shut off and PGOOD will go low to maximize protection. This protection is also referred to as way-overcurrent protection or fast-overcurrent protection, for short-circuit protections.

The ISL62883C monitors the ISEN pin voltages to determine current-balance protection. If the ISEN pin voltage difference is greater than 9mV for 1ms, the controller will declare a fault and latch off.

The ISL62883C will declare undervoltage (UV) fault and latch off if the output voltage is less than the VID set value by 300mV or more for 1ms. It'll turn off the PWM outputs and de-assert PGOOD.

The ISL62883C has two levels of overvoltage protections. The first level of overvoltage protection is referred to as PGOOD overvoltage protection. If the output voltage exceeds the VID set value by +200mV for 1ms, the ISL62883C will declare a fault and de-assert PGOOD.

The ISL62883C takes the same actions for all of the above fault protections: de-assertion of PGOOD and turn-off of the high-side and low-side power MOSFETs. Any residual inductor current will decay through the MOSFET body diodes. These fault conditions can be reset by bringing VR_ON low or by bringing V_{DD} below the POR threshold. When VR_ON and V_{DD} return to their high operating levels, a soft-start will occur.

The second level of overvoltage protection is different. If the output voltage exceeds 1.55V, the ISL62883C will immediately declare an OV fault, de-assert PGOOD, and turn on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below 0.85V when all power MOSFETs are turned off. If the output voltage rises above 1.55V again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground. Resetting VR_ON cannot clear the 1.55V OVP. Only resetting V_{DD} will clear it. The 1.55V OVP is active all the time when the controller is enabled, even if one of the other faults have been declared. This ensures that the processor is protected against high-side power MOSFET leakage while the MOSFETs are commanded off.

The ISL62883C has a thermal throttling feature. If the voltage on the NTC pin goes below the 1.18V OT threshold, the VR_TT# pin is pulled low indicating the need for thermal throttling to the system. No other action is taken within the ISL62883C in response to NTC pin voltage.

Table 5 summarizes the fault protections.

TABLE 5. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	120µs	PWM tri-state, PGOOD latched low	VR_ON toggle or VDD toggle
Way-Overcurrent (2.5xOC)	<2µs	Low-side MOSFET on until $V_{core} < 0.85V$, then PWM tri-state, PGOOD latched low.	VDD toggle
Overvoltage +200mV	1ms		
Undervoltage -300mV			
Phase Current Unbalance			
Overvoltage 1.55V	Immediately		
Over-Temperature		1ms	N/A

Current Monitor

The ISL62883C provides the current monitor function. The IMON pin outputs a high-speed analog current source that is 3 times of the droop current flowing out of the FB pin. Thus Equation 18:

$$I_{IMON} = 3 \times I_{droop} \quad (EQ. 18)$$

As Figures 1 and 2 show, a resistor R_{imon} is connected to the IMON pin to convert the IMON pin current to voltage. A capacitor can be paralleled with R_{imon} to filter the voltage information. The IMVP-6.5™ specification requires that the IMON voltage information be referenced to VSS_{SENSE} .

The IMON pin voltage range is 0V to 1.1V. A clamp circuit prevents the IMON pin voltage from going above 1.1V.

FB2 Function

The FB2 function is only available when the ISL62883C is in 2-phase configuration.

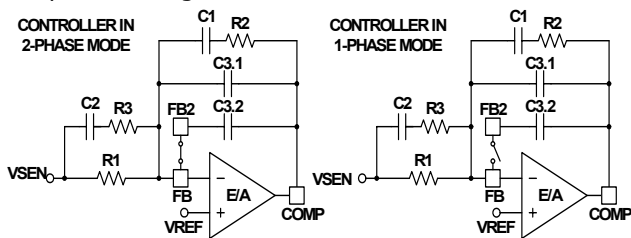


FIGURE 16. FB2 FUNCTION

Figure 16 shows the FB2 function. A switch (called FB2 switch) turns on to short the FB and the FB2 pins when the controller is in 2-phase mode. Capacitors C3.1 and C3.2 are in parallel, serving as part of the compensator. When the controller enters 1-phase mode, the FB2 switch turns off, removing C3.2 and leaving only C3.1 in

the compensator. The compensator gain will increase with the removal of C3.2. By properly sizing C3.1 and C3.2, the compensator can be optimal for both 2-phase mode and 1-phase mode.

When the FB2 switch is off, C3.2 is disconnected from the FB pin. However, the controller still actively drives the FB2 pin voltage to follow the FB pin voltage such that C3.2 voltage always follows C3.1 voltage. When the controller turns on the FB2 switch, C3.2 will be reconnected to the compensator smoothly.

The FB2 function ensures excellent transient response in both 2-phase mode and 1-phase mode. If one decides not to use the FB2 function, simply populate C3.1 only.

Adaptive Body Diode Conduction Time Reduction

In DCM, the controller turns off the low-side MOSFET when the inductor current approaches zero. During on-time of the low-side MOSFET, phase voltage is negative and the amount is the MOSFET $r_{DS(ON)}$ voltage drop, which is proportional to the inductor current. A phase comparator inside the controller monitors the phase voltage during on-time of the low-side MOSFET and compares it with a threshold to determine the zero-crossing point of the inductor current. If the inductor current has not reached zero when the low-side MOSFET turns off, it'll flow through the low-side MOSFET body diode, causing the phase node to have a larger voltage drop until it decays to zero. If the inductor current has crossed zero and reversed the direction when the low-side MOSFET turns off, it'll flow through the high-side MOSFET body diode, causing the phase node to have a spike until it decays to zero. The controller continues monitoring the phase voltage after turning off the low-side MOSFET and adjusts the phase comparator threshold voltage accordingly in iterative steps such that the low-side MOSFET body diode conducts for approximately 40ns to minimize the body diode-related loss.

Overshoot Reduction Function

The ISL62883C has an optional overshoot reduction function. Tables 2 and 4 show how to enable and disable it.

When a load release occurs, the energy stored in the inductors will dump to the output capacitor, causing output voltage overshoot. The inductor current freewheels through the low-side MOSFET during this period of time. The overshoot reduction function turns off the low-side MOSFET during the output voltage overshoot, forcing the inductor current to freewheel through the low-side MOSFET body diode. Since the body diode voltage drop is much higher than MOSFET $r_{DS(ON)}$ voltage drop, more energy is dissipated on the low-side MOSFET therefore the output voltage overshoot is lower.

If the overshoot reduction function is enabled, the ISL62883C monitors the COMP pin voltage to determine the output voltage overshoot condition. The COMP voltage will fall and hit the clamp voltage when the

output voltage overshoots. The ISL62883C will turn off LGATE1 and LGATE2 when COMP is being clamped. All the low-side MOSFETs in the power stage will be turned off. When the output voltage has reached its peak and starts to come down, the COMP voltage starts to rise and is no longer clamped. The ISL62883C will resume normal PWM operation.

When PSI# is low, indicating a low power state of the CPU, the controller will disable the overshoot reduction function as large magnitude transient event is not expected and overshoot is not a concern.

While the overshoot reduction function reduces the output voltage overshoot, energy is dissipated on the low-side MOSFET, causing additional power loss. The more frequent transient event, the more power loss dissipated on the low-side MOSFET. The MOSFET may face severe thermal stress when transient events happen at a high repetitive rate. User discretion is advised when this function is enabled.

Key Component Selection

RBIAS

The ISL62883C uses a resistor (1% or better tolerance is recommended) from the RBIAS pin to GND to establish highly accurate reference current sources inside the IC. Refer to Table 2 to select the resistance according to desired configuration. Do not connect any other components to this pin. Do not connect any capacitor to the RBIAS pin as it will create instability.

Care should be taken in layout that the resistor is placed very close to the RBIAS pin and that a good quality signal ground is connected to the opposite side of the RBIAS resistor.

Inductor DCR Current-Sensing Network

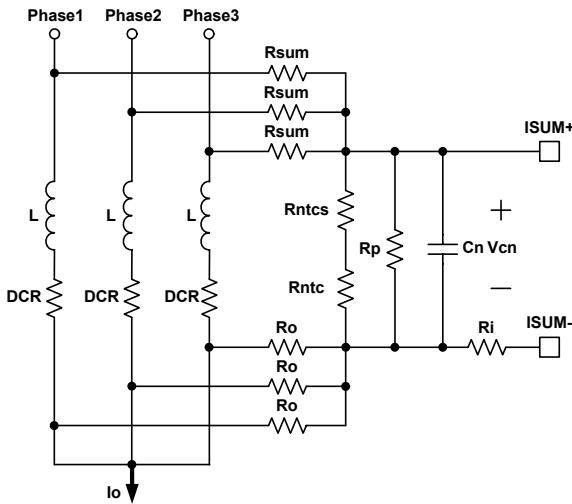


FIGURE 17. DCR CURRENT-SENSING NETWORK

Figure 17 shows the inductor DCR current-sensing network for a 3-phase solution. An inductor current flows through the DCR and creates a voltage drop. Each inductor has two resistors in R_{SUM} and R_O connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{SUM} and R_O resistors are connected in a summing network as shown, and feed the total current information to the NTC network (consisting of R_{ntcs} , R_{ntc} and R_p) and capacitor C_n . R_{ntc} is a negative temperature coefficient (NTC) thermistor, used to temperature-compensate the inductor DCR change.

The inductor output side pads are electrically shorted in the schematic, but have some parasitic impedance in actual board layout, which is why one cannot simply short them together for the current-sensing summing network. It is recommended to use 1W~10W R_O to create quality signals. Since R_O value is much smaller than the rest of the current sensing circuit, the following analysis will ignore it for simplicity.

The summed inductor current information is presented to the capacitor C_n . Equations 19 thru 23 describe the frequency-domain relationship between inductor total current $I_o(s)$ and C_n voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad (EQ. 19)$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad (EQ. 20)$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad (EQ. 21)$$

$$\omega_L = \frac{DCR}{L} \quad (EQ. 22)$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n} \quad (EQ. 23)$$

where N is the number of phases.

Transfer function $A_{CS}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, giving higher reading of the inductor DC current. The NTC R_{ntc} values decreases as its temperature decreases. Proper selections of R_{SUM} , R_{ntcs} , R_p and R_{ntc} parameters ensure that V_{Cn} represent the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. It is recommended to have a higher ratio of V_{cn} to the inductor DCR voltage, so the droop circuit has higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: $R_{sum} = 3.65k\Omega$, $R_p = 11k\Omega$, $R_{ntcs} = 2.61k\Omega$ and $R_{ntc} = 10k\Omega$ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. One can apply full load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is recommended to follow the Intersil evaluation board layout and current-sensing network parameters to minimize engineering time.

$V_{cn}(s)$ also needs to represent real-time $I_o(s)$ for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ has a pole w_{sns} and a zero w_L . One needs to match w_L and w_{sns} so $A_{cs}(s)$ is unity gain at all frequencies. By forcing w_L equal to w_{sns} and solving for the solution, Equation 24 gives C_n value.

$$C_n = \frac{L}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad (EQ. 24)$$

For example, given $N = 3$, $R_{sum} = 3.65k\Omega$, $R_p = 11k\Omega$, $R_{ntcs} = 2.61k\Omega$, $R_{ntc} = 10k\Omega$, $DCR = 0.88m\Omega$ and $L = 0.36\mu H$, Equation 24 gives $C_n = 0.406\mu F$.

Assuming the compensator design is correct, Figure 18 shows the expected load transient response waveforms if C_n is correctly selected. When the load current I_{core} has a square change, the output voltage V_{core} also has a square response.

If C_n value is too large or too small, $V_{cn}(s)$ will not accurately represent real-time $I_o(s)$ and will worsen the transient response. Figure 19 shows the load transient response when C_n is too small. V_{core} will sag excessively upon load insertion and may create a system failure. Figure 20 shows the transient response when C_n is too large. V_{core} is sluggish in drooping to its final value. There will be excessive overshoot if load insertion occurs during this time, which may potentially hurt the CPU reliability.

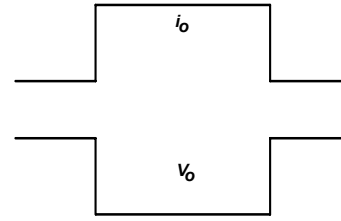


FIGURE 18. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

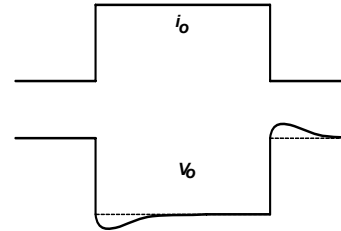


FIGURE 19. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

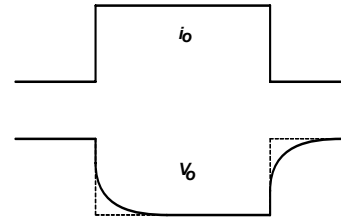


FIGURE 20. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

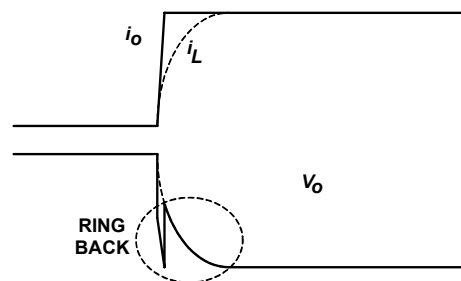


FIGURE 21. OUTPUT VOLTAGE RING BACK PROBLEM

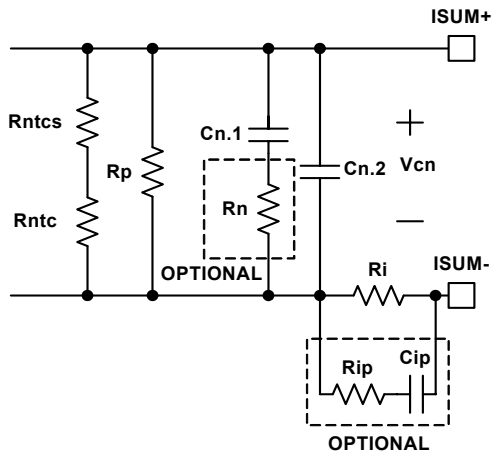


FIGURE 22. OPTIONAL CIRCUITS FOR RING BACK REDUCTION

Figure 21 shows the output voltage ring back problem during load transient response. The load current i_o has a fast step change, but the inductor current i_L cannot accurately follow. Instead, i_L responds in first order system fashion due to the nature of current loop. The ESR and ESL effect of the output capacitors makes the output voltage V_o dip quickly upon load current change. However, the controller regulates V_o according to the droop current i_{droop} , which is a real-time representation of i_L ; therefore it pulls V_o back to the level dictated by i_L , causing the ring back problem. This phenomenon is not observed when the output capacitor have very low ESR and ESL, such as all ceramic capacitors.

Figure 22 shows two optional circuits for reduction of the ring back.

C_n is the capacitor used to match the inductor time constant. It usually takes the parallel of two (or more) capacitors to get the desired value. Figure 22 shows that two capacitors $C_{n.1}$ and $C_{n.2}$ are in parallel. Resistor R_n is an optional component to reduce the V_o ring back. At steady state, $C_{n.1} + C_{n.2}$ provides the desired C_n capacitance. At the beginning of i_o change, the effective capacitance is less because R_n increases the impedance of the $C_{n.1}$ branch. As Figure 19 explains, V_o tends to dip when C_n is too small, and this effect will reduce the V_o ring back. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when R_n is bigger. However, the presence of R_n increases the ripple of the V_n signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. R_n value usually is a few ohms. $C_{n.1}$, $C_{n.2}$ and R_n values should be determined through tuning the load transient response waveforms on an actual board.

R_{ip} and C_{ip} form an R-C branch in parallel with R_i , providing a lower impedance path than R_i at the beginning of i_o change. R_{ip} and C_{ip} do not have any effect at steady state. Through proper selection of R_{ip} and C_{ip} values, i_{droop} can resemble i_o rather than i_L , and V_o will not ring back. The recommended value for R_{ip} is 100Ω. C_{ip} should be determined through tuning the load

transient response waveforms on an actual board. The recommended range for C_{ip} is 100pF~2000pF. However, it should be noted that the $R_{ip} - C_{ip}$ branch may distort the i_{droop} waveform. Instead of being triangular as the real inductor current, i_{droop} may have sharp spikes, which may adversely affect i_{droop} average value detection and therefore may affect OCP accuracy. User discretion is advised.

Resistor Current-Sensing Network

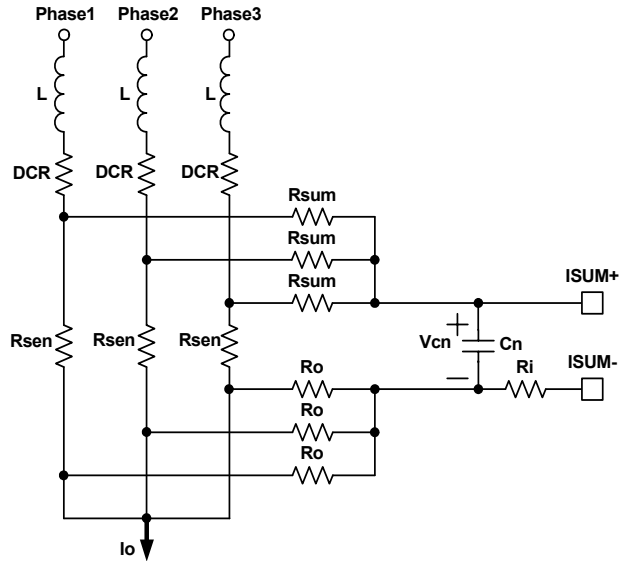


FIGURE 23. RESISTOR CURRENT-SENSING NETWORK

Figure 23 shows the resistor current-sensing network for a 2-phase solution. Each inductor has a series current-sensing resistor R_{sen} . R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n . R_{sum} and C_n form a a filter for noise attenuation. Equations 25 thru 27 give $V_{Cn}(s)$ expression

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{R_{sen}}(s) \tag{EQ25}$$

$$A_{R_{sen}}(s) = \frac{1}{1 + \frac{s}{\omega_{sns}}} \tag{EQ26}$$

$$\omega_{R_{sen}} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \tag{EQ27}$$

Transfer function $A_{R_{sen}}(s)$ always has unity gain at DC. Current-sensing resistor R_{sen} value will not have significant variation over-temperature, so there is no need for the NTC network.

The recommended values are $R_{sum} = 1k\Omega$ and $C_n = 5600pF$.

Overcurrent Protection

Refer to Equation 1 on page 17 and Figures 17, 21 and 23; resistor R_i sets the droop current I_{droop} . Table 4 on page 21 shows the internal OCP threshold. It is recommended to design I_{droop} without using the R_{comp} resistor.

For example, the OCP threshold is 60µA for 3-phase solution. We will design I_{droop} to be 40.9µA at full load, so the OCP trip level is 1.5x of the full load current.

For inductor DCR sensing, Equation 28 gives the DC relationship of $V_{Cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o \quad (EQ. 28)$$

Substitution of Equation 28 into Equation 1 gives Equation 29:

$$I_{droop} = \frac{2}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \quad (EQ29)$$

Therefore:

$$R_i = \frac{2R_{ntcnet} \times DCR \times I_o}{N \times \left(R_{ntcnet} + \frac{R_{sum}}{N} \right) \times I_{droop}} \quad (EQ30)$$

Substitution of Equation 20 and application of the OCP condition in Equation 30 gives Equation 31:

$$R_i = \frac{2 \times \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{N \times \left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + \frac{R_{sum}}{N} \right) \times I_{droopmax}} \quad (EQ31)$$

where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given $N = 3$, $R_{sum} = 3.65k\Omega$, $R_p = 11k\Omega$, $R_{ntcs} = 2.61k\Omega$, $R_{ntc} = 10k\Omega$, $DCR = 0.88m\Omega$, $I_{omax} = 51A$ and $I_{droopmax} = 40.9\mu A$, Equation 31 gives $R_i = 606\Omega$.

For resistor sensing, Equation 32 gives the DC relationship of $V_{Cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \frac{R_{sen}}{N} \times I_o \quad (EQ32)$$

Substitution of Equation 32 into Equation 1 gives Equation 33:

$$I_{droop} = \frac{2}{R_i} \times \frac{R_{sen}}{N} \times I_o \quad (EQ33)$$

Therefore

$$R_i = \frac{2R_{sen} \times I_o}{N \times I_{droop}} \quad (EQ34)$$

Substitution of Equation 34 and application of the OCP condition in Equation 30 gives Equation 35:

$$R_i = \frac{2R_{sen} \times I_{omax}}{N \times I_{droopmax}} \quad (EQ35)$$

where I_{omax} is the full load current, $I_{droopmax}$ is the corresponding droop current. For example, given $N = 3$, $R_{sen} = 1m\Omega$, $I_{omax} = 51A$ and $I_{droopmax} = 40.9\mu A$, Equation 35 gives $R_i = 831\Omega$.

A resistor from COMP to GND can adjust the internal OCP threshold, providing another dimension of fine-tune

flexibility. Table 4 shows the detail. It is recommended to scale I_{droop} such that the default OCP threshold gives approximately the desired OCP level, then use R_{comp} to fine tune the OCP level if necessary.

Load Line Slope

Refer to Figure 12.

For inductor DCR sensing, substitution of Equation 29 into Equation 2 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \quad (EQ36)$$

For resistor sensing, substitution of Equation 33 into Equation 2 gives the load line slope expression:

$$LL = \frac{V_{droop}}{I_o} = \frac{2R_{sen} \times R_{droop}}{N \times R_i} \quad (EQ37)$$

Substitution of Equation 30 and rewriting Equation 36, or substitution of Equation 34 and rewriting Equation 37 give the same result in Equation 38:

$$R_{droop} = \frac{I_o}{I_{droop}} \times LL \quad (EQ. 38)$$

One can use the full load condition to calculate R_{droop} . For example, given $I_{omax} = 51A$, $I_{droopmax} = 40.9\mu A$ and $LL = 1.9m\Omega$, Equation 38 gives $R_{droop} = 2.37k\Omega$.

It is recommended to start with the R_{droop} value calculated by Equation 38, and fine tune it on the actual board to get accurate load line slope. One should record the output voltage readings at no load and at full load for load line slope calculation. Reading the output voltage at lighter load instead of full load will increase the measurement error.

Current Monitor

Refer to Equation 18 for the IMON pin current expression.

Refer to Figures 1 and 2, the IMON pin current flows through R_{imon} . The voltage across R_{imon} is expressed in Equation 39:

$$V_{Rimon} = 3 \times I_{droop} \times R_{imon} \quad (EQ39)$$

Rewriting Equation 38 gives Equation 40:

$$I_{droop} = \frac{I_o}{R_{droop}} \times LL \quad (EQ40)$$

Substitution of Equation 40 into Equation 39 gives Equation 41:

$$V_{Rimon} = \frac{3I_o \times LL}{R_{droop}} \times R_{imon} \quad (EQ41)$$

Rewriting Equation 41 and application of full load condition gives Equation 42:

$$R_{imon} = \frac{V_{Rimon} \times R_{droop}}{3I_o \times LL} \quad (EQ42)$$

For example, given $LL = 1.9m\Omega$, $R_{droop} = 2.37k\Omega$, $V_{Rimon} = 999mV$ at $I_{omax} = 51A$, Equation 42 gives $R_{imon} = 8.14k\Omega$.

A capacitor C_{imon} can be paralleled with R_{imon} to filter the IMON pin voltage. The $R_{imon}C_{imon}$ time constant is the user's choice. It is recommended to have a time constant long enough such that switching frequency ripples are removed.

Compensator

Figure 18 shows the desired load transient response waveforms. Figure 24 shows the equivalent circuit of a voltage regulator (VR) with the droop function. A VR is equivalent to a voltage source ($= V_{ID}$) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope LL, i.e. constant output impedance, in the entire frequency range, V_o will have square response when I_o has a square change.

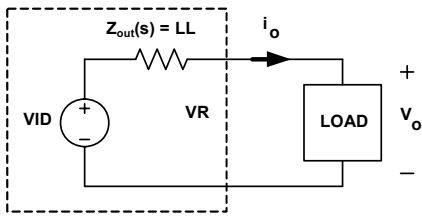


FIGURE 24. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

Intersil provides a Microsoft Excel-based spreadsheet to help design the compensator and the current sensing network, so the VR achieves constant output impedance as a stable system. Figure 27 shows a screenshot of the spreadsheet.

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, $T1(s)$ and $T2(s)$, that describe the entire system. Figure 25 conceptually shows $T1(s)$ measurement set-up and Figure 26 conceptually shows $T2(s)$ measurement set-up. The VR senses the inductor current, multiplies it by a gain of the load line slope, then adds it on top of the sensed output voltage and feeds it to the compensator. $T(1)$ is measured after the summing node, and $T2(s)$ is measured in the voltage loop before the summing node. The spreadsheet gives both $T1(s)$ and $T2(s)$ plots. However, only $T2(s)$ can be actually measured on an ISL62883C regulator.

$T1(s)$ is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than $T2(s)$ and has more meaning of system stability.

$T2(s)$ is the voltage loop gain with closed droop loop. It has more meaning of output voltage response.

Design the compensator to get stable $T1(s)$ and $T2(s)$ with sufficient phase margin, and output impedance equal or smaller than the load line slope.

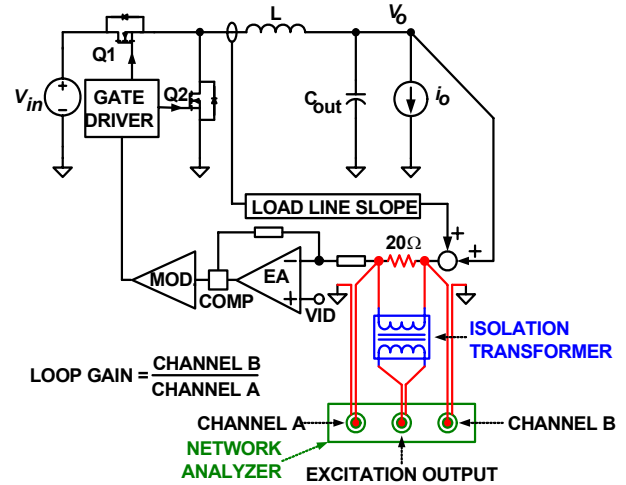


FIGURE 25. LOOP GAIN $T1(s)$ MEASUREMENT SET-UP

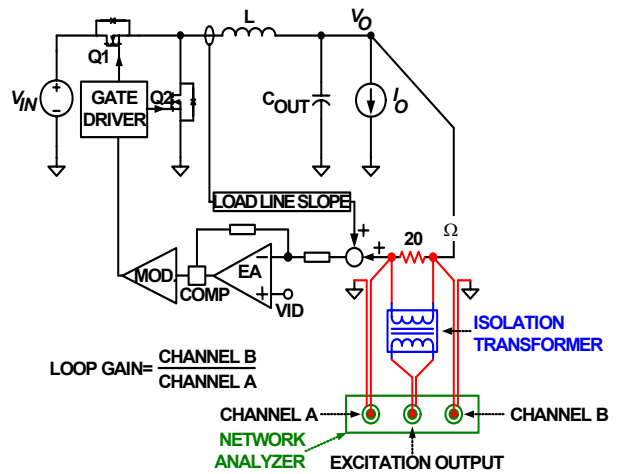


FIGURE 26. LOOP GAIN $T2(s)$ MEASUREMENT SET-UP

Compensation & Current Sensing Network Design for Intersil Multiphase R² Regulators for IMVP-6.5

Jia Wei, jwei@intersil.com, 919-405-3605

Attention: 1. "Analysis ToolPak" Add-in is required. To turn on, go to Tools--Add-Ins, and check "Analysis ToolPak".

2. Green cells require user input

Operation Parameters	
Controller Part Number:	ISL6288x
Phase Number:	2
Vin:	12 volts
Vo:	1.15 volts
Full Load Current:	50 Amps
Estimated Full-Load Efficiency:	87 %
Number of Output Bulk Capacitors:	3
Capacitance of Each Output Bulk Capacitor:	470 uF
ESR of Each Output Bulk Capacitor:	4.5 mΩ
ESL of Each Output Bulk Capacitor:	0.6 nH
Number of Output Ceramic Capacitors:	30
Capacitance of Each Output Ceramic Capacitor:	10 uF
ESR of Each Output Ceramic Capacitor:	3 mΩ
ESL of Each Output Ceramic Capacitor:	3 nH
Switching Frequency:	300 kHz
Inductance Per Phase:	0.36 uH
CPU Socket Resistance:	0.9 mΩ
Desired Load-Line Slope:	1.9 mΩ
Desired ISUM- Pin Current at Full Load:	33.1 uA
(This sets the over-current protection level)	

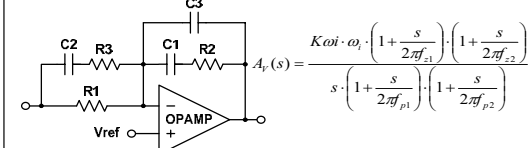
Changing the settings in red requires deep understanding of control loop design

Place the 2nd compensator pole fp2 at: 1.9 xfs (Switching Frequency)

Tune Kwi to get the desired loop gain bandwidth

Tune the compensator gain factor Kwi: 1.15
(Recommended Kwi range is 0.8~2)

Compensator Parameters



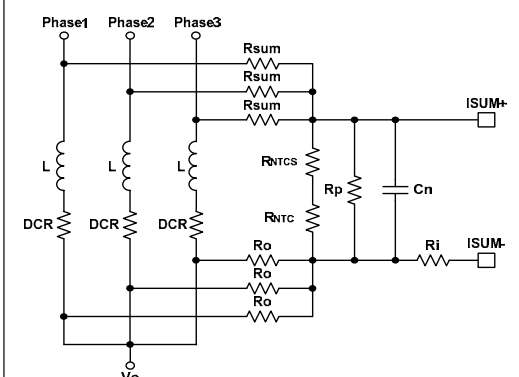
Recommended Value	User-Selected Value
R1: 2.870 kΩ	R1: 2.87 kΩ
R2: 387.248 kΩ	R2: 412 kΩ
R3: 0.560 kΩ	R3: 0.562 kΩ
C1: 188.980 pF	C1: 150 pF
C2: 498.514 pF	C2: 390 pF
C3: 32.245 pF	C3: 32 pF

Use User-Selected Value (Y/N)? N

Performance and Stability

T1 Bandwidth: 190kHz	T2 Bandwidth: 52kHz
T1 Phase Margin: 63.4°	T2 Phase Margin: 94.7°

Current Sensing Network Parameters



Operation Parameters

Inductor DCR	0.88 mΩ
Rsum	3.65 kΩ
Rntc	10 kΩ
Rntcs	2.61 kΩ
Rp	11 kΩ

Recommended Value	User Selected Value
Cn: 0.294 uF	Cn: 0.294 uF
Ri: 1014.245 Ω	Ri: 1000 Ω

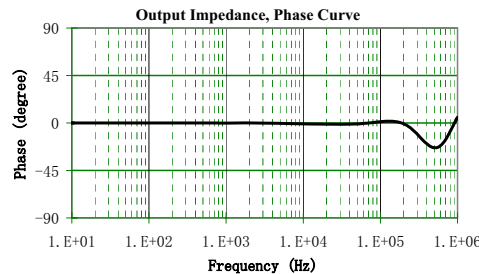
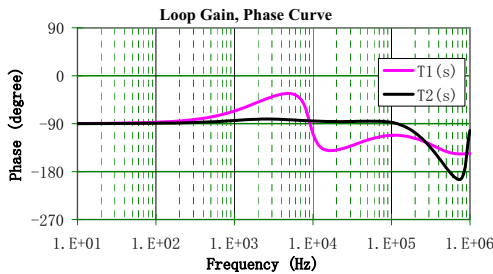
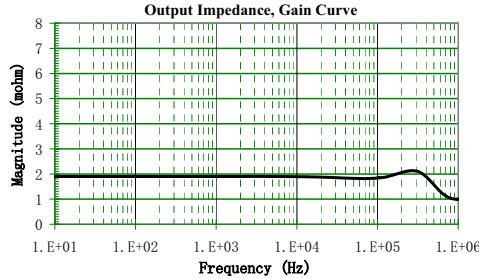
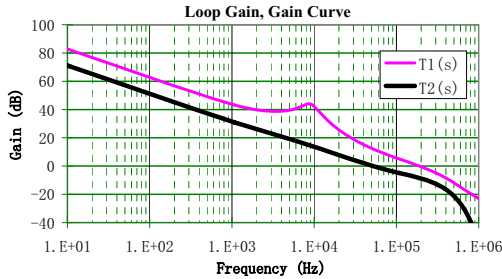


FIGURE 27. SCREENSHOT OF THE COMPENSATOR DESIGN SPREADSHEET

Optional Slew Rate Compensation Circuit For 1-Tick VID Transition

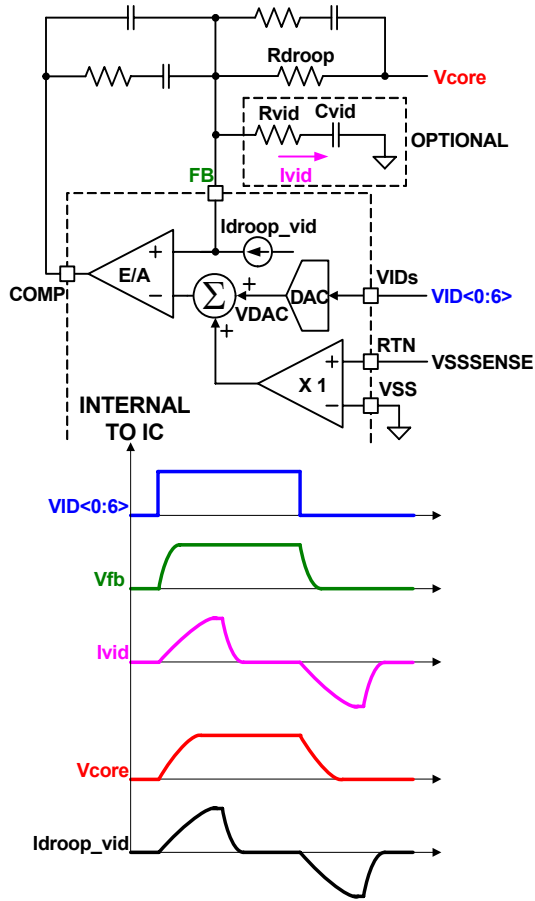


FIGURE 28. OPTIONAL SLEW RATE COMPENSATION CIRCUIT FOR 1-TICK VID TRANSITION

During a large VID transition, the DAC steps through the VIDs at a controlled slew rate. For example, the DAC may change a tick (12.5mV) per 2.5µs per, controlling output voltage V_{core} slew rate at 5mV/µs.

Figure 28 shows the waveforms of 1-tick VID transition. During 1-tick VID transition, the DAC output changes at approximately 15mV/µs slew rate, but the DAC cannot step through multiple VIDs to control the slew rate. Instead, the control loop response speed determines V_{core} slew rate. Ideally, V_{core} will follow the FB pin voltage slew rate. However, the controller senses the inductor current increase during the up transition, as the I_{droop_vid} waveform shows, and will droop the output voltage V_{core} accordingly, making V_{core} slew rate slow. Similar behavior occurs during the down transition.

To control V_{core} slew rate during 1-tick VID transition, one can add the R_{vid}-C_{vid} branch, whose current I_{vid} cancels I_{droop_vid}.

When V_{core} increases, the time domain expression of the induced I_{droop} change is

$$I_{droop}(t) = \frac{C_{out} \times LL}{R_{droop}} \times \frac{dV_{core}}{dt} \times \left(1 - e^{-\frac{t}{C_{out} \times LL}} \right) \quad (EQ43)$$

where C_{out} is the total output capacitance.

In the mean time, the R_{vid}-C_{vid} branch current I_{vid} time domain expression is:

$$I_{vid}(t) = C_{vid} \times \frac{dV_{fb}}{dt} \times \left(1 - e^{-\frac{t}{R_{vid} \times C_{vid}}} \right) \quad (EQ44)$$

It is desired to let I_{vid}(t) cancel I_{droop_vid}(t). So there are:

$$C_{vid} \times \frac{dV_{fb}}{dt} = \frac{C_{out} \times LL}{R_{droop}} \times \frac{dV_{core}}{dt} \quad (EQ45)$$

and:

$$R_{vid} \times C_{vid} = C_{out} \times LL \quad (EQ46)$$

The result is expressed in Equation 47:

$$R_{vid} = R_{droop} \quad (EQ47)$$

and:

$$C_{vid} = \frac{C_{out} \times LL}{R_{droop}} \times \frac{dV_{core}}{dt} \times \frac{dV_{fb}}{dt} \quad (EQ48)$$

For example: given LL = 1.9mΩ, R_{droop} = 2.37kΩ, C_{out} = 1320µF, dV_{core}/dt = 5mV/µs and dV_{fb}/dt = 15mV/µs, Equation 47 gives R_{vid} = 2.37kΩ and Equation 48 gives C_{vid} = 350pF.

It's recommended to select the calculated R_{vid} value and start with the calculated C_{vid} value and tweak it on the actual board to get the best performance.

During normal transient response, the FB pin voltage is held constant, therefore is virtual ground in small signal sense. The R_{vid} - C_{vid} network is between the virtual ground and the real ground, and hence has no effect on transient response.

Voltage Regulator Thermal Throttling

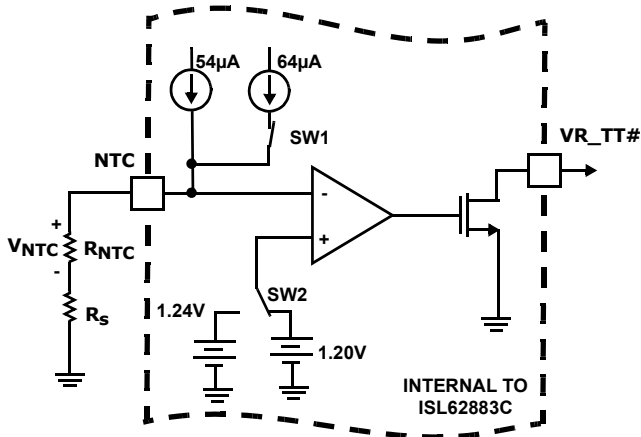


FIGURE 29. CIRCUITRY ASSOCIATED WITH THE THERMAL THROTTLING FEATURE

Figure 29 shows the thermal throttling feature with hysteresis. An NTC network is connected between the NTC pin and GND. At low temperature, SW1 is on and SW2 connects to the 1.20V side. The total current flowing out of the NTC pin is 60µA. The voltage on NTC pin is higher than threshold voltage of 1.20V and the comparator output is low. VR_TT# is pulled up by the external resistor.

When temperature increases, the NTC thermistor resistance decreases so the NTC pin voltage drops. When the NTC pin voltage drops below 1.20V, the comparator changes polarity and turns SW1 off and throws SW2 to 1.24V. This pulls VR_TT# low and sends the signal to start thermal throttle. There is a 6µA current reduction on NTC pin and 40mV voltage increase on threshold voltage of the comparator in this state. The VR_TT# signal will be used to change the CPU operation and decrease the power consumption. When the temperature drops down, the NTC thermistor voltage will go up. If NTC voltage increases to above 1.24V, the comparator will flip back. The external resistance difference in these two conditions is shown in Equation 49:

$$\frac{1.24V}{54\mu A} - \frac{1.20V}{60\mu A} = 2.96k \quad (EQ. 49)$$

One needs to properly select the NTC thermistor value such that the required temperature hysteresis correlates to 2.96kΩ resistance change. A regular resistor may need to be in series with the NTC thermistor to meet the threshold voltage values.

For example, given Panasonic NTC thermistor with B = 4700, the resistance will drop to 0.03322 of its nominal at +105°C, and drop to 0.03956 of its nominal at +100°C. If the required temperature hysteresis is +105°C to +100°C, the required resistance of NTC will be as shown in Equation 50:

$$\frac{2.96k\Omega}{(0.03956 - 0.03322)} = 467k\Omega \quad (EQ. 50)$$

Therefore, a larger value thermistor such as 470k NTC should be used.

At +105°C, 470kΩ NTC resistance becomes (0.03322 × 470kΩ) = 15.6kΩ. With 60µA on the NTC pin, the voltage is only (15.6kΩ × 60µA) = 0.937V. This value is much lower than the threshold voltage of 1.20V. Therefore, a regular resistor needs to be in series with the NTC. The required resistance can be calculated by Equation 51:

$$\frac{1.20V}{60\mu A} - 15.6k\Omega = 4.4k\Omega \quad (EQ. 51)$$

4.42k is a standard resistor value. Therefore, the NTC branch should have a 470k NTC and 4.42k resistor in series. The part number for the NTC thermistor is ERTJ0EV474J. It is a 0402 package. NTC thermistor will be placed in the hot spot of the board.

Current Balancing

Refer to Figures 1 and 2. The ISL62883C achieves current balancing through matching the ISEN pin voltages. R_S and C_S form filters to remove the switching ripple of the phase node voltages. It is recommended to use rather long R_SC_S time constant such that the ISEN voltages have minimal ripple and represent the DC current flowing through the inductors. Recommended values are R_S = 10kΩ and C_S = 0.22µF.

Layout Guidelines

Table 6 shows the layout considerations. The designators refer to the reference design shown in Figure 31.

TABLE 6. LAYOUT CONSIDERATION

PIN	NAME	LAYOUT CONSIDERATION
EP	GND	Create analog ground plane underneath the controller and the analog signal processing components. Don't let the power ground plane overlap with the analog ground plane. Avoid noisy planes/traces (e.g.: phase node) from crossing over/overlapping with the analog plane.
1	PGOOD	No special consideration
2	PSI#	No special consideration
3	RBIAS	Place the R _{BIAS} resistor (R16) in general proximity of the controller. Low impedance connection to the analog ground plane.
4	VR_TT#	No special consideration
5	NTC	The NTC thermistor (R9) needs to be placed close to the thermal source that is monitor to determine thermal throttling. Usually it's placed close to phase-1 high-side MOSFET.
6	VW	Place the capacitor (C4) across VW and COMP in close proximity of the controller
7	COMP	Place the compensator components (C3, C5, C6 R7, R11, R10 and C11) in general proximity of the controller.
8	FB	

TABLE 6. LAYOUT CONSIDERATION (Continued)

PIN	NAME	LAYOUT CONSIDERATION
9	ISEN3/FB2	For ISEN3 function, capacitor C7 decouples it to VSUM-, then through capacitor C20 to GND. Keep the decoupling path short and minimize the loop impedance. For FB2 function, a capacitor connects this pin to the COMP pin. Put the capacitor in general proximity of the controller.
10	ISEN2	Capacitor C9 decouples it to VSUM-, then through capacitor C20 to GND. Keep the decoupling path short and minimize the loop impedance.
11	ISEN1	Capacitor C10 decouples it to VSUM-, then through capacitor C20 to GND. Keep the decoupling path short and minimize the loop impedance.
12	VSEN	Place the VSEN/RTN filter (C12, C13) in close proximity of the controller for good decoupling.
13	RTN	
14	ISUM-	Place the current sensing circuit in general proximity of the controller. Place C82 very close to the controller. Place NTC thermistors R42 next to phase-1 inductor (L1) so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of VSUM+ and VSUM- signals to the controller. Run these two signals traces in parallel fashion with decent width (>20mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. Route R63 and R71 to the phase-1 side pad of inductor L1. Route R88 to the output side pad of inductor L1. Route R65 and R72 to the phase-2 side pad of inductor L2. Route R90 to the output side pad of inductor L2. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current sensing traces.
15	ISUM+	
16	VDD	A capacitor (C16) decouples it to GND. Place it in close proximity of the controller.
17	VIN	A capacitor (C17) decouples it to GND. Place it in close proximity of the controller.

TABLE 6. LAYOUT CONSIDERATION (Continued)

PIN	NAME	LAYOUT CONSIDERATION
18	IMON	Place the filter capacitor (C21) close to the CPU.
19	BOOT1	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
20	UGATE1	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE1 trace to the phase-1 high-side MOSFET (Q2 and Q8) source pins instead of general phase-1 node copper.
21	PHASE1	
22	VSSP1	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing VSSP1 to the phase-1 low-side MOSFET (Q3 and Q9) source pins instead of general power ground plane for better performance.
23	LGATE1	
24	PWM3	No special consideration.
25	VCCP	A capacitor (C22) decouples it to GND. Place it in close proximity of the controller.
26	LGATE2	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing VSSP2 to the phase-2 low-side MOSFET (Q5 and Q1) source pins instead of general power ground plane for better performance.
27	VSSP2	
28	PHASE2	Run these two traces in parallel fashion with decent width (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing PHASE2 trace to the phase-2 high-side MOSFET (Q4 and Q10) source pins instead of general phase-2 node copper.
29	UGATE2	
30	BOOT2	Use decent wide trace (>30mil). Avoid any sensitive analog signal trace from crossing over or getting close.
31~37	VID0~6	No special consideration.
38	VR_ON	No special consideration.
39	DPRSLPVR	No special consideration.
40	CLK_EN#	No special consideration.
Other	Phase Node	Minimize phase node copper area. Don't let the phase node copper overlap with/getting close to other sensitive traces. Cut the power ground plane to avoid overlapping with phase node copper.
Other		Minimize the loop consisting of input capacitor, high-side MOSFETs and low-side MOSFETs (e.g.: C27, C33, Q2, Q8, Q3 and Q9).

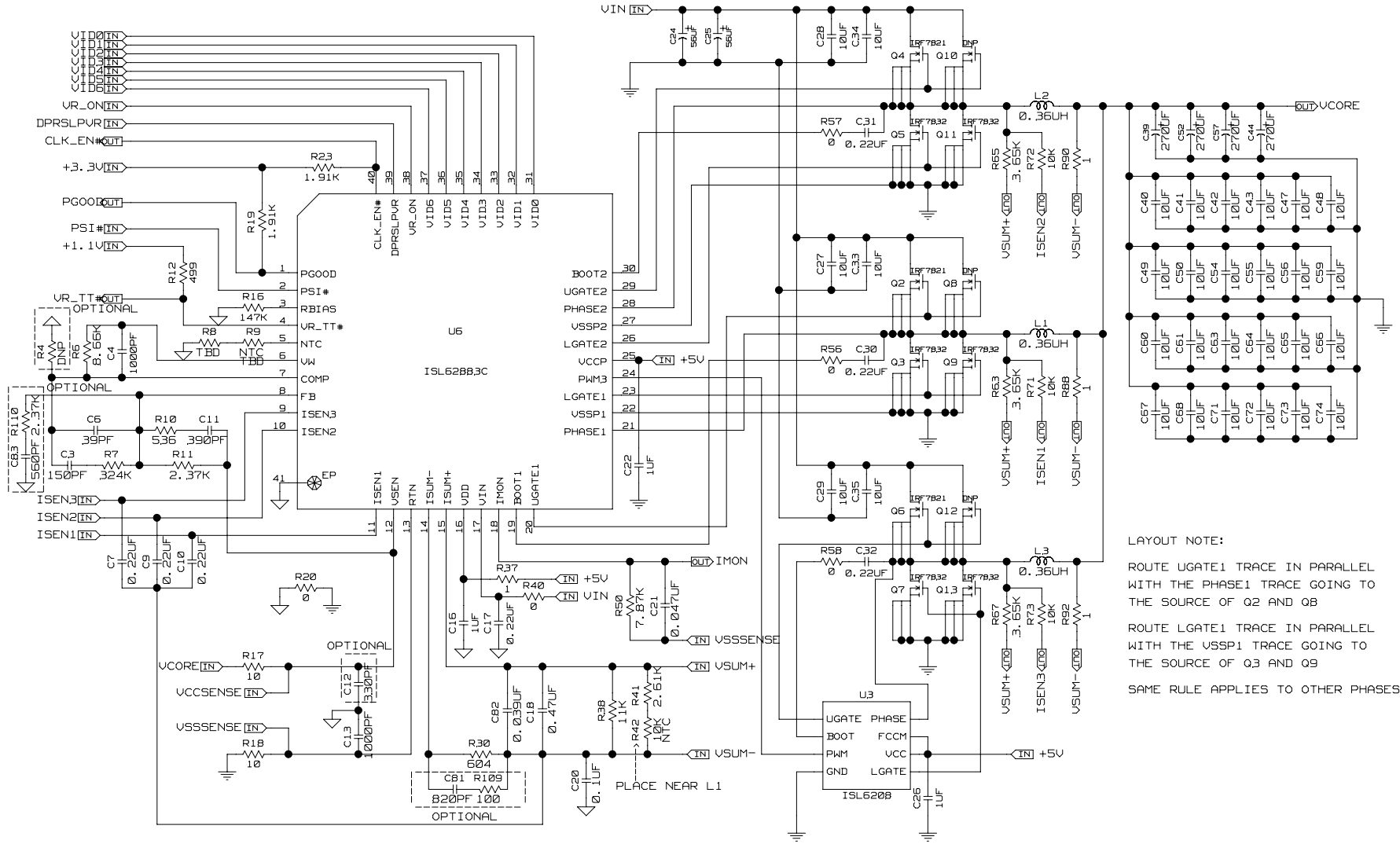


FIGURE 30. 3-PHASE CPU APPLICATION REFERENCE DESIGN

LAYOUT NOTE:
 ROUTE UGATE1 TRACE IN PARALLEL WITH THE PHASE1 TRACE GOING TO THE SOURCE OF Q2 AND Q8
 ROUTE LGATE1 TRACE IN PARALLEL WITH THE VSSP1 TRACE GOING TO THE SOURCE OF Q3 AND Q9
 SAME RULE APPLIES TO OTHER PHASES

ISL62883C

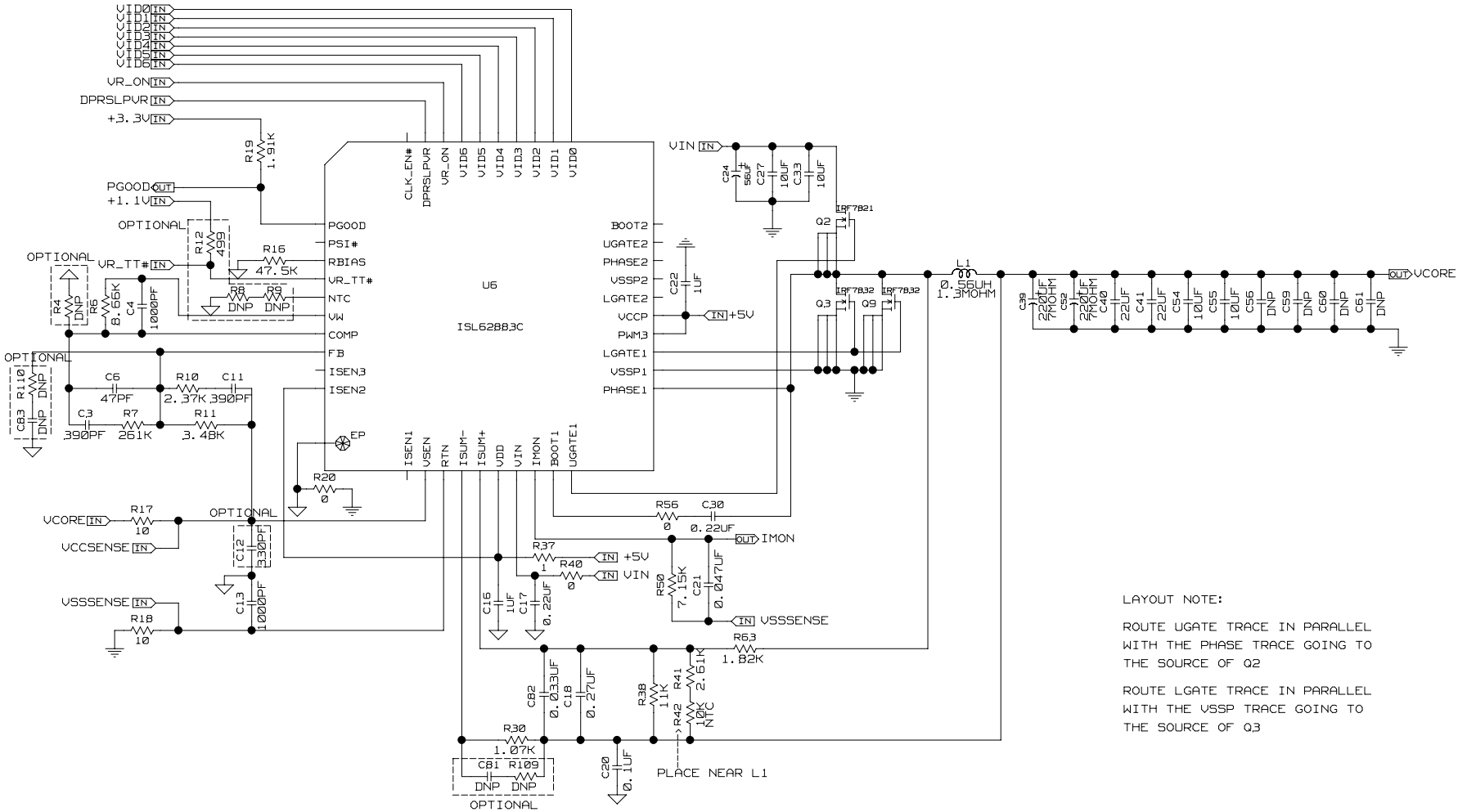


FIGURE 31. 1-PHASE GPU APPLICATION REFERENCE DESIGN

LAYOUT NOTE:
 ROUTE UGATE TRACE IN PARALLEL WITH THE PHASE TRACE GOING TO THE SOURCE OF Q2
 ROUTE LGATE TRACE IN PARALLEL WITH THE VSSP TRACE GOING TO THE SOURCE OF Q3

1-PHASE GPU Application Reference Design Bill of Materials

QTY	REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER	PACKAGE
1	C11	390pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00391-16V10	SM0603
1	C12	330pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00331-16V10	SM0603
1	C13	1000pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00102-16V10	SM0603
0	C15	DNP				
2	C16, C22	1μF	Multilayer Cap, 16V, 20%	GENERIC	H1045-00105-16V20	SM0603
2	C17, C30	0.22μF	Multilayer Cap, 25V, 10%	GENERIC	H1045-00224-25V10	SM0603
1	C18	0.27μF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00274-16V10	SM0603
1	C20	0.1μF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00104-16V10	SM0603
1	C21	0.047μF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00473-16V10	SM0603
1	C24	56μF	Radial SP Series Cap, 25V, 20%	SANYO	25SP56M	CASE-CC
2	C27,C33	10μF	Multilayer Cap, 25V, 20%	GENERIC	H1065-00106-25V20	SM1206
1	C3	390pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00391-16V10	SM0603
2	C39, C52	220μF	SPCAP, 2V, 7MΩ	PANASONIC	EEXSX0D221E7	
1	C4	1000pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00102-16V10	SM0603
2	C40, C41	22μF	Multilayer Cap, 6.3V, 20%	TAIYO MURATA Kyocera TDK	JMK212BJ226MG-T GRM21BC80J226M CM21X5R226M04AT C2012X5R0J226MT009N	SM0805
2	C54, C55	10μF	Multilayer Cap, 6.3V, 20%	TAIYO MURATA Kyocera TDK	JMK212BJ106MG-T GRM21BR60J106ME19 CM21X5R106M06AT C2012X5R0J106MT009N	SM0805
1	C6	47pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00470-16V10	SM0603
1	C82	0.033μF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00333-16V10	SM0603
0	C56, C59-C61, C81, C83	DNP				
1	L1	0.56μH	Inductor, Inductance 20%, DCR 7%	PANASONIC	ETQP4LR56AFC	10mmx10mm
1	Q2		N-Channel Power MOSFET	IR	IRF7821	PWRPAKS08
2	Q3, Q9		N-Channel Power MOSFET	IR	IRF7832	PWRPAKS08
1	R10	2.37k	Thick Film Chip Resistor, 1%	GENERIC	H2511-02371-1/16W1	SM0603
1	R11	3.48k	Thick Film Chip Resistor, 1%	GENERIC	H2511-03481-1/16W1	SM0603
1	R16	47.5k	Thick Film Chip Resistor, 1%	GENERIC	H2511-04752-1/16W1	SM0603
2	R17, R18	10	Thick Film Chip Resistor, 1%	GENERIC	H2511-00100-1/16W1	SM0603
1	R19	1.91k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01911-1/16W1	SM0603
0	R26	DNP				
3	R20, R40, R56	0	Thick Film Chip Resistor, 1%	GENERIC	H2511-00R00-1/16W1	SM0603
1	R30	1.07k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01071-1/16W1	SM0603
1	R37	1	Thick Film Chip Resistor, 1%	GENERIC	H2511-01R00-1/16W1	SM0603
1	R38	11k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01102-1/16W1	SM0603
1	R41	2.61k	Thick Film Chip Resistor, 1%	GENERIC	H2511-02611-1/16W1	SM0603
1	R42	10k NTC	Thermistor, 10k NTC	PANASONIC	ERT-J1VR103J	SM0603
1	R50	7.15k	Thick Film Chip Resistor, 1%	GENERIC	H2511-07151-1/16W1	SM0603

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1-PHASE GPU Application Reference Design Bill of Materials (Continued)

QTY	REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER	PACKAGE
1	R6	8.66k	Thick Film Chip Resistor, 1%	GENERIC	H2511-08661-1/16W1	SM0603
1	R63	1.82k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01821-1/16W1	SM0805
1	R7	261k	Thick Film Chip Resistor, 1%	GENERIC	H2511-02613-1/16W1	SM0603
0	R109, R110, R4, R8, R9	DNP				
1	U6		IMVP-6.5 PWM Controller	INTERSIL	ISL62883CHRTZ	QFN-40

2-PHASE CPU Application Reference Design Bill of Materials

QTY	REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER	PACKAGE
1	C11	390pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00391-16V10	SM0603
1	C12	330pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00331-16V10	SM0603
1	C13	1000pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00102-16V10	SM0603
1	C15	0.01μF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00103-16V10	SM0603
3	C16, C22, C26	1μF	Multilayer Cap, 16V, 20%	GENERIC	H1045-00105-16V20	SM0603
1	C18	0.47μF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00474-16V10	SM0603
1	C20	0.1μF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00104-16V10	SM0603
8	C21, C7, C9, C10, C17, C30, C31, C32	0.22μF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00224-16V10	SM0603
2	C24, C25	56μF	Radial SP Series Cap, 25V, 20%	SANYO	25SP56M	CASE-CC
6	C27, C28, C29, C33, C34, C35	10μF	Multilayer Cap, 25V, 20%	GENERIC	H1065-00106-25V20	SM1206
1	C3	150pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00151-16V10	SM0603
4	C39, C44, C52, C57	270μF	SPCAP, 2V, 4MΩ POLYMER CAP, 2.5V, 4.5MΩ	PANASONIC KEMET	EEXSX0D471E4 T520V277M2R5A(1)E4R 5-6666	
1	C4	1000pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00102-16V10	SM0603
24	C40-C43, C47-C50, C53-C56, C59-C69, C78	10μF	Multilayer Cap, 6.3V, 20%	TAIYO MURATA Kyocera TDK	JMK212BJ106MG-T GRM21BR60J106ME19 CM21X5R106M06AT C2012X5R0J106MT009N	SM0805
1	C6	39pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00390-16V10	SM0603
1	C81	820pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00821-16V10	SM0603
1	C82	0.039μF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00393-16V10	SM0603
1	C83	560pF	Multilayer Cap, 16V, 10%	GENERIC	H1045-00561-16V10	SM0603
3	L1, L2, L3	0.36μH	Inductor, Inductance 20%, DCR 5%	NEC-TOKIN PANASONIC	MPCH1040LR36 ETQP4LR36AFC	10mmx10mm
3	Q2, Q4, Q6		N-Channel Power MOSFET	IR	IRF7821	PWRPAKSO8
6	Q3, Q5, Q7, Q9, Q11, Q13		N-Channel Power MOSFET	IR	IRF7832	PWRPAKSO8
3	Q8, Q10, Q12	DNP				
1	R10	536	Thick Film Chip Resistor, 1%	GENERIC	H2511-05360-1/16W1	SM0603
1	R109	100	Thick Film Chip Resistor, 1%	GENERIC	H2511-01000-1/16W1	SM0603
1	R11	2.37k	Thick Film Chip Resistor, 1%	GENERIC	H2511-02371-1/16W1	SM0603
1	R110	2.37k	Thick Film Chip Resistor, 1%	GENERIC	H2511-02371-1/16W1	SM0603

ISL62883C

2-PHASE CPU Application Reference Design Bill of Materials (Continued)

QTY	REFERENCE	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER	PACKAGE
1	R12	499	Thick Film Chip Resistor, 1%	GENERIC	H2511-04990-1/16W1	SM0603
1	R16	147k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01473-1/16W1	SM0603
2	R17, R18	10	Thick Film Chip Resistor, 1%	GENERIC	H2511-00100-1/16W1	SM0603
4	R19, R71, R72, R73	10k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01002-1/16W1	SM0603
1	R23	1.91k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01911-1/16W1	SM0603
1	R26	82.5	Thick Film Chip Resistor, 1%	GENERIC	H2511-082R5-1/16W1	SM0603
5	R20, R40, R56, R57, R58	0	Thick Film Chip Resistor, 1%	GENERIC	H2511-00R00-1/16W1	SM0603
1	R30	604	Thick Film Chip Resistor, 1%	GENERIC	H2511-06040-1/16W1	SM0603
4	R37, R88, R90, R92	1	Thick Film Chip Resistor, 1%	GENERIC	H2511-01R00-1/16W1	SM0603
1	R38	11k	Thick Film Chip Resistor, 1%	GENERIC	H2511-01102-1/16W1	SM0603
1	R4	DNP				
1	R41	2.61k	Thick Film Chip Resistor, 1%	GENERIC	H2511-02611-1/16W1	SM0603
1	R42	10k NTC	Thermistor, 10k NTC	PANASONIC	ERT-J1VR103J	SM0603
1	R50	7.87k	Thick Film Chip Resistor, 1%	GENERIC	H2511-07871-1/16W1	SM0603
1	R6	8.66k	Thick Film Chip Resistor, 1%	GENERIC	H2511-08662-1/16W1	SM0603
3	R63, R65, R67	3.65k	Thick Film Chip Resistor, 1%	GENERIC	H2511-03651-1/16W1	SM0805
2	R8, R9	DNP				
1	R7	324k	Thick Film Chip Resistor, 1%	GENERIC	H2511-03243-1/16W1	SM0603
1	U3		Synchronous Rectified MOSFET Driver	INTERSIL	ISL6208CBZ	SOIC8_150_50
1	U6		IMVP-6.5 PWM Controller	INTERSIL	ISL62883CHRTZ	QFN-40

Typical Performance

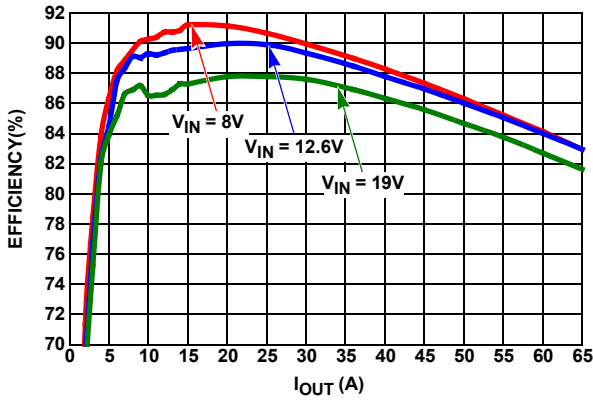


FIGURE 32. 3-PHASE CCM EFFICIENCY, VID = 1.075V, VIN1 = 8V, VIN2 = 12.6V AND VIN3 = 19V

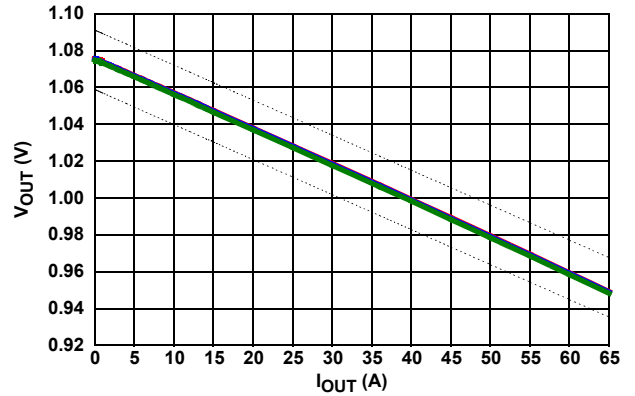


FIGURE 33. 3-PHASE CCM LOAD LINE, VID = 1.075V, VIN1 = 8V, VIN2 = 12.6V AND VIN3 = 19V

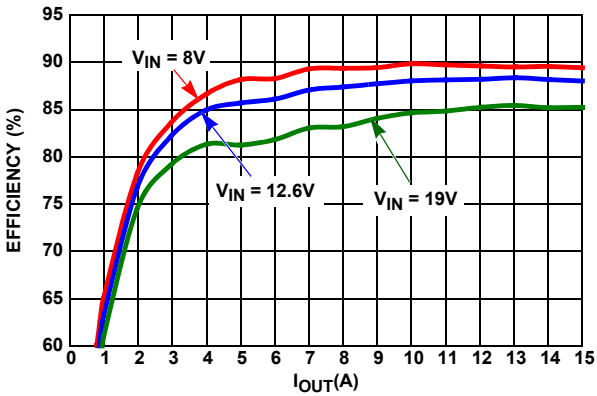


FIGURE 34. 2-PHASE CCM EFFICIENCY, VID = 0.875V, VIN1 = 8V, VIN2 = 12.6V AND VIN3 = 19V

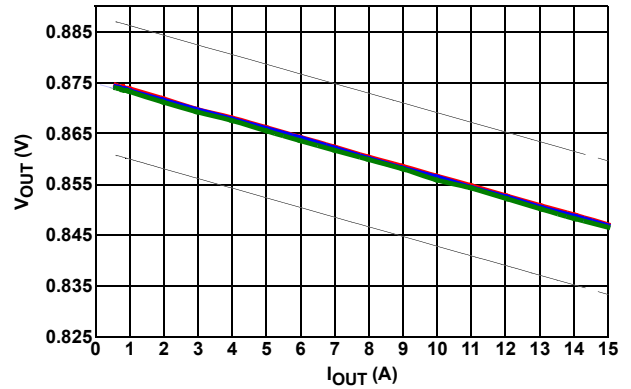


FIGURE 35. 2-PHASE CCM LOAD LINE, VID = 0.875V, VIN1 = 8V, VIN2 = 12.6V AND VIN3 = 19V

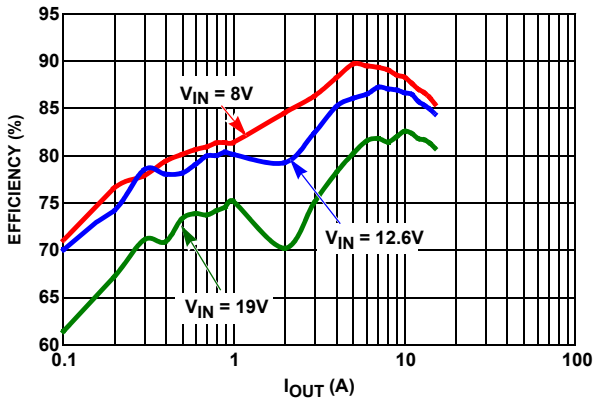


FIGURE 36. 1-PHASE DEM EFFICIENCY, VID = 0.875V, VIN1 = 8V, VIN2 = 12.6V AND VIN3 = 19V

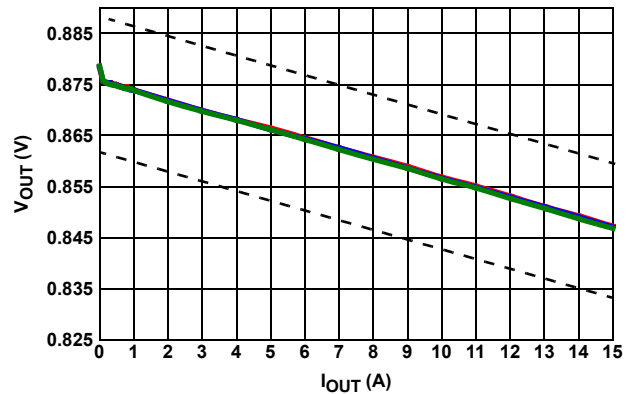


FIGURE 37. 1-PHASE DEM LOAD LINE, VID = 0.875V, VIN1 = 8V, VIN2 = 12.6V AND VIN3 = 19V

Typical Performance (Continued)

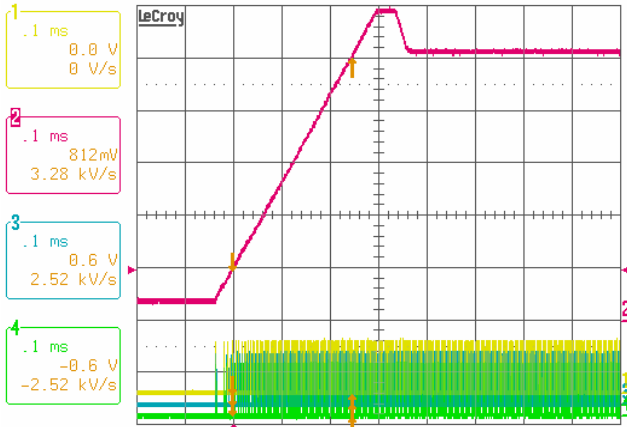


FIGURE 38. SOFT-START, $V_{IN} = 19V$, $I_O = 0A$, $VID = 0.95V$, Ch1: PHASE1, Ch2: V_O , Ch3: PHASE2, Ch4: PHASE3

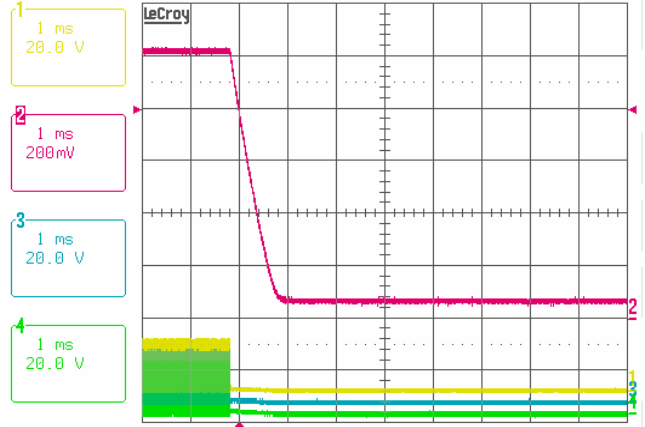


FIGURE 39. SHUT DOWN, $V_{IN} = 19V$, $I_O = 1A$, $VID = 0.95V$, Ch1: PHASE1, Ch2: V_O , Ch3: PHASE2, Ch4: PHASE3

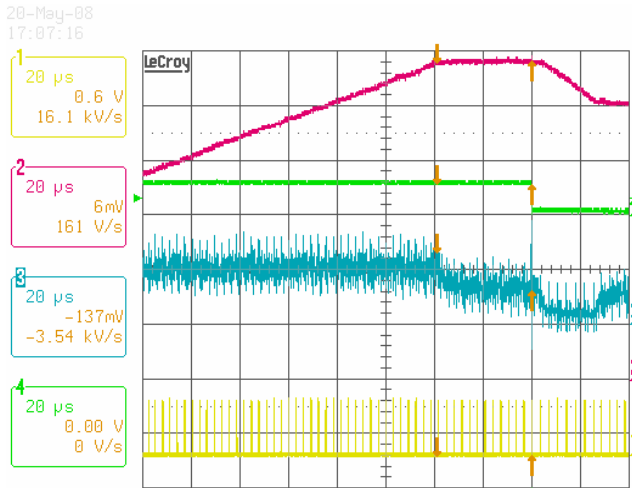


FIGURE 40. CLK_EN# DELAY, $V_{IN} = 19V$, $I_O = 2A$, $VID = 1.5V$, Ch1: PHASE1, Ch2: V_O , Ch3: IMON, Ch4: CLK_EN#

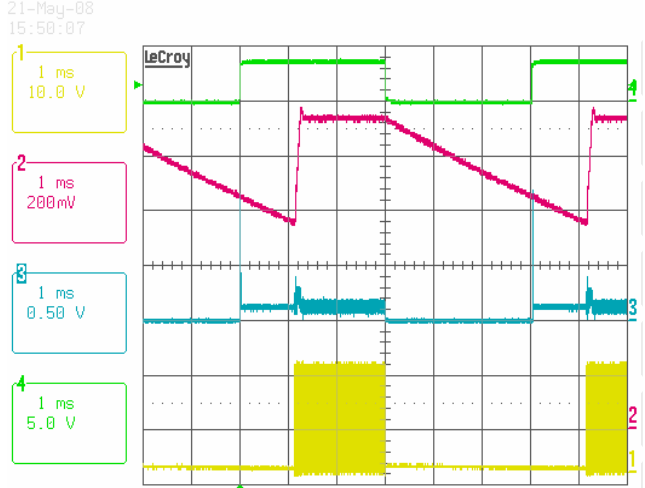


FIGURE 41. PRE-CHARGED START UP, $V_{IN} = 19V$, $VID = 0.95V$, Ch1: PHASE1, Ch2: V_O , Ch3: IMON, Ch4: VR_ON

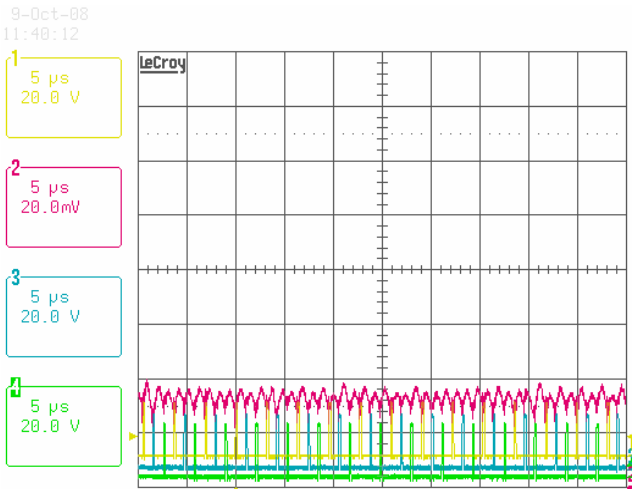


FIGURE 42. STEADY STATE, $V_{IN} = 19V$, $I_O = 51A$, $VID = 0.95V$, Ch1: PHASE1, Ch2: V_O , Ch3: PHASE2, Ch4: PHASE3

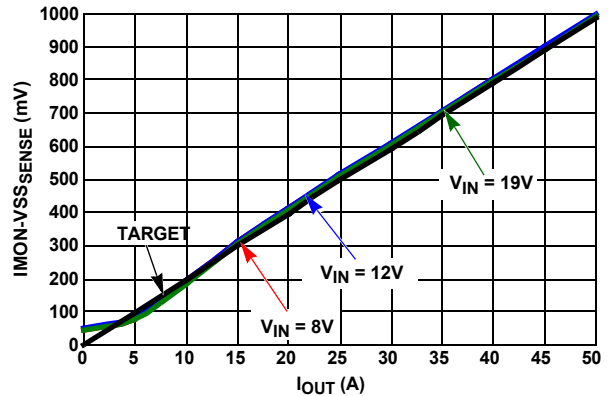


FIGURE 43. IMON, $VID = 1.075V$

Typical Performance (Continued)

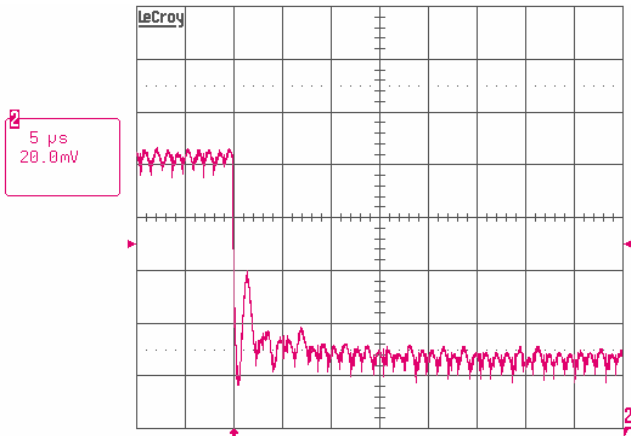


FIGURE 44. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, $V_{IN} = 12V$, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, $I_O = 12A/51A$, di/dt = "FASTEST", LL = 1.9mW

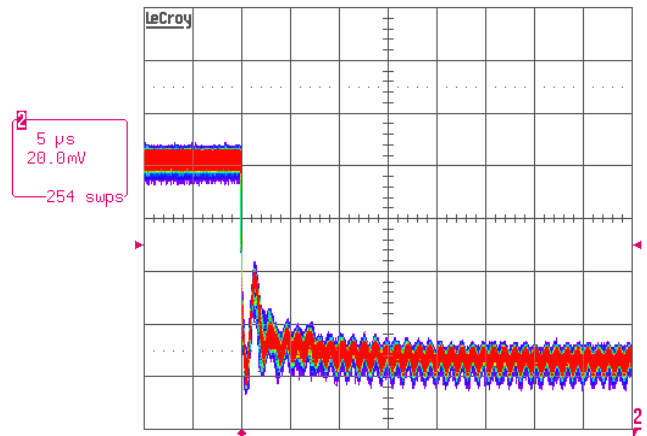


FIGURE 45. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, $V_{IN} = 12V$, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, $I_O = 12A/51A$, di/dt = "FASTEST", LL = 1.9mW

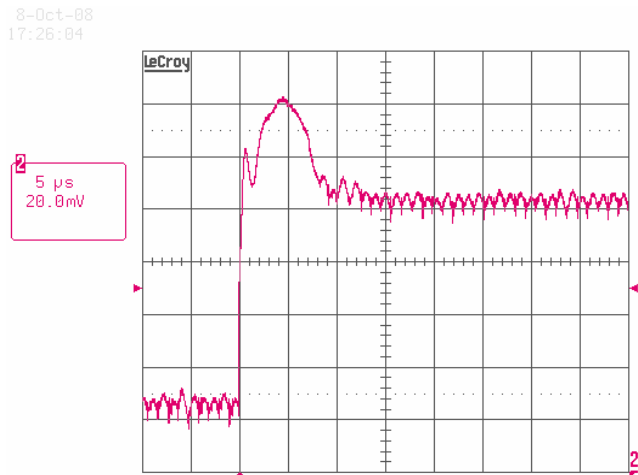


FIGURE 46. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, $V_{IN} = 12V$, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, $I_O = 12A/51A$, di/dt = "FASTEST", LL = 1.9mW

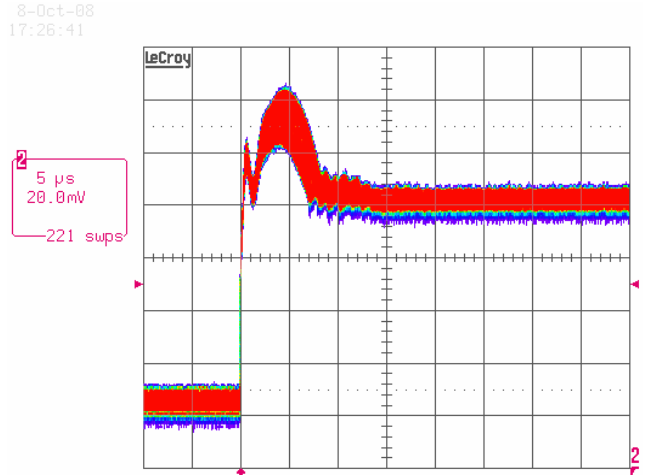


FIGURE 47. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, $V_{IN} = 12V$, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, $I_O = 12A/51A$, di/dt = "FASTEST", LL = 1.9mW

Typical Performance (Continued)

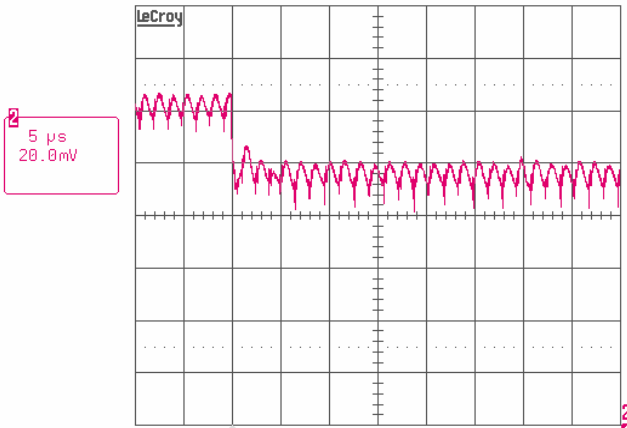


FIGURE 48. 2-PHASE MODE LOAD INSERTION RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, 3-PHASE CONFIGURATION, PSI# = 0, DPRSLPVR = 0, V_{IN} = 12V, VID = 0.875V, I_O = 4A/17A, di/dt = "FASTEST"

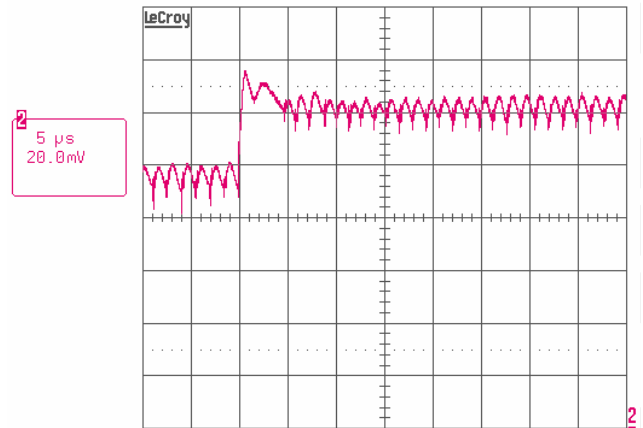


FIGURE 49. 2-PHASE MODE LOAD INSERTION RESPONSE WITH OVERSHOOT REDUCTION FUNCTION DISABLED, 3-PHASE CONFIGURATION, PSI# = 0, DPRSLPVR=0, V_{IN} = 12V, VID = 0.875V, I_O = 4A/17A, di/dt = "FASTEST"

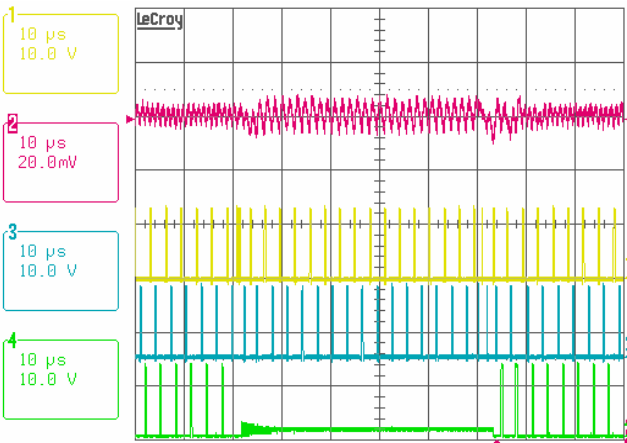


FIGURE 50. PHASE ADDING/DROPPING (PSI# TOGGLE), I_O = 15A, VID = 1.075V, Ch1: PHASE1, Ch2: V_O , Ch3: PHASE2, Ch4: PHASE3

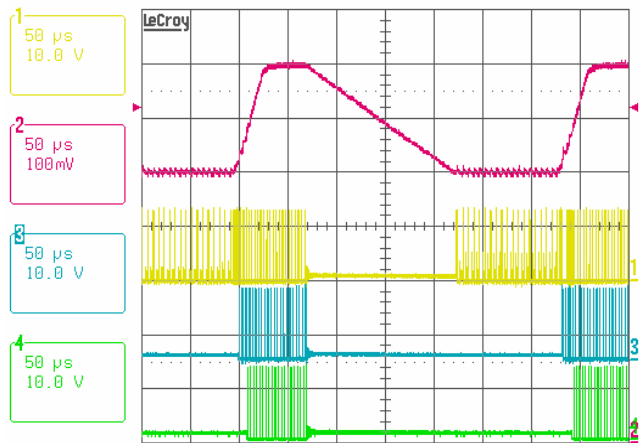


FIGURE 51. DEEPER SLEEP MODE ENTRY/EXIT, I_O = 1.5A, HFM VID = 1.075V, LFM VID = 0.875V, DEEPER SLEEP VID = 0.875V, Ch1: PHASE1, Ch2: V_O , Ch3: PHASE2, Ch4: PHASE3

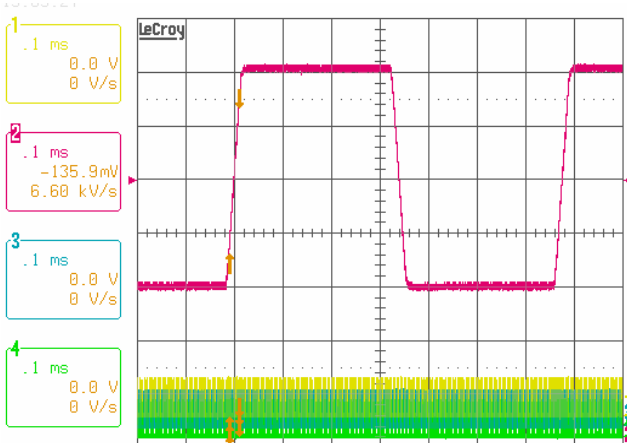


FIGURE 52. VID ON THE FLY, 1.075V/0.875V, 3-PHASE CONFIGURATION, PSI# = 1, DPRSLPVR=0, Ch1: PHASE1, Ch2: V_O , Ch3: PHASE2, Ch4: PHASE3

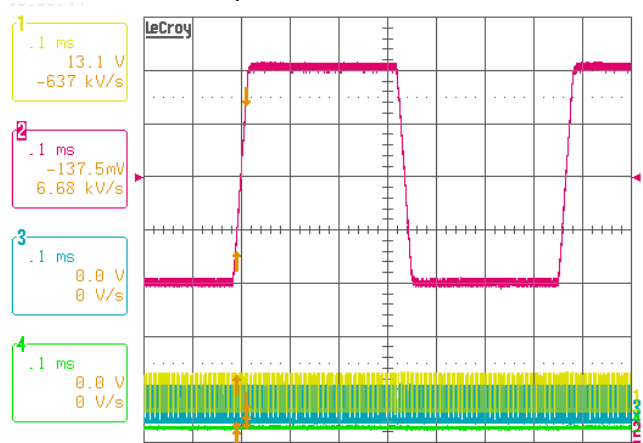


FIGURE 53. VID ON THE FLY, 1.075V/0.875V, 3-PHASE CONFIGURATION, PSI# = 0, DPRSLPVR=0, Ch1: PHASE1, Ch2: V_O , Ch3: PHASE2, Ch4: PHASE3

Typical Performance (Continued)

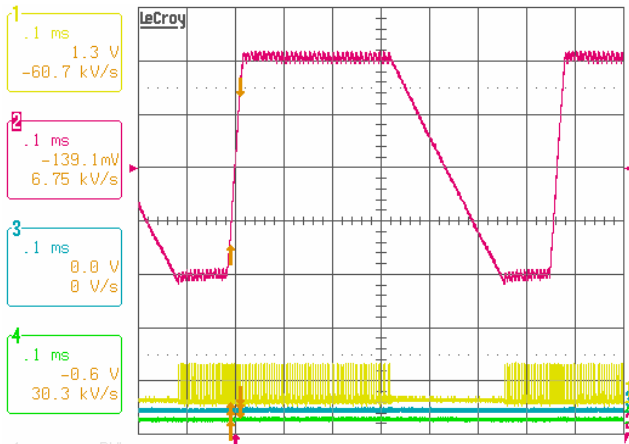


FIGURE 54. VID ON THE FLY, 1.075V/0.875V, 3-PHASE CONFIGURATION, PSI# = 0, DPRSLPVR = 1, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

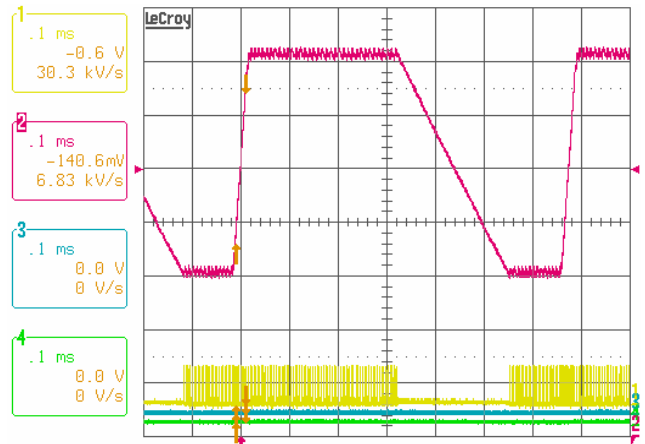


FIGURE 55. VID ON THE FLY, 1.075V/0.875V, 3-PHASE CONFIGURATION, PSI# = 1, DPRSLPVR = 1, Ch1: PHASE1, Ch2: V_O, Ch3: PHASE2, Ch4: PHASE3

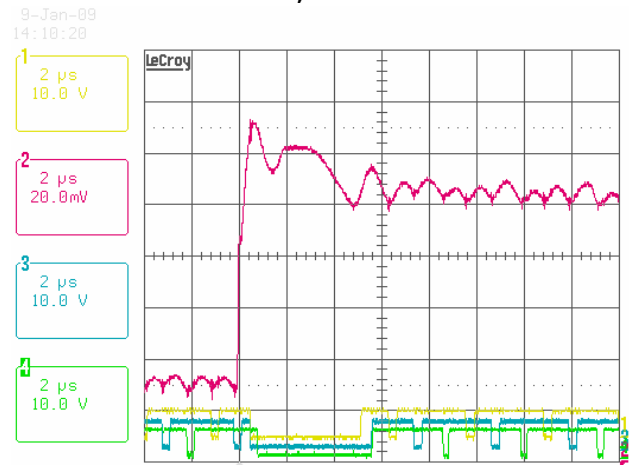


FIGURE 56. LOAD TRANSIENT RESPONSE WITH OVERSHOOT REDUCTION FUNCTION ENABLED, V_{IN} = 12V, SV CLARKSFIELD CPU TEST CONDITION: VID = 0.95V, I_O = 12A/51A, di/dt = "FASTEST", LL = 1.9mW, Ch1: LGATE1, Ch2: V_O, Ch3: LGATE2, Ch4: ISL6208 LGATE



FIGURE 57. REFERENCE DESIGN LOOP GAIN T2(s) MEASUREMENT RESULT

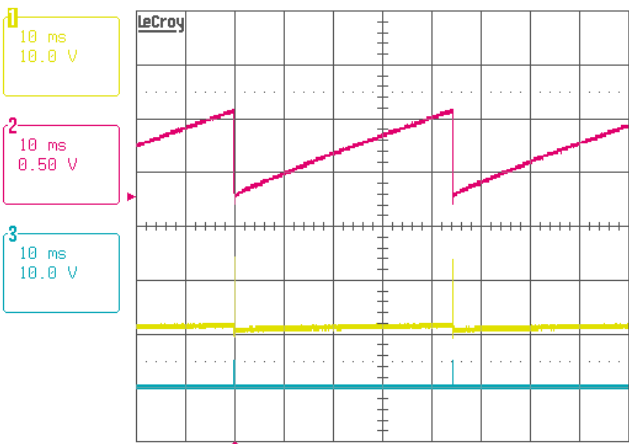


FIGURE 58. 1.55V OVP, Ch1: PHASE1, Ch2: V_O, Ch3: LGATE1

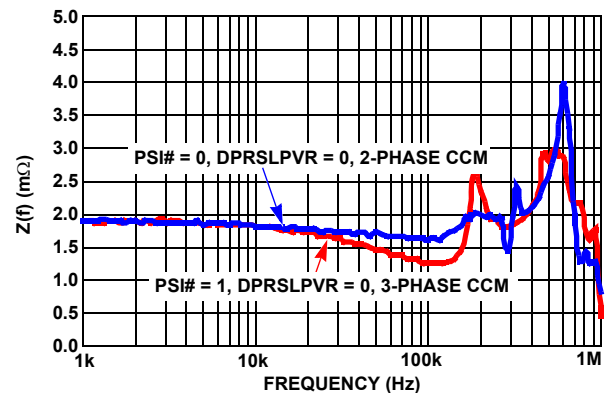


FIGURE 59. REFERENCE DESIGN FDIM RESULT

Typical Performance (Continued)

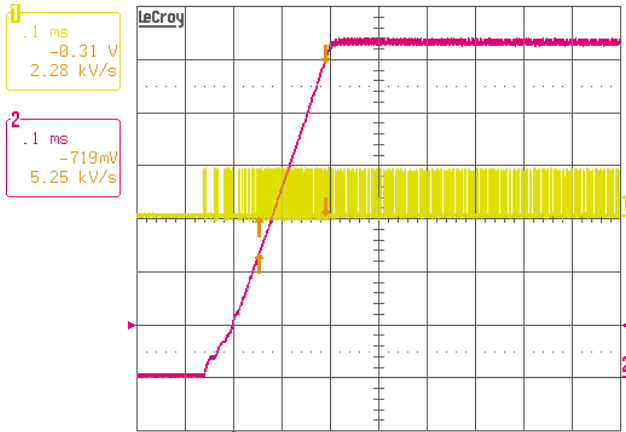


FIGURE 60. 1-PHASE GPU MODE SOFT-START, DPRSLPVR=0, $V_{IN} = 8V$, $I_O = 0A$, VID = 1.2375V, Ch1: PHASE1, Ch2: V_O

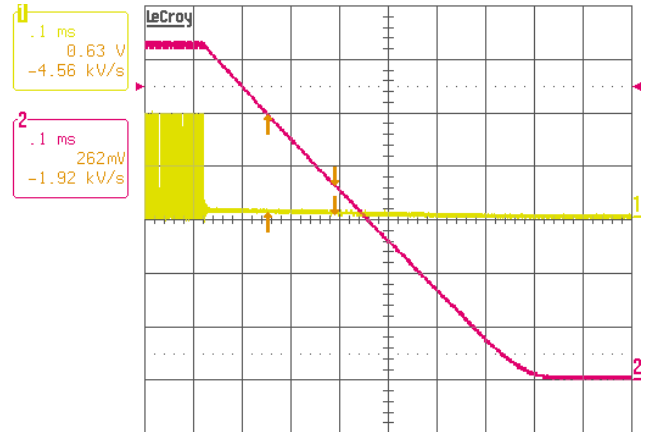


FIGURE 61. 1-PHASE GPU MODE SHUT DOWN, $V_{IN} = 8V$, $I_O = 1A$, VID = 1.2375V, Ch1: PHASE1, Ch2: V_O

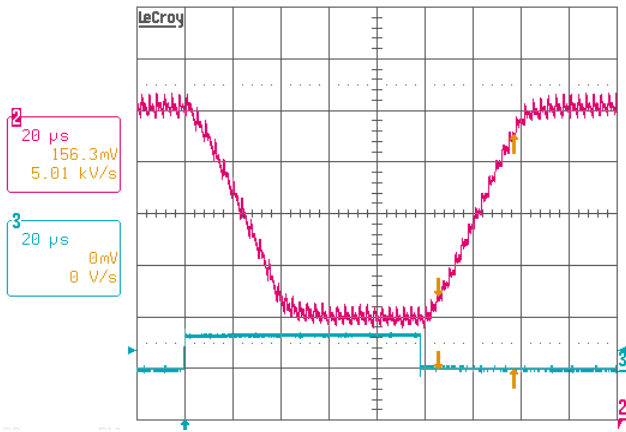


FIGURE 62. 1-PHASE GPU MODE VID TRANSITION, DPRSLPVR=0, $I_O = 2A$, VID = 1.2375V/1.0375V, Ch2: V_O , Ch3: VID4

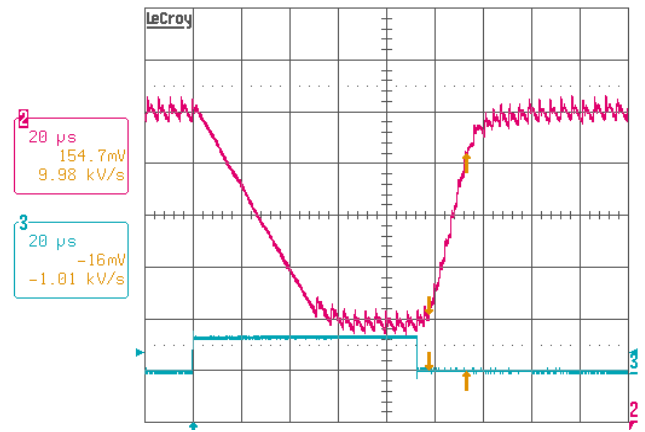


FIGURE 63. 1-PHASE GPU MODE VID TRANSITION, DPRSLPVR=1, $I_O = 2A$, VID = 1.2375V/1.0375V, Ch2: V_O , Ch3: VID4

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL62883C](http://www.intersil.com/ISL62883C)

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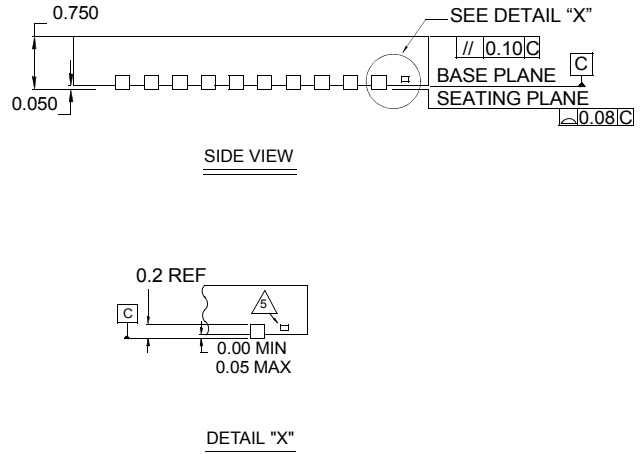
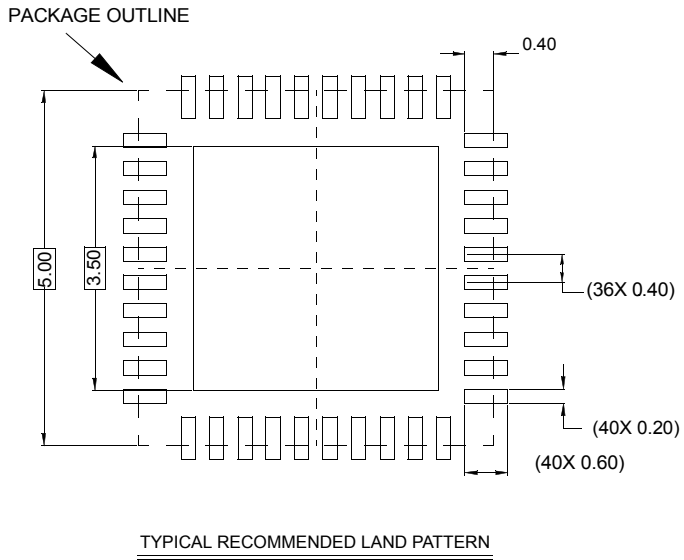
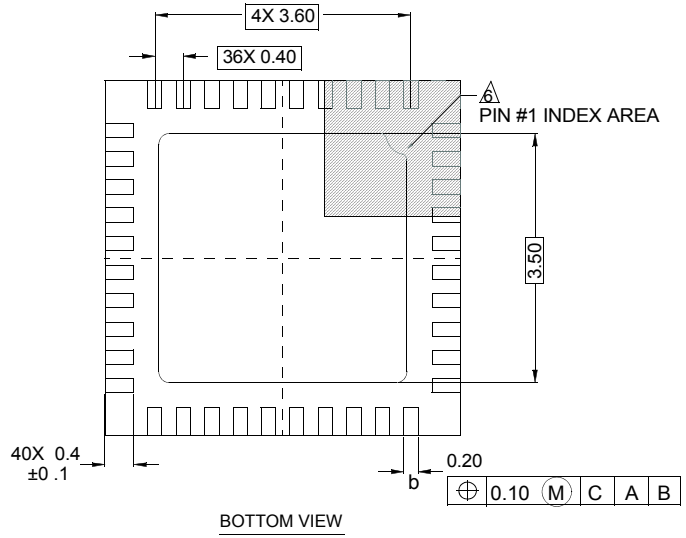
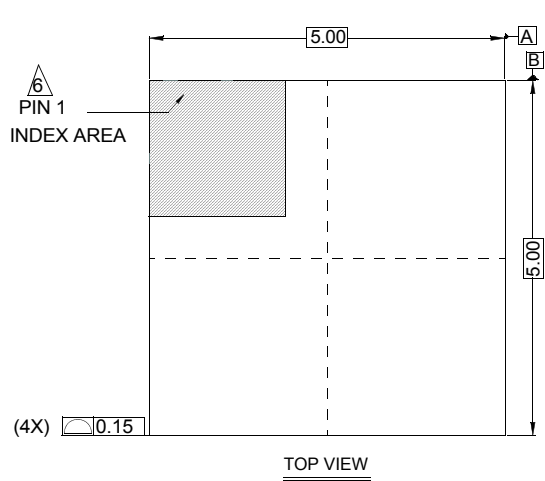
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Package Outline Drawing

L40.5x5

40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 4/07



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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