

# 2.5V Drive Pch+SBD MOS FET

## QS6U22

**●Structure**

Silicon P-channel MOS FET  
Schottky Barrier DIODE

**●Features**

- 1) The QS6U22 combines Pch MOS FET with a Schottky barrier diode in a TSMT6 package.
- 2) Low on-state resistance with fast switching.
- 3) Low voltage drive (2.5V).
- 4) Built-in schottky barrier diode has low forward voltage.

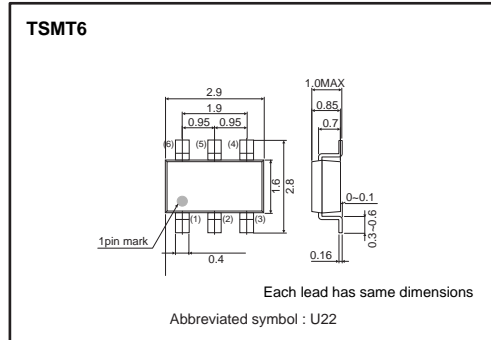
**●Applications**

Load switch, DC / DC conversion

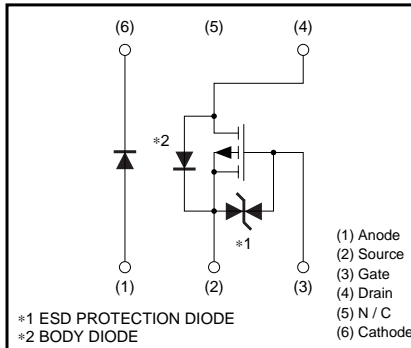
**●Packaging specifications**

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS6U22		○

**●External dimensions (Unit : mm)**



**●Equivalent circuit**



\*1 ESD PROTECTION DIODE  
\*2 BODY DIODE  
\*A protection diode has been in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltages are exceeded.

Transistors

●Absolute maximum ratings (Ta=25°C)

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Parameter	Symbol	Limits	Unit
Drain-source voltage	V <sub>DSS</sub>	-20	V
Gate-source voltage	V <sub>GSS</sub>	±12	V
Drain current	Continuous	I <sub>D</sub>	±1.5
	Pulsed	I <sub>DP</sub> *1	±6.0
Source current (Body diode)	Continuous	I <sub>S</sub>	-0.75
	Pulsed	I <sub>SP</sub> *1	-6.0
Channel temperature	T <sub>ch</sub>	150	°C
Power dissipation	P <sub>D</sub> *3	0.9	W / ELEMENT

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Repetitive peak reverse voltage	V <sub>RM</sub>	25	V
Reverse voltage	V <sub>R</sub>	20	V
Forward current	I <sub>F</sub>	0.7	A
Forward current surge peak	I <sub>FSM</sub> *2	3.0	A
Junction temperature	T <sub>j</sub>	150	°C
Power dissipation	P <sub>D</sub> *3	0.7	W / ELEMENT

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Total power dissipation	P <sub>D</sub> *3	1.25	W / TOTAL
Range of Storage temperature	T <sub>stg</sub>	-55 to +150	°C

\*1 Pw≤10μs, Duty cycles≤1% \*2 60Hz·1cyc. \*3 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>gss</sub>	-	-	±10	μA	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	-20	-	-	V	I <sub>D</sub> =-1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	-	-	-1	μA	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	-0.7	-	-2.0	V	V <sub>DS</sub> =-10V, I <sub>D</sub> =-1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	-	155	215	mΩ	I <sub>D</sub> =-1.5A, V <sub>GS</sub> =-4.5V
		-	170	235	mΩ	I <sub>D</sub> =-1.5A, V <sub>GS</sub> =-4V
		-	310	430	mΩ	I <sub>D</sub> =-0.75A, V <sub>GS</sub> =-2.5V
Forward transfer admittance	Y <sub>fs</sub>   *	1.0	-	-	S	V <sub>DS</sub> =-10V, I <sub>D</sub> =-0.75A
Input capacitance	C <sub>iss</sub>	-	270	-	pF	V <sub>DS</sub> =-10V
Output capacitance	C <sub>oss</sub>	-	40	-	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	-	35	-	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	-	10	-	ns	I <sub>D</sub> =-0.75A
Rise time	t <sub>r</sub> *	-	12	-	ns	V <sub>DD</sub> ≐-15V
Turn-off delay time	t <sub>d(off)</sub> *	-	45	-	ns	V <sub>GS</sub> =-4.5V
						R <sub>L</sub> =20Ω
Fall time	t <sub>f</sub> *	-	20	-	ns	R <sub>G</sub> =10Ω
Total gate charge	Q <sub>g</sub> *	-	3.0	-	nC	V <sub>DD</sub> ≐-15V
Gate-source charge	Q <sub>gs</sub> *	-	0.8	-	nC	V <sub>GS</sub> =-4.5V
Gate-drain charge	Q <sub>gd</sub> *	-	0.85	-	nC	R <sub>L</sub> =10Ω / R <sub>G</sub> =10Ω
						I <sub>D</sub> =-1.5A

\*Pulsed

<Body diode (source-drain)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub>	-	-	-1.2	V	I <sub>S</sub> =-0.75A, V <sub>GS</sub> =0V

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage drop	V <sub>F</sub>	-	-	0.49	V	I <sub>F</sub> =0.7A
Reverse current	I <sub>R</sub>	-	-	200	μA	V <sub>R</sub> =20V

Transistors

●Electrical characteristic curves  
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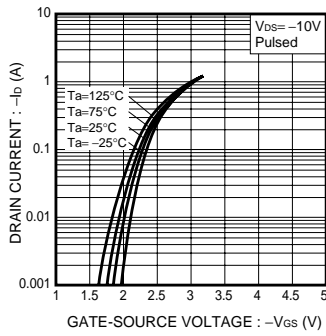


Fig.1 Typical Transfer Characteristics

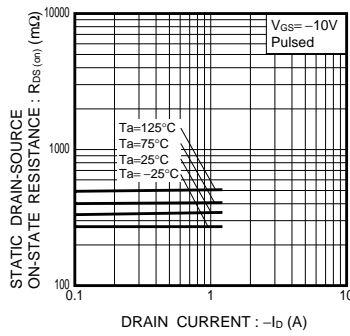


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (I)

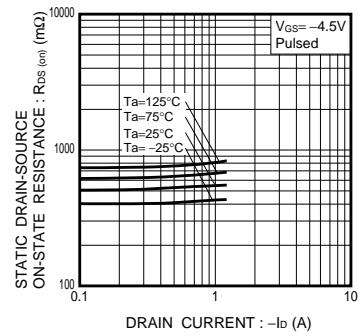


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (II)

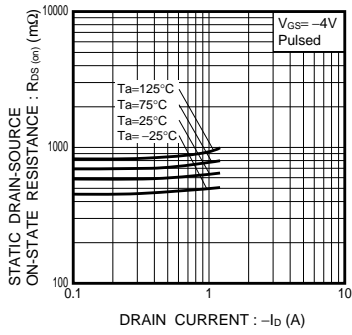


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (III)

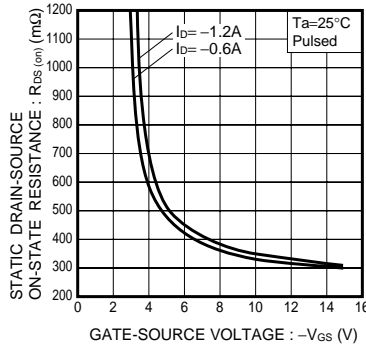


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

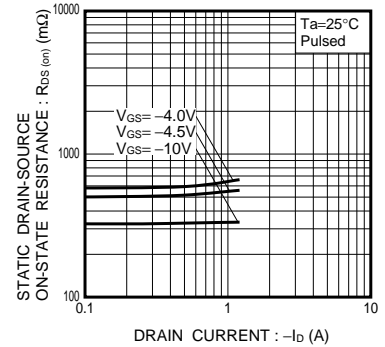


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (IV)

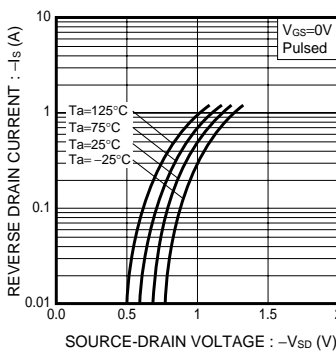


Fig.7 Reverse Drain Current vs. Source-Drain Voltage

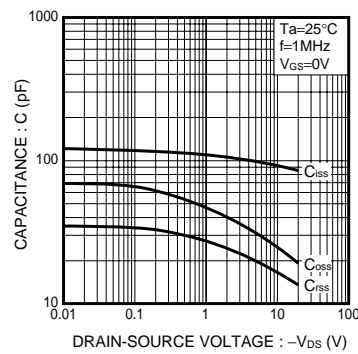


Fig.8 Typical Capacitance vs. Drain-Source Voltage

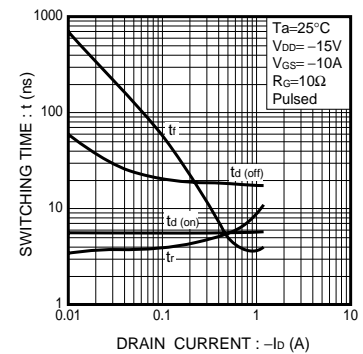


Fig.9 Switching Characteristics

Transistors

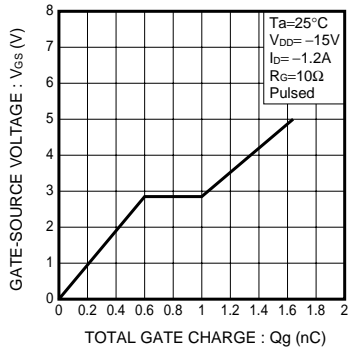


Fig.10 Dynamic Input Characteristics

●Measurement circuits

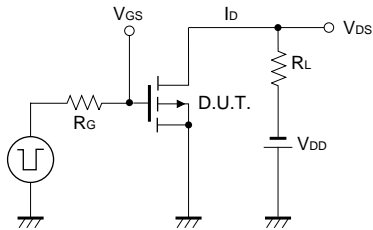


Fig.11 Switching Time Measurement Circuit

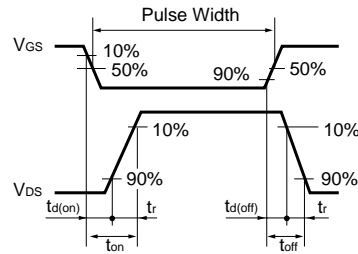


Fig.12 Switching Waveforms

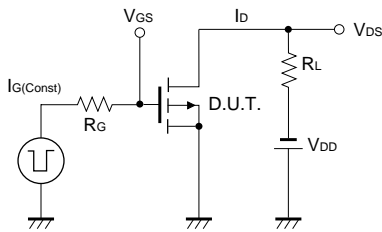


Fig.13 Gate Charge Measurement Circuit

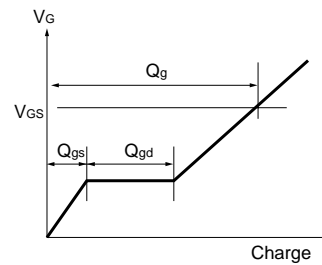


Fig.14 Gate Charge Waveform

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