3A, 1MHz, Synchronous Step-Down Converter

General Description

The RT8061A is a high efficiency synchronous, step-down DC/DC converter. Its input voltage range from 2.7V to 5.5V that provides an adjustable regulated output voltage from 0.6V to V_{IN} while delivering up to 3A of output current. The internal synchronous low on resistance power switches increase efficiency and eliminate the need for an external Schottky diode. The switching frequency is fixed internally at 1MHz. The 100% duty cycle provides low dropout operation, hence extending battery life in portable systems. Current mode operation with internal compensation allows the transient response to be optimized over a wide range of loads and output capacitors. The RT8061A is operated in PWM/PSM mode to achieve high efficiency for a wide load range. The RT8061A is available in a WDFN-10L 3x3 package.

Ordering Information

RT8061A□□

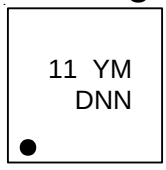
- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



11 : Product Code

YMDNN : Date Code

Features

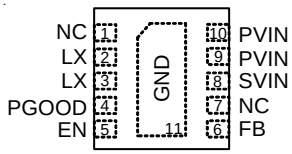
- **High Efficiency : Up to 95%**
- **Low $R_{DS(ON)}$ Internal Switches : 69mΩ/49mΩ at V_{IN} = 5V**
- **Fixed Frequency : 1MHz**
- **No Schottky Diode Required**
- **0.6V Reference Allows Low Output Voltage**
- **PWM/PSM Mode Operation**
- **Low Dropout Operation : 100% Duty Cycle**
- **OCP, UVP, OVP, OTP**
- **RoHS Compliant and Halogen Free**

Applications

- Portable Instruments
- Battery-Powered Equipment
- Notebook Computers
- Distributed Power Systems
- IP Phones
- Digital Cameras

Pin Configurations

(TOP VIEW)



WDFN-10L 3x3

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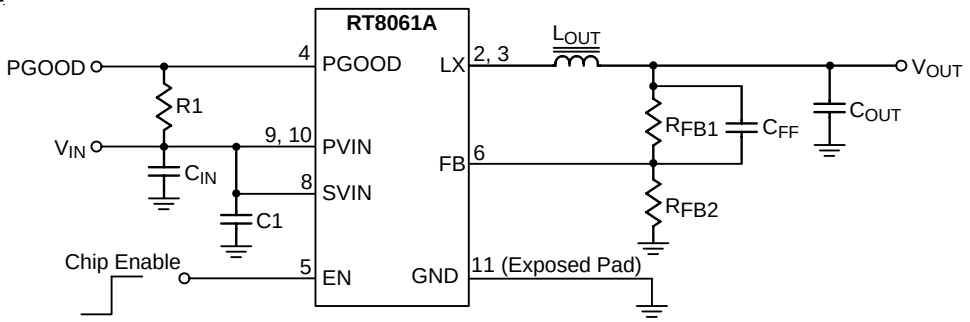
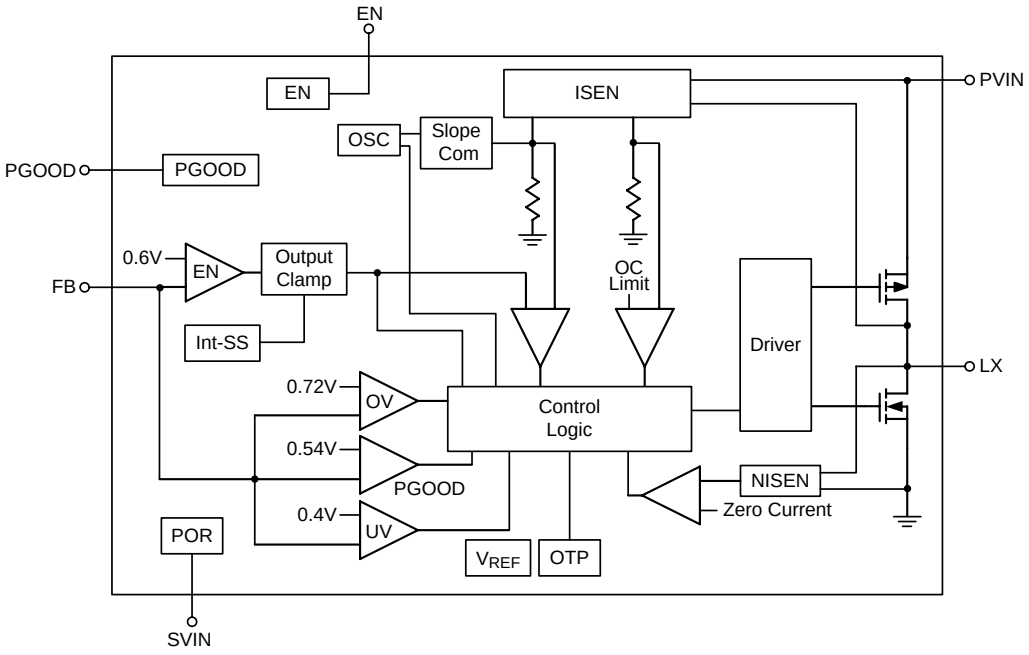
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 7	NC	No Internal Connection.
2, 3	LX	Switch Node. Connection this pin to the inductor.
4	PGOOD	Power Good Indicator. This pin is an open drain logic output that is pulled to ground when the output voltage is less than 90% of the target output voltage.
5	EN	Enable Control. Pull high to turn on. Do not float.
6	FB	Feedback. This pin receives the feedback voltage from a resistive voltage divider connected across the output.
8	SVIN	Signal Input. Decouple this pin to GND with at least 1μF ceramic cap.
9, 10	PVIN	Power Input. Decouple this pin to GND with at least 4.7μF ceramic cap.
11 (Exposed Pad)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, PVIN, SVIN ---------- –0.3V to 6.5V
- LX Pin Voltage ---------- (V_{IN} + 0.3V) to 6.8V
- Other I/O Pin Voltage ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WDNF-10L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  WDFN-10L 3x3 θ_{JC} ---------- 8.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, PVIN, SVIN ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Reference Voltage		V_{REF}		0.594	0.6	0.606	V
Feedback Leakage Current		I_{FB}		--	0.1	0.4	μA
DC Bias Current			Active , V_{FB} = 0.7V, Not Switching	--	110	140	μA
			Shutdown	--	--	1	
Output Voltage Line Regulation			V_{IN} = 2.7V to 5.5V I_{OUT} = 0A	--	0.3	--	%/V
Output Voltage Load Regulation			I_{OUT} = 0A to 3A	–1	--	1	%
Switch Leakage Current			V_{EN} = 0A	--	--	1	μA
Switching Frequency				0.8	1	1.2	MHz
Switch On Resistance, High		$R_{DS(ON)_P}$	V_{IN} = 5V	--	69	--	mΩ
Switch On Resistance, Low		$R_{DS(ON)_N}$	V_{IN} = 5V	--	49	--	mΩ
PMOS Current Limit (latch-off)		I_{LIM}		4	--	--	A
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	2.2	2.4	2.6	V
			V_{IN} Falling	2	2.2	2.4	
EN Threshold Voltage	Logic-High	V_{IH}		1.6	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
EN Pull Low Resistance				--	500	--	kΩ

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over Temperature Protection (latch-off)	T_{SD}		--	150	--	°C
Soft-Start Time	t_{SS}		500	--	--	μs
V_{OUT} Discharge Resistance			--	100	--	Ω
V_{OUT} Over Voltage Protection (latch-off, delay time = 10μs)			115	120	130	%
V_{OUT} Under Voltage Lockout Threshold (latch-off)			57	66	75	%
Power Good		Measured FB, With Respect to V_{REF}	85	90	--	%
Power Good Hysteresis			--	5	--	%

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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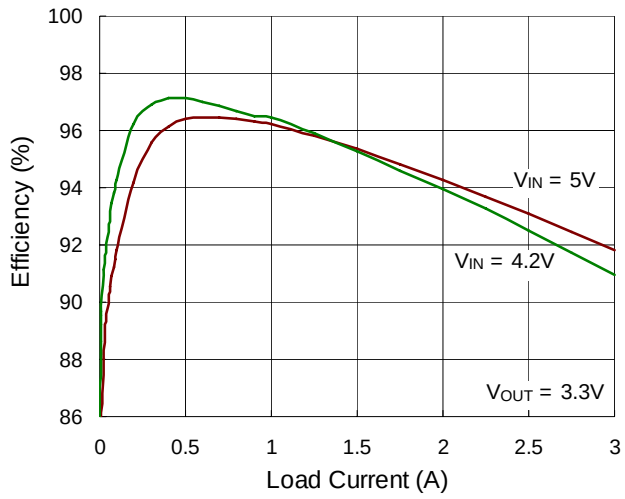
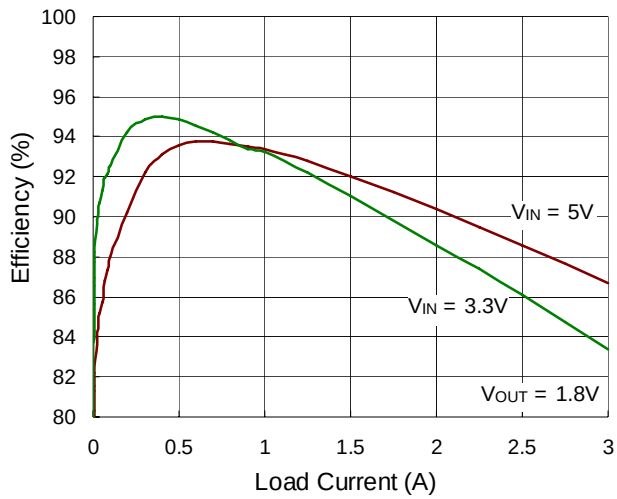
Typical Operating Characteristics

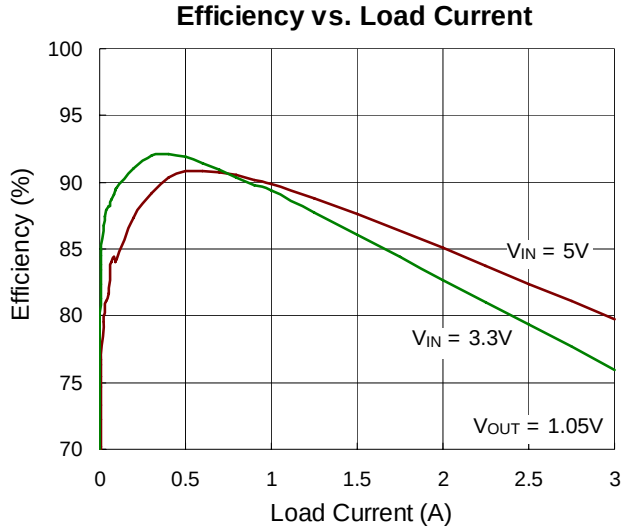
Efficiency vs. Load Current



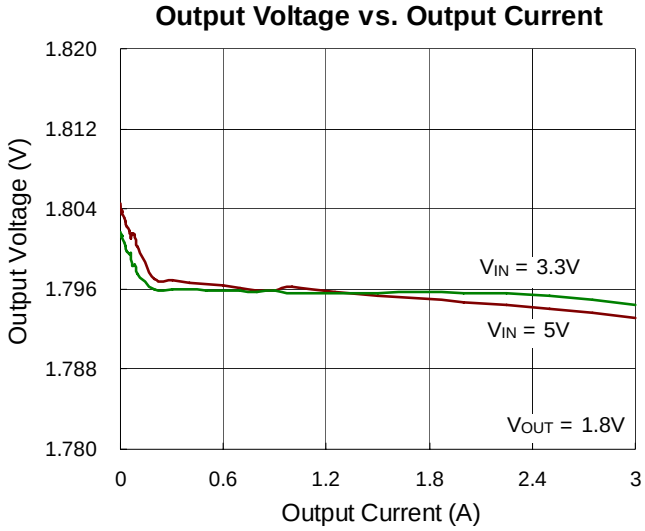
Efficiency vs. Load Current



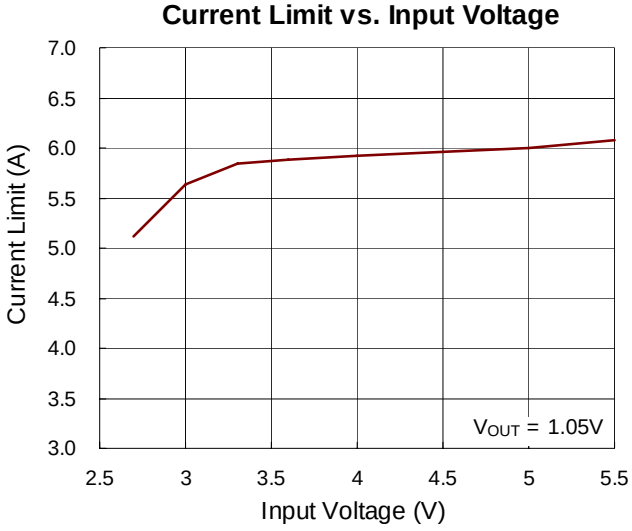
Efficiency vs. Load Current



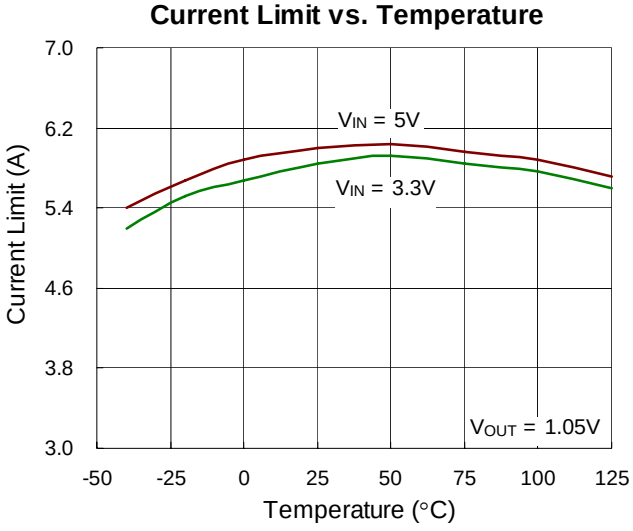
Output Voltage vs. Output Current



Current Limit vs. Input Voltage



Current Limit vs. Temperature



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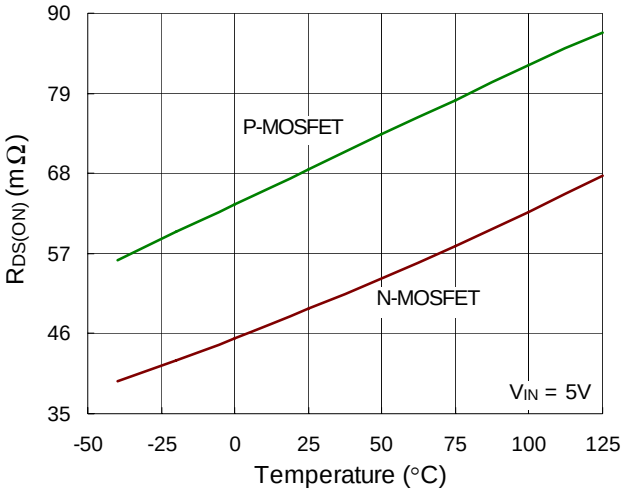
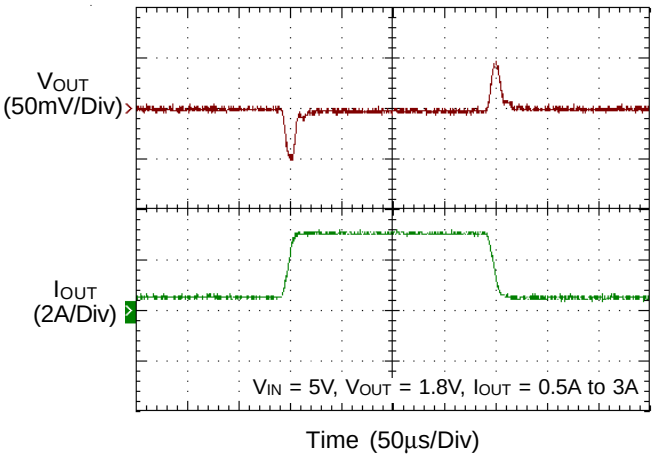
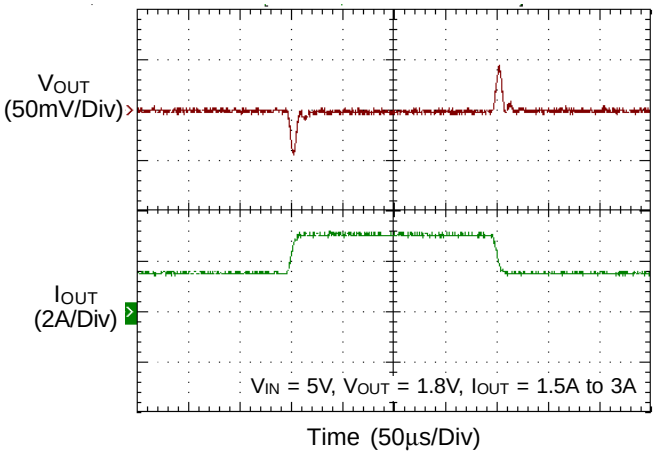
$R_{DS(ON)}$ vs. Temperature



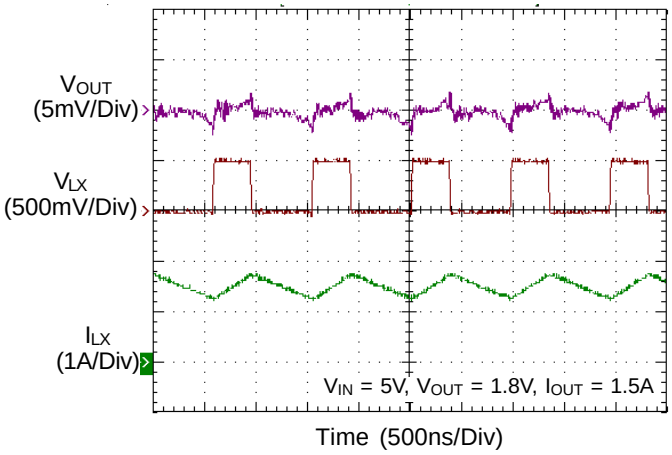
Load Transient Response



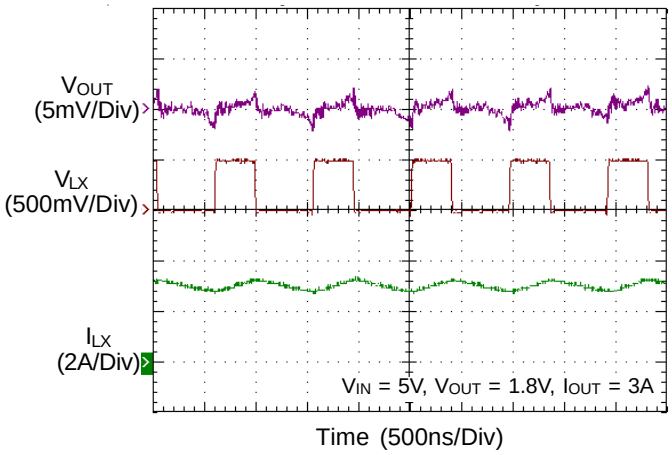
Load Transient Response



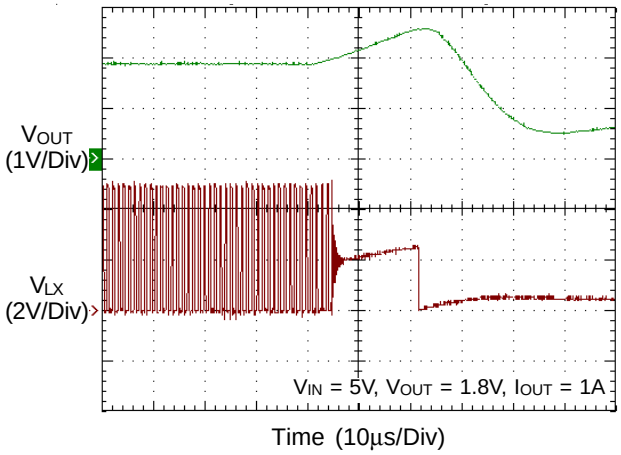
Switching



Switching



Over Voltage Protection



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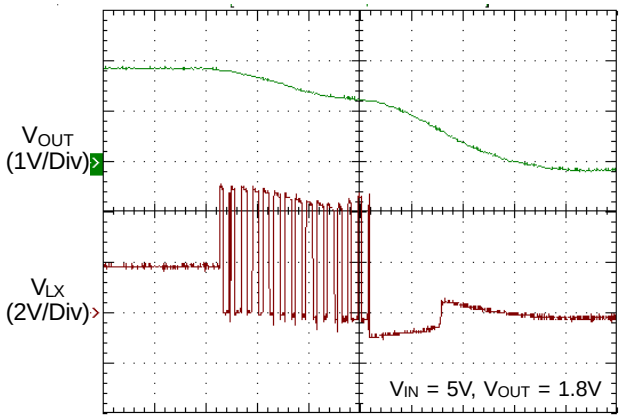
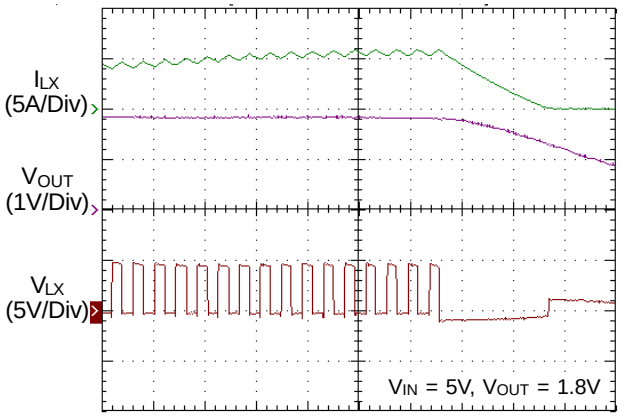
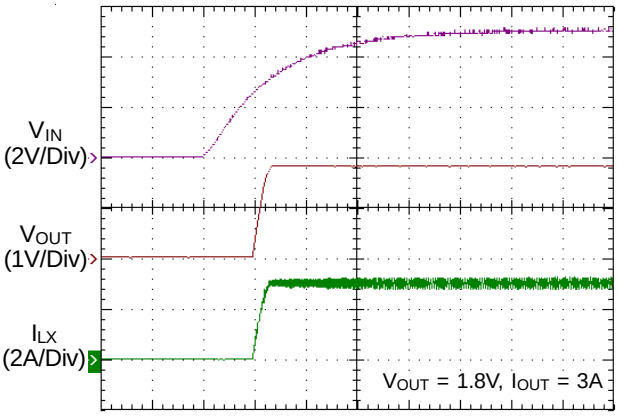
Under Voltage Protection



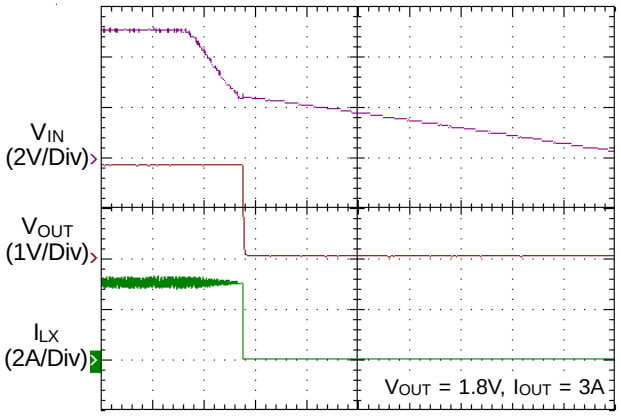
Over Current Protection



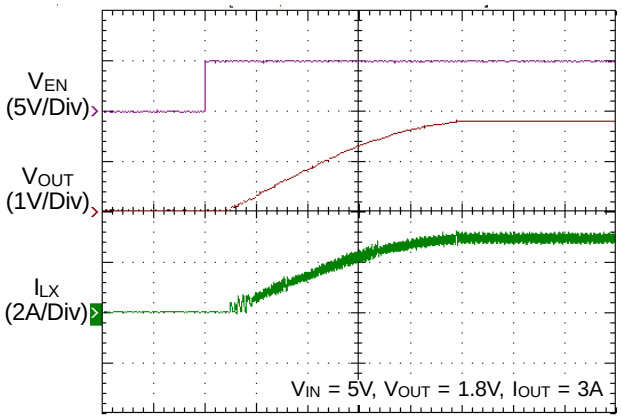
Power On from V_{IN}



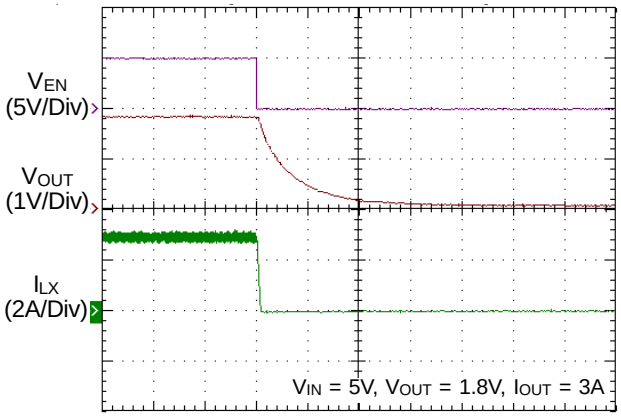
Power Off from V_{IN}



Power On from EN



Power Off from EN



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Application Information

The RT8061A is a single-phase buck PWM converter. It provides single feedback loop, current mode control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (1MHz) oscillator and internal compensation are integrated to minimize external component count. Protection features include over current protection, under voltage protection, over voltage protection and over temperature protection.

PWM Operation

The RT8061A utilizes DEM control to improve light load efficiency. Depending on the load current, the controller automatically operates in Diode-Emulation Mode (DEM) or in Continuous Conduction Mode (CCM) with fixed-frequency PWM.

At light load condition, the RT8061A automatically operates in diode-emulation mode to reduce switching frequency and improve efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point where its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial negative current to flow when the inductor freewheeling current reaches negative. As the load current further decreases, it takes longer and longer to discharge the output capacitor to the level that that requires the next UGATE "ON" cycle. In contrast, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The controller will then operate in continuous conduction mode with 1MHz fixed PWM switching frequency.

Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{FB} is 0.6V (typ.).

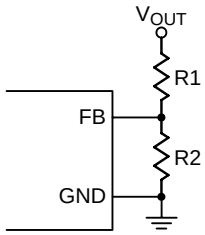

Figure 1. Setting V_{OUT} with a Voltage Divider

Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT8061A remains in shutdown if the EN pin is lower than 400mV. When the EN pin rises above the V_{EN} trip point, the RT8061A begins a new initialization and soft-start cycle.

Internal Soft-Start

The RT8061A provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The Soft-Start (SS) automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the output surge current. The internal 0.6V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V.

UVLO Protection

The RT8061A has input Under Voltage Lockout protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage (2.4V typ.), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

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where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor.

Input Capacitor Selection

High quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 20µF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{IN_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The next step is selecting a proper capacitor for RMS current rating. One good design is using more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{IN} \times f_{SW}}$$

For example, if $I_{OUT(MAX)}$ = 3A, C_{IN} = 20µF, f_{SW} = 1MHz, the input voltage ripple will be 37.5mV.

Output Capacitor Selection

The output capacitor and the inductor form a low pass filter in the buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in ripple voltage. The output voltage ripple (V_{P-P}) can be calculated by the following equation :

$$V_{P-P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage undershoot (V_{SAG}) can be calculated by the following equation :

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

Unlike the electrolytic capacitor, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, use a mixed combination of electrolytic capacitor and ceramic capacitor to obtain better transient performance.

Power Good Output (PGOOD)

PGOOD is an open-drain type output and requires a pull-up resistor. PGOOD is actively held low in soft-start, standby, and shutdown. It is released when the output voltage rises above 90% of nominal regulation point. The PGOOD signal goes low if the output is turned off or is 10% below its nominal regulation point.

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Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage. When under voltage protection is enabled, both UGATE and LGATE gate drivers will be forced low if the output is less than 66% of its set voltage threshold. The UVP will be ignored for at least 3ms (typ.) after start up or a rising edge on the EN threshold. Toggle EN threshold or cycle V_{IN} to reset the UVP fault latch and restart the controller.

Over Voltage Protection (OVP)

The RT8061A is latched once OVP is triggered and can only be released by toggling EN threshold or cycling V_{IN}. There is a 10µs delay built into the over voltage protection circuit to prevent false transition.

Over Current Protection (OCP)

The RT8061A provides over current protection by detecting high side MOSFET peak inductor current. If the sensed peak inductor current remains over 4A (typ) for 5 clock cycles, OCP will be triggered. When OCP trips, the RT8061A will shut down and enter Latch-Off Mode to stop the energy transfer to the load. In Latch-Off Mode, the RT8061A can only be reset by EN or V_{IN}.

Thermal Shutdown (OTP)

The device implements internal thermal shutdown when the junction temperature exceeds 150°C. When the OTP function is triggered, the RT8061A shuts down and enters Latch-Off Mode. In Latch-Off Mode, the RT8061A can be reset by EN or V_{IN}.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-10L 3x3 packages, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for

WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

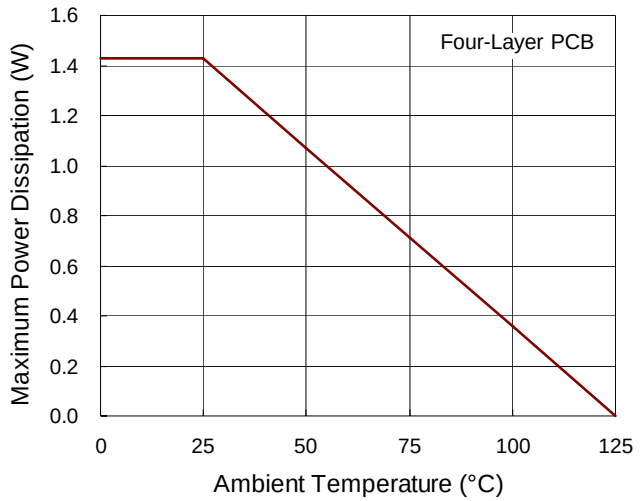

Figure 2. Derating Curve of Maximum Power Dissipation

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Layout Considerations

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout. Certain points must be considered before starting a layout using the RT8061A.

- Make the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (V_{IN} and GND).
- LX node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the LX node to prevent stray capacitive noise pick-up.
- Ensure all feedback network connections are short and direct. Place the feedback network as close to the chip as possible.
- The GND pin and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.
- An example of PCB layout guide is shown in Figure 3. for reference.

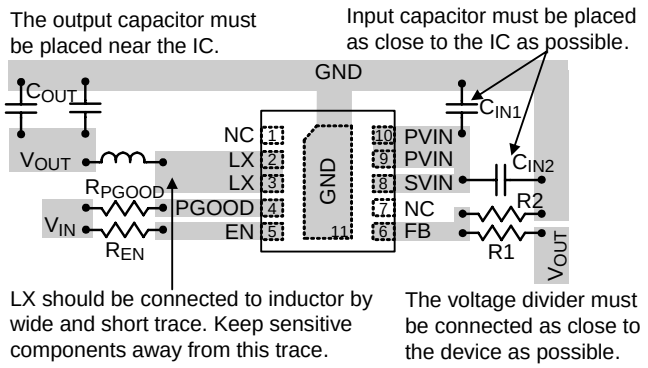

Figure 3. PCB Layout Guide

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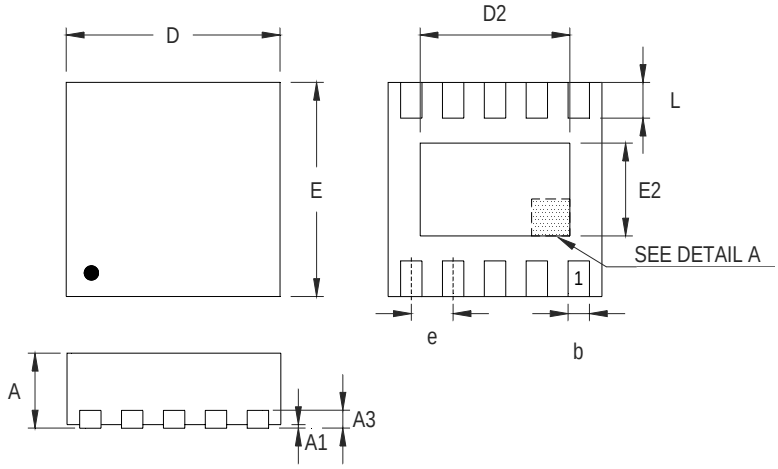
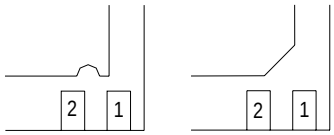
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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