Complete DDRII/DDRIII Memory Power Supply Controller

General Description

The RT8207 provides a complete power supply for both DDRII/DDRIII memory systems. It integrates a synchronous PWM buck controller with a 3A sink/source tracking linear regulator and a buffered low noise reference.

The PWM controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low voltage chipset RAM supplies in notebook computers. The constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT8207 achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs. The buck conversion allows this device to directly step down high-voltage batteries for the highest possible efficiency.

The 3A sink/source LDO maintains fast transient response only requiring 20µF of ceramic output capacitance. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The RT8207 supports all of the sleep state controls placing VTT at High-Z in S3 and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5.

The RT8207 has all of the protection features including thermal shutdown and is available in the WQFN-24L 4x4 package.

Ordering Information

RT8207 □□

- Package Type
  QW : WQFN-24L 4x4 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

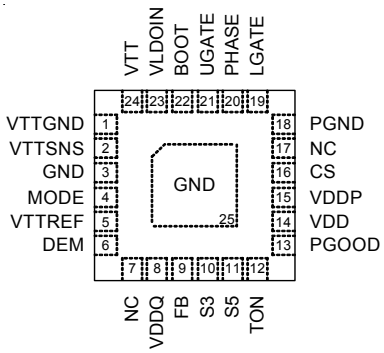
- **PWM Controller**
  - **Resistor Programmable Current Limit by Low-Side $R_{DS(ON)}$ Sense**
  - **Quick Load-Step Response within 100ns**
  - **1% V_{OUT} Accuracy Over Line and Load**
  - **Fixed 1.8V (DDRII), 1.5V (DDRIII) or Adjustable 0.75V to 3.3V Output Range**
  - **Battery Input Range 2.5V to 26V**
  - **Resistor Programmable Frequency**
  - **Over/Under Voltage Protection**
  - **4 Steps Current Limit During Soft-Start**
  - **Drives Large Synchronous-Rectifier FETs**
  - **Power-Good Indicator**
- **3A LDO (VTT), Buffered Reference (VTTREF)**
  - **Capable to Sink and Source Up to 3A**
  - **LDO Input Available to Optimize Power Losses**
  - **Requires Only 20µF Ceramic Output Capacitor**
  - **Buffered Low Noise 10mA VTTREF Output**
  - **Accuracy ±20mV for Both VTTREF and VTT**
  - **Supports High-Z in S3 and Soft-Off in S4/S5**
- **RoHS Compliant and Halogen Free**

Applications

- DDRII/DDRIII Memory Power Supplies
- Notebook Computers
- SSTL18, SSTL15 and HSTL Bus Termination

Pin Configurations

(TOP VIEW)



WQFN-24L 4x4

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Typical Application Circuit

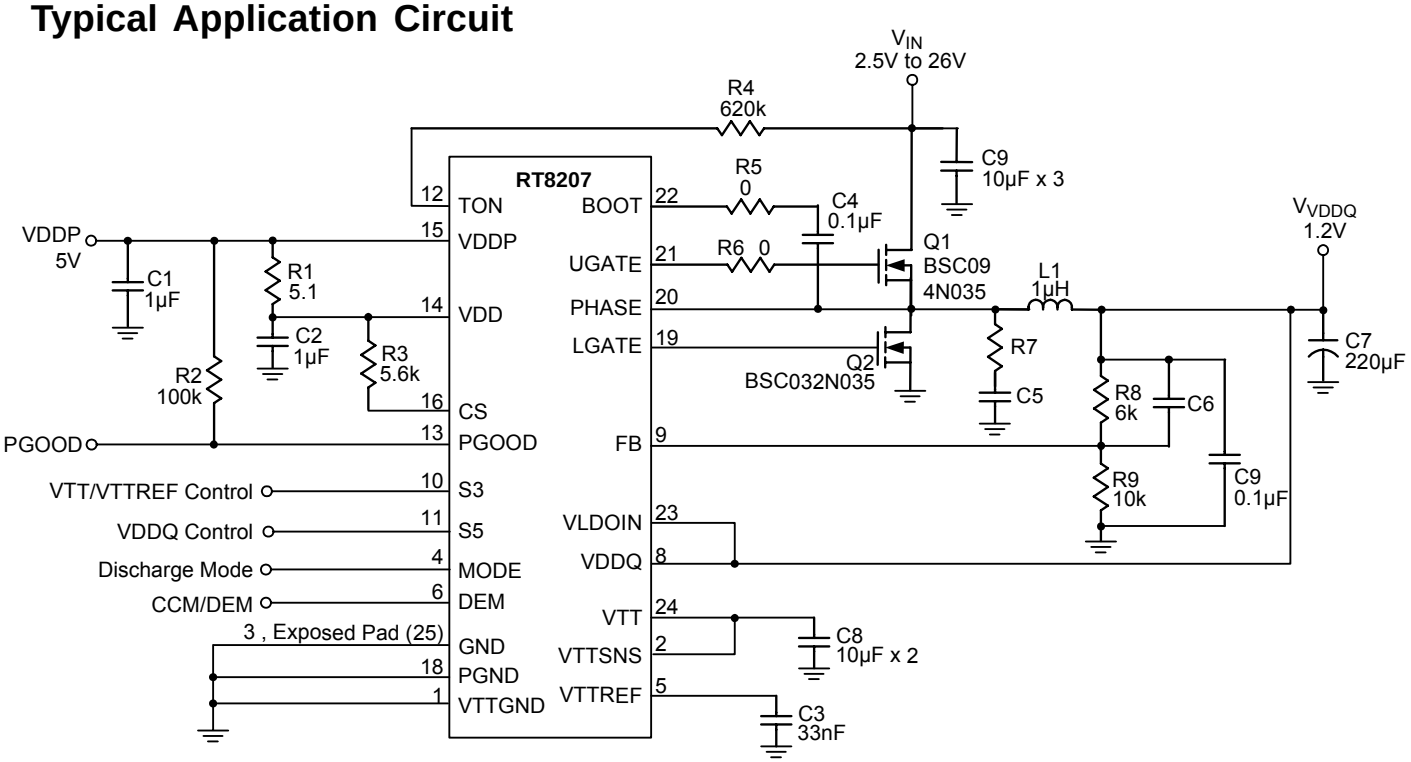


Figure A. Adjustable Voltage Regulator

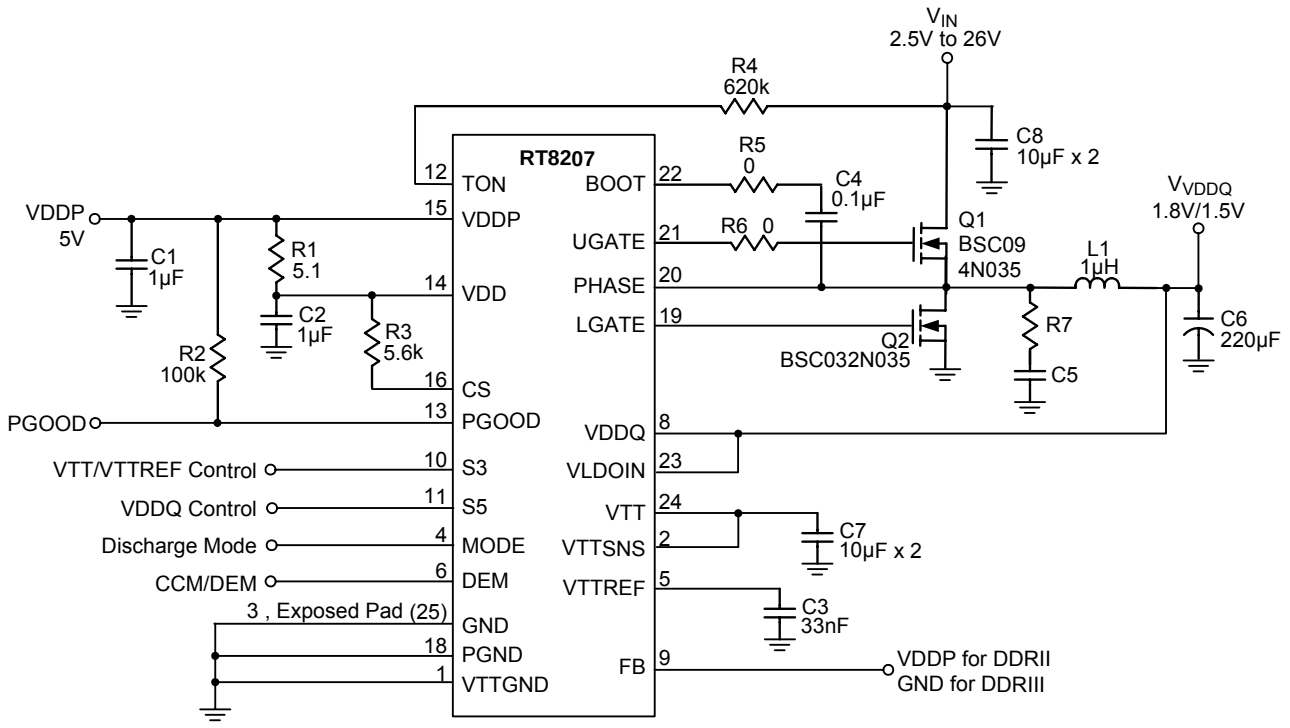
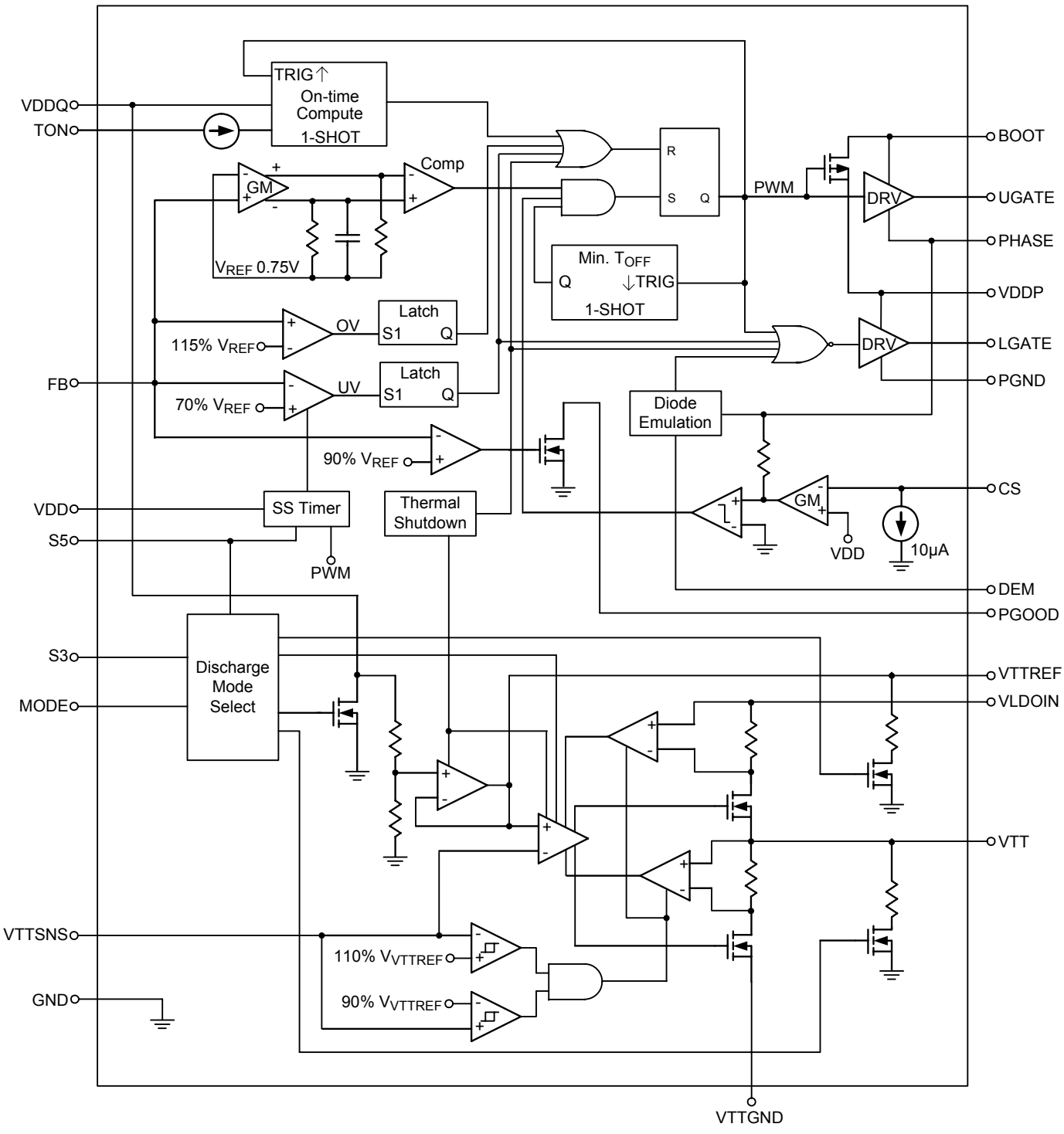


Figure B. Fixed Voltage Regulator

Function Block Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VTTGND	Power Ground for the VTT_LDO.
2	VTTSNS	Voltage Sense Input for the VTT_LDO. Connect to the terminal of the VTT_LDO output capacitor
3, 25 (Exposed Pad)	GND	Analog Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	MODE	Output Discharge Mode Setting Pin. Connect to VDDQ for tracking discharge. Connect to GND for non-tracking discharge. Connect to VDD for no discharge.
5	VTTREF	VTTREF Buffered Reference Output.
6	DEM	Diode-Emulation Mode Enable Pin. Connect to VDD will enable diode-emulation mode. Connect to GND will always operate in forced CCM mode.
7, 17	NC	No Internal Connection.
8	VDDQ	VDDQ Reference Input for VTT and VTTREF. Discharge current sinking terminal for VDDQ non-tracking discharge. Output voltage feedback input for VDDQ output if FB pin is connected to VDD or GND
9	FB	VDDQ Output Setting Pin. Connect to GND for DDRIII (V_{DDQ} = 1.5V) power supply. The pin should be connect to VDD for DDRII (V_{DDQ} = 1.8V) power supply or be connected to a resistive voltage divider from VDDQ to GND to adjust the output of PWM from 0.75V to 3.3V.
10	S3	S3 Signal Input.
11	S5	S5 Signal Input
12	TON	The pin is used to set the UGATE on time through a pull-up resistor connecting to V_{IN}.
13	PGOOD	Power-Good Open-Drain Output. This pin will be in HIGH state when VDDQ output voltage is within the target range.
14	VDD	Supply Input for the Analog Supply.
15	VDDP	Supply Input for the Low Gate Driver.
16	CS	Current Limit Threshold Setting Input. Connect this pin to VDD through the voltage setting resistor.
18	PGND	Power Ground for Low-Side MOSFET.
19	LGATE	Low-Side Gate Driver Output for VDDQ.
20	PHASE	External Inductor Connection for VDDQ and it behaves as the current sense comparator input for Low-Side MOSFET $R_{DS(ON)}$ sensing.
21	UGATE	High-Side Gate Driver Output for VDDQ.
22	BOOT	Boost Flying Capacitor Connection for VDDQ.
23	VLDOIN	Power Supply for the VTT_LDO.
24	VTT	Power Output for the VTT_LDO

Absolute Maximum Ratings (Note 1)

- Input Voltage, TON to GND ---------- –0.3V to 32V
- BOOT to GND ---------- –0.3V to 38V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - <20ns ---------- –8V to 38V
- PHASE to BOOT ---------- –6V to 0.3V
- VDD, VDDP, CS, MODE, S3, S5, VTTSNS, VDDQ, DEM to GND ---------- –0.3V to 6V
- VTTREF, VTT, VLDOIN, FB, PGOOD to GND ---------- –0.3V to 6V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –2.5V to 7.5V
- PGND, VTTGND to GND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-24L 4x4 ---------- 1.923W
- Package Thermal Resistance (Note 2)
  - WQFN-24L 4x4, θ_{JA} ---------- 52°C/W
  - WQFN-24L 4x4, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 2.5V to 26V
- Control Voltage, V_{DDP}, V_{DD} ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DDP} = V_{DD} = 5V, V_{IN} = 15V, DEM = V_{DD} , R_{TON} = 1MΩ, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
Quiescent Supply Current (VDD + VDDP)		FB forced above the regulation point, V_{S5} = 5V, V_{S3} = 0V	--	470	1000	μA
TON Operating Current		R_{TON} = 1MΩ	--	15	--	μA
I_{VLDOIN} BIAS Current		V_{S5} = V_{S3} = 5V, V_{TT} = No Load	--	1	--	μA
I_{VLDOIN} Standby Current		V_{S5} = 5V, V_{S3}= 0, V_{TT} = No Load	--	0.1	10	μA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown current (V_{S5} = V_{S3} = 0V)		V_{DD} + V_{DDP}	--	0.1	10	µA
		TON	--	0.1	5	
		S3/S5/DEM = 0V	–1	0.1	1	
		I_{VLDOIN}	--	0.1	1	
FB Reference Voltage	V_{REF}	V_{DD} = 4.5V to 5.5V	0.742	0.75	0.758	V
Fixed VDDQ Output Voltage		FB = GND	--	1.5	--	V
		FB = V_{DD}	--	1.8	--	
FB Input Bias Current		FB = 0.75V	–1	0.1	1	µA
VDDQ Voltage Range			0.75	–	3.3	V
On-Time, V_{IN} = 15V		R_{TON} = 1MΩ	267	334	401	ns
Minimum Off-Time			250	400	550	ns
VDDQ Input Resistance			--	100	--	kΩ
VDDQ Shutdown Discharge Resistance		V_{S5} = GND	--	15	--	Ω
Current Sensing						
CS Sink Current		V_{CS} > 4.5V, After UV Blank Time	9	10	11	µA
Current Comparator Offset		GND – PHASE	–15	–	15	mV
Zero Crossing Threshold		PHASE – GND, DEM = 5V	–10	–	5	mV
Fault Protection						
Current Limit (Positive)		GND – PHASE, R_{CS} = 5kΩ	35	50	65	mV
		GND – PHASE, R_{CS} = 20kΩ	170	200	230	mV
Output UV Threshold			60	70	80	%
OVP Threshold		With respect to error comparator threshold	10	15	20	%
OV Fault Delay		FB forced above OV threshold	--	20	--	µs
VDDP Under voltage Lockout Threshold		Rising edge, hysteresis = 20mV, PWM disabled below this level	3.9	4.2	4.5	V
Current Limit Step Time at Soft Start		Each step	--	128	--	clks
UV Blank Time		From S5 signal going high	--	512	--	clks
Thermal Shutdown		Hysteresis = 10°C	--	165	--	°C
Driver On-Resistance						
UGATE Gate Driver (pull up)		(BOOT – PHASE) forced to 5V	--	2	4	Ω
UGATE Gate Driver (sink)		(BOOT – PHASE) forced to 5V	--	1	3	Ω
LGATE Gate Driver (pull up)		LGATE, High State (source)	--	2.5	6	Ω
LGATE Gate Driver (pull down)		LGATE, Low State (sink)	--	0.6	1.5	Ω
UGATE Gate Driver Source/Sink Current		UGATE forced to 2.5V, (BOOT – PHASE) forced to 5V	--	1	--	A
LGATE Gate Driver Source Current		LGATE Forced to 2.5V	--	1	--	A
LGATE Gate Driver Sink Current		LGATE Forced to 2.5V	--	3	--	A
Dead Time		LGATE Rising (PHASE = 1.5V)	--	40	--	ns
		UGATE Rising	--	40	--	
Internal boost charging switch on resistance		VDDP to BOOT, 10mA	--	–	80	Ω

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic I/O						
Logic Input Low Voltage		S3, S5, DEM Low	--	--	0.8	V
Logic Input High Voltage		S3, S5, DEM High	2	--	--	V
Logic Input Current		S3/S5/DEM = VDD/GND	−1	0	1	μA
PGOOD (upper side threshold decide by OV threshold)						
Trip Threshold (falling)		Measured at FB, with respect to reference, no load. Hysteresis = 3%	−13	−10	−7	%
Fault Propagation Delay		Falling edge, FB forced below PGOOD trip threshold	--	2.5	--	μs
Output Low Voltage		I_{SINK} = 1mA	--	--	0.4	V
Leakage Current		High state, forced to 5.0V	--	--	1	μA
VTT LDO T_A = 25°C, Unless Otherwise specification						
VTT Output Tolerance	V_{VTTTOL}	V_{DDQ} = V_{LDOIN} = 1.5V/1.8V, $\lvert I_{VTT} \rvert$ = 0A	−20	--	+20	mV
		V_{DDQ} = V_{LDOIN} = 1.5V/1.8V, $\lvert I_{VTT} \rvert$ = 1A	−30	--	+30	
		V_{DDQ} = V_{LDOIN} = 1.5V/1.8V, $\lvert I_{VTT} \rvert$ = 2A,	−40	--	+40	
VTT Source Current Limit	$I_{VTTOCLSRC}$	$VTT = \left(\frac{V_{DDQ}}{2}\right) \times 0.95$, PGOOD = High	3	--	6	A
		VTT = 0V	--	2	--	
VTT Sink Current Limit	$I_{VTTOCLSNK}$	$VTT = \left(\frac{V_{DDQ}}{2}\right) \times 1.05$ PGOOD = High	3	--	6	A
		VTT = VDDQ	--	2	--	
VTT Leakage Current	I_{VTTLK}	S5 = 5V, S3 = 0V, $VTT = \left(\frac{V_{DDQ}}{2}\right)$	−10	--	10	μA
VTTFB Leakage Current	$I_{VTTSNSLK}$	I_{SINK} = 1mA	−1	--	1	μA
VTT Discharge Current	I_{DSCHRG}	V_{DDQ} = 0V, VTT = 0.5V, S5 = S3 = 0V	10	30	--	mA
VTTREF Output Voltage	V_{VTTREF}	$V_{VTTREF} = \left(\frac{V_{DDQ}}{2}\right)$	--	0.9/0.75	--	V
VDDQ/2, VTTREF Output Voltage Tolerance	$V_{VTTREFTOL}$	V_{LDOIN} = V_{DDQ} = 1.5V, $\lvert I_{VTTREF} \rvert$ < 10mA	−15	--	+15	mV
		V_{LDOIN} = V_{DDQ} = 1.8V, $\lvert I_{VTTREF} \rvert$ < 10mA	−18	--	+18	
VTTREF Source Current Limit	$I_{VTTREFOCL}$	V_{VTTREF} = 0V	10	40	80	mA

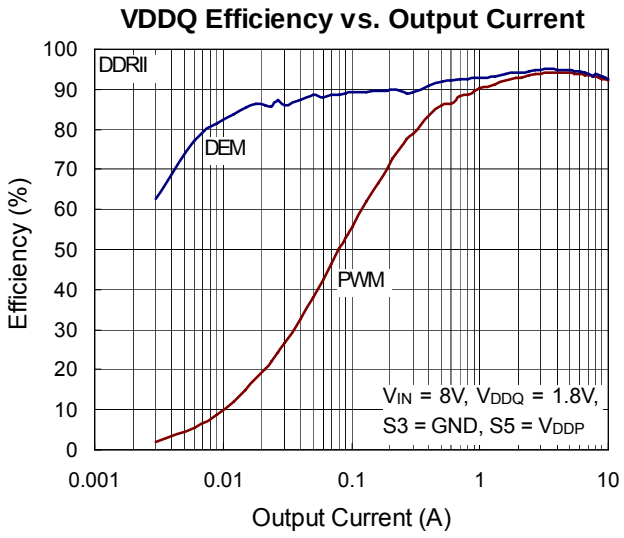
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

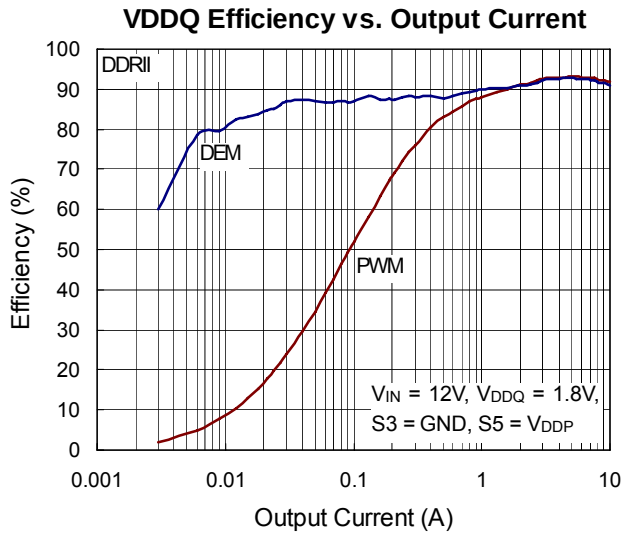
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective 4 layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the WQFN package.

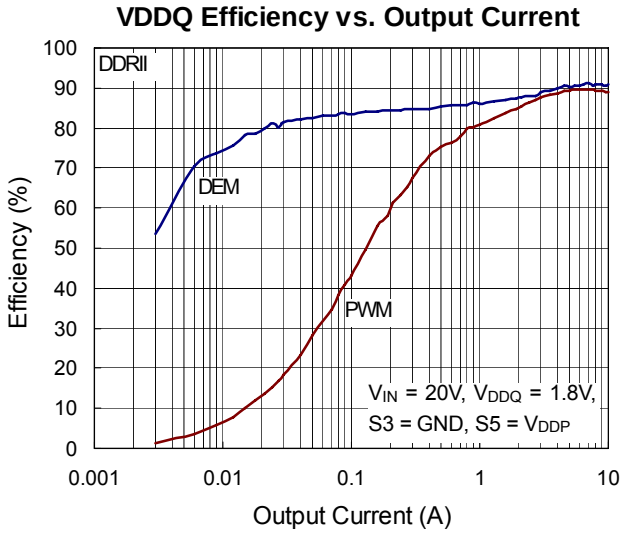
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

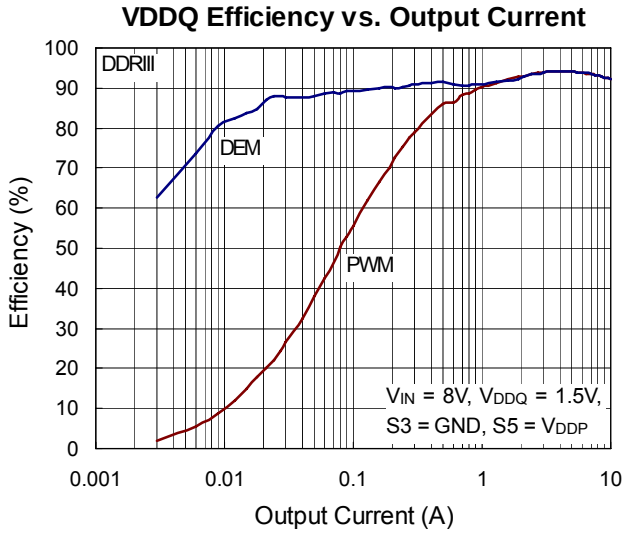
Note 4. The device is not guaranteed to function outside its operating conditions.

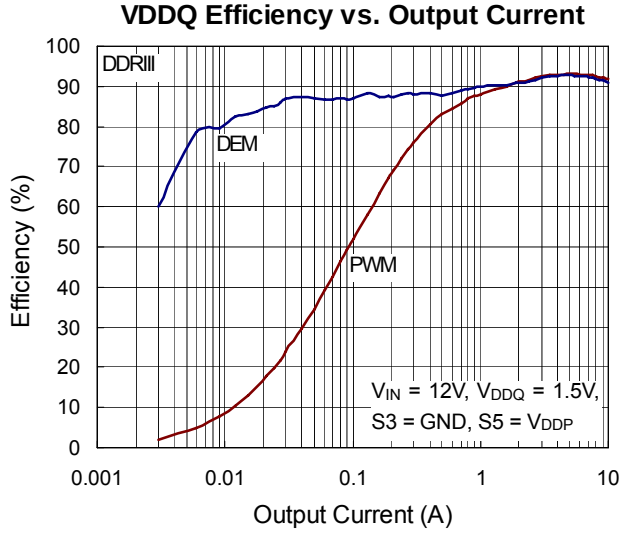
Typical Operating Characteristics

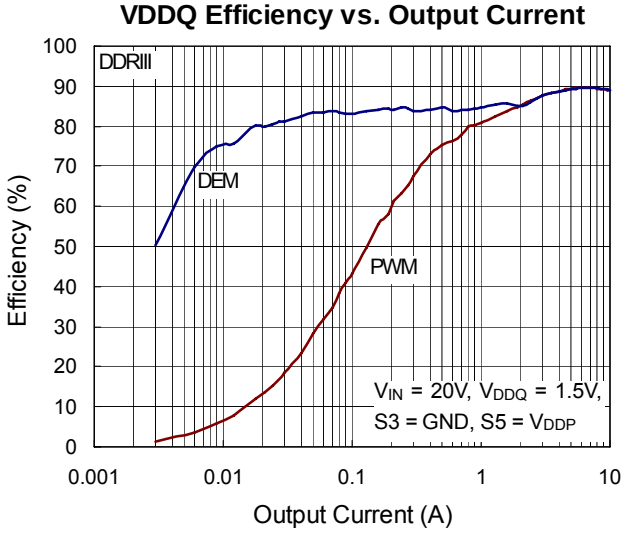




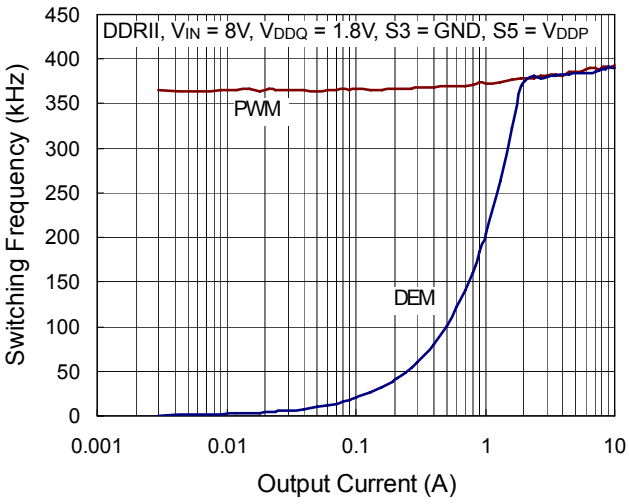








Switching Frequency vs. Output Current



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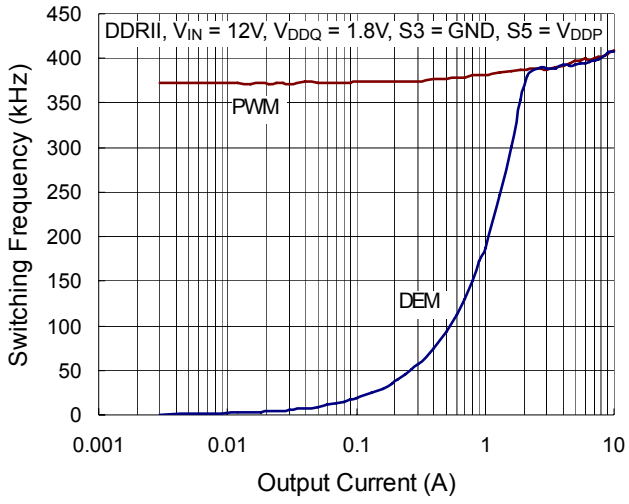

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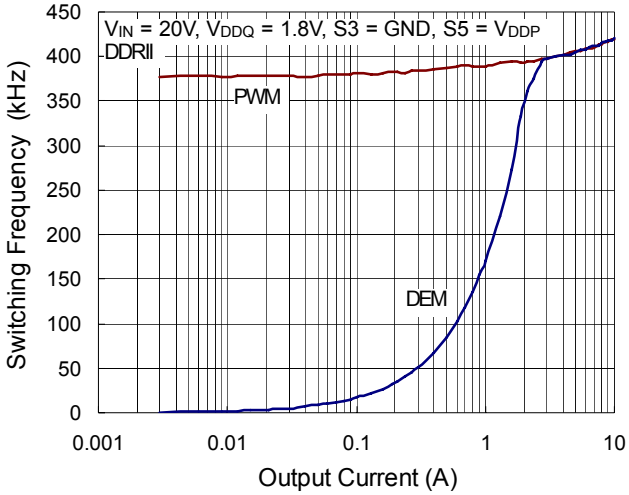

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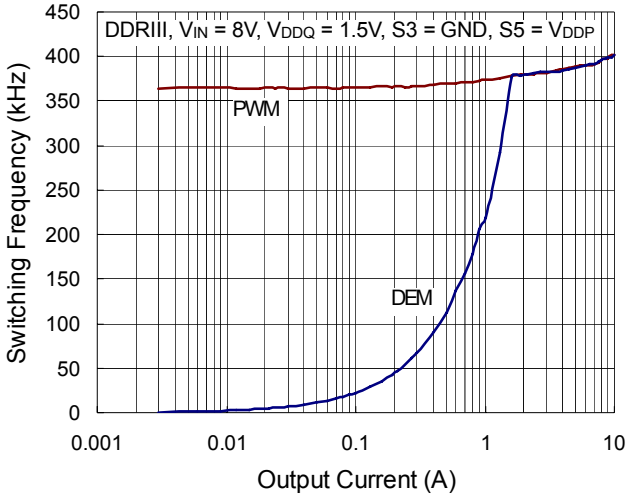

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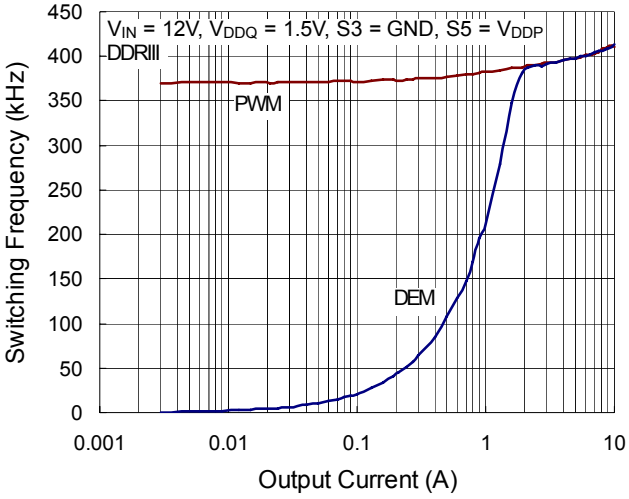

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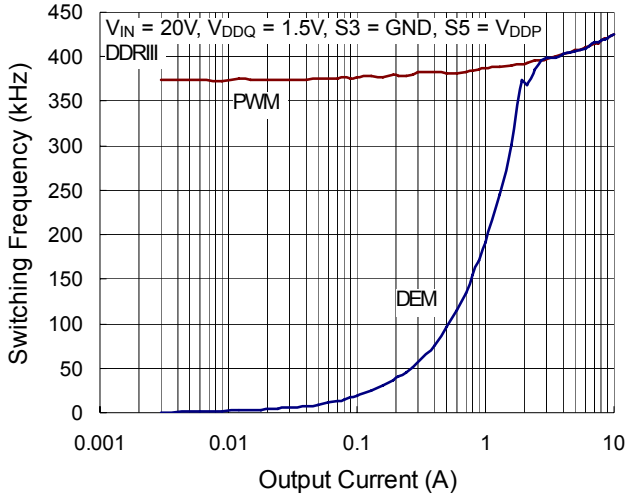
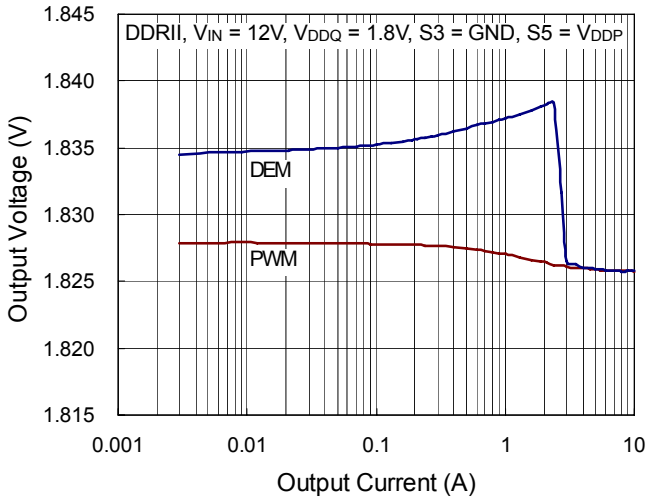
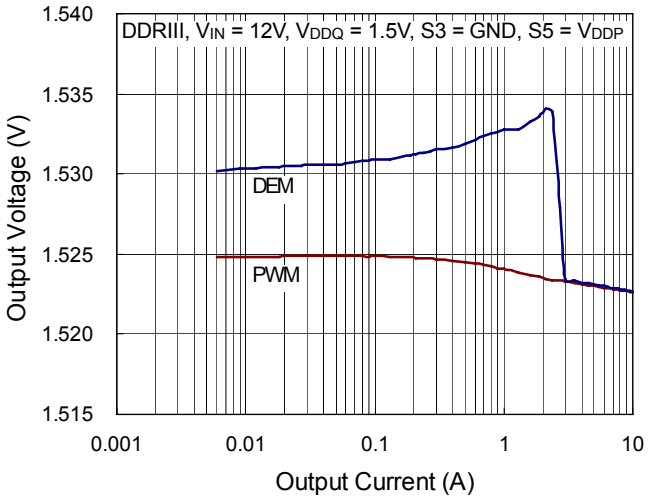


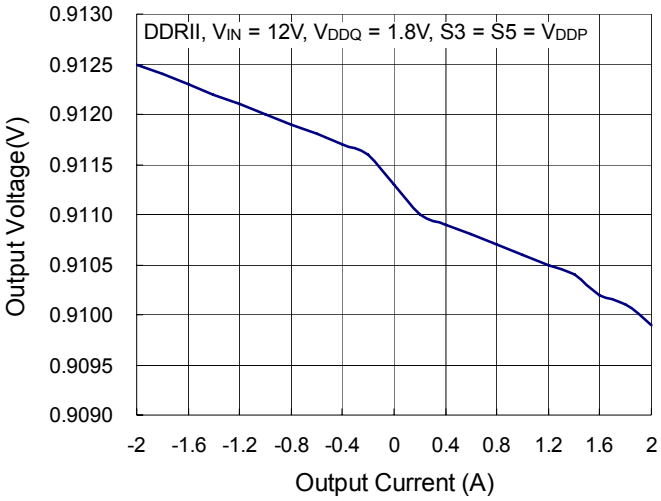
VDDQ Output Voltage vs. Output Current



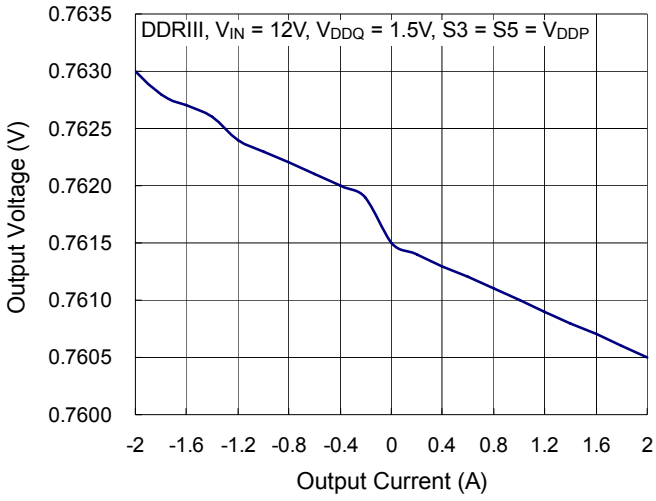
VDDQ Output Voltage vs. Output Current



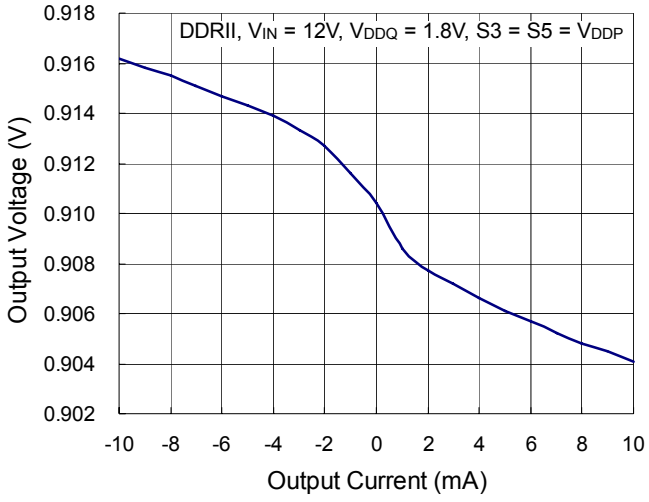
VTT Output Voltage vs. Output Current



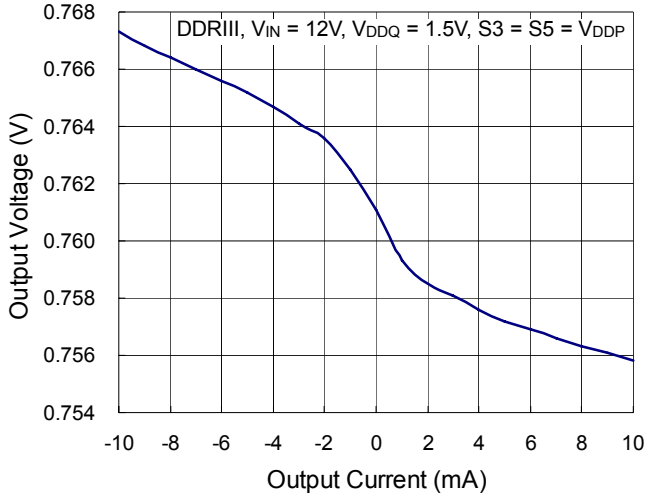
VTT Output Voltage vs. Output Current



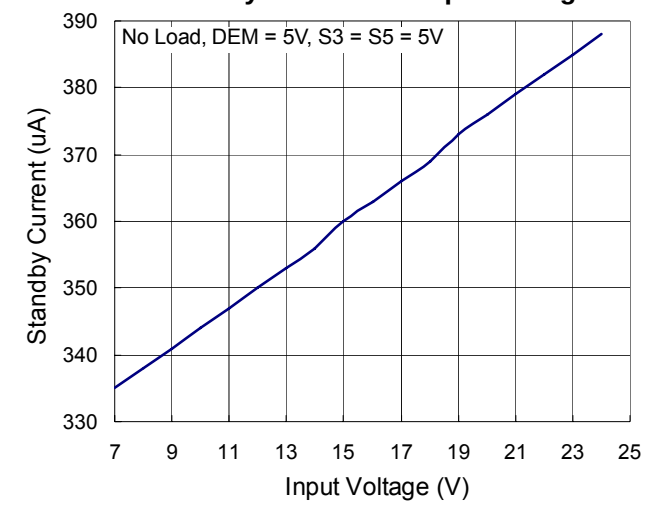
VTTREF Output Voltage vs. Output Current



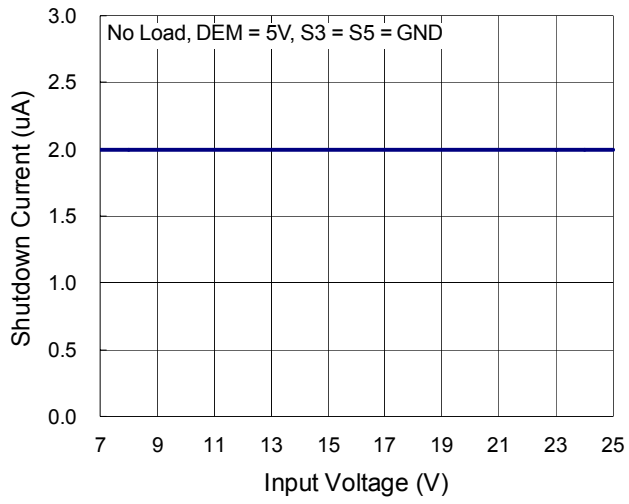
VTTREF Output Voltage vs. Output Current



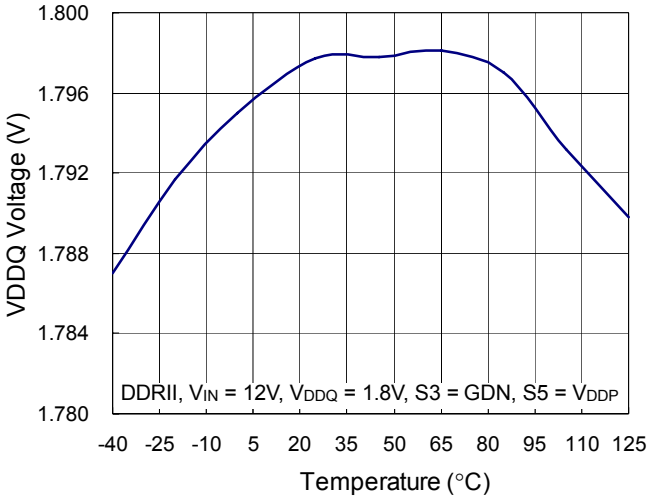
Standby Current vs. Input Voltage



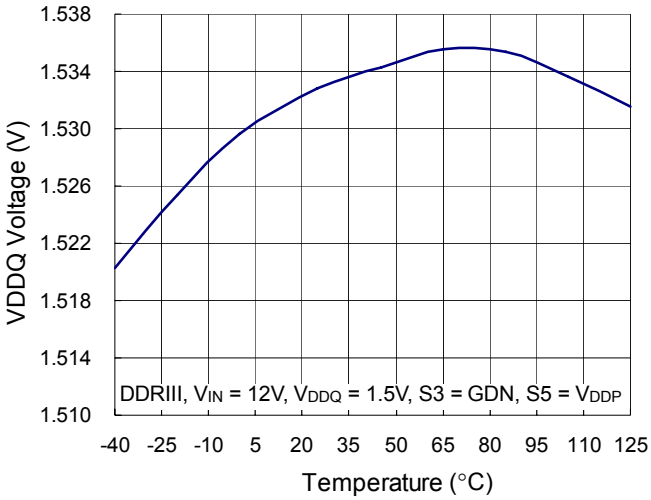
Shutdown Current vs. Input Voltage



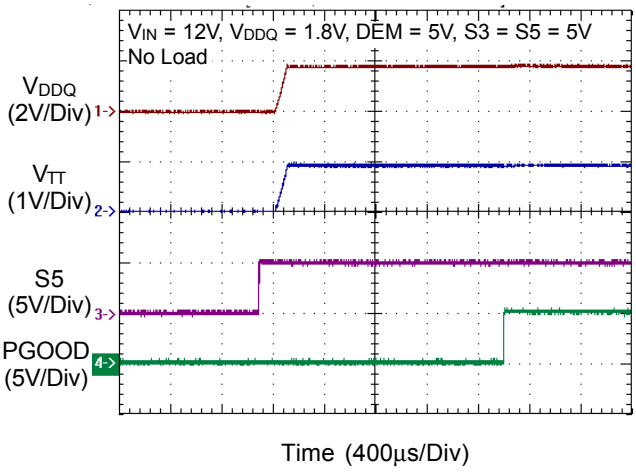
VDDQ Voltage vs. Temperature



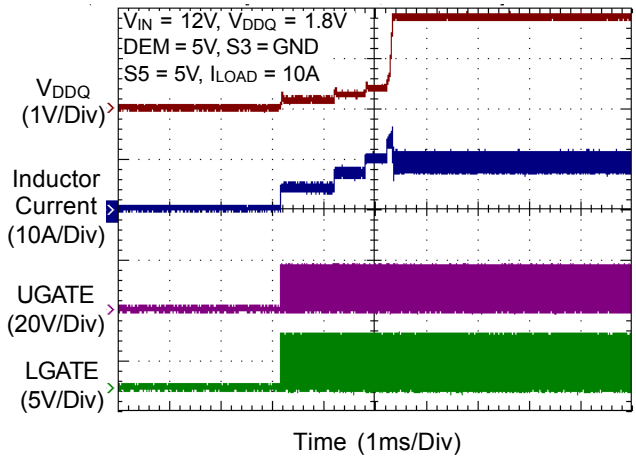
VDDQ Voltage vs. Temperature



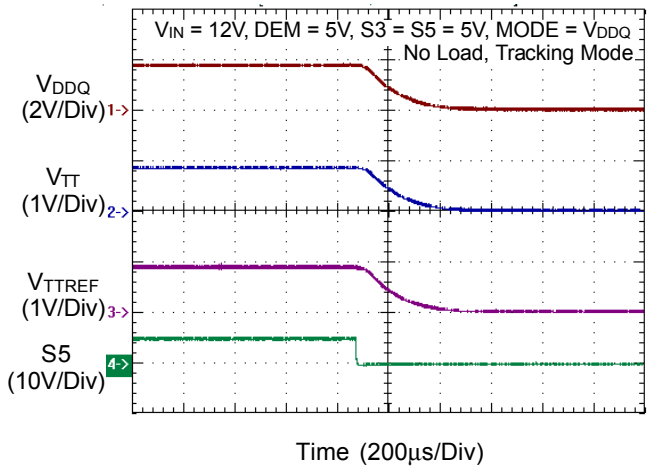
VDDQ and VTT Start Up



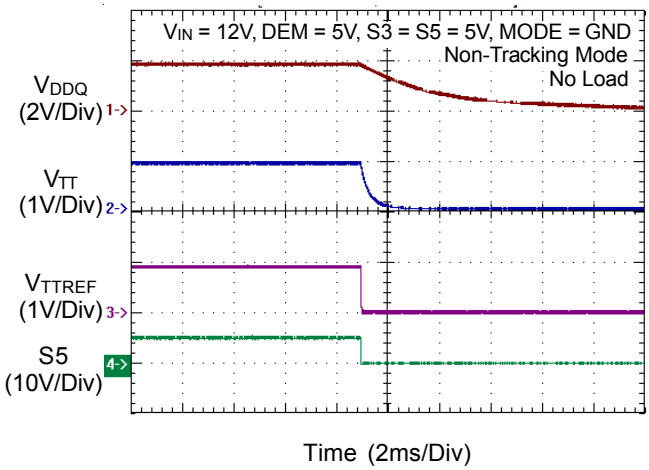
VDDQ Start Up



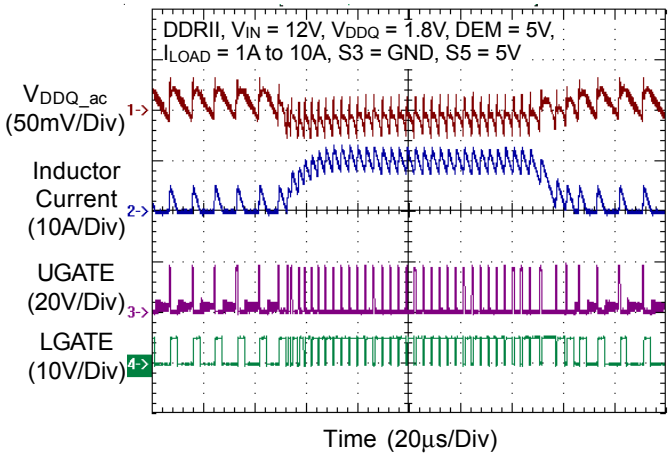
Shutdown



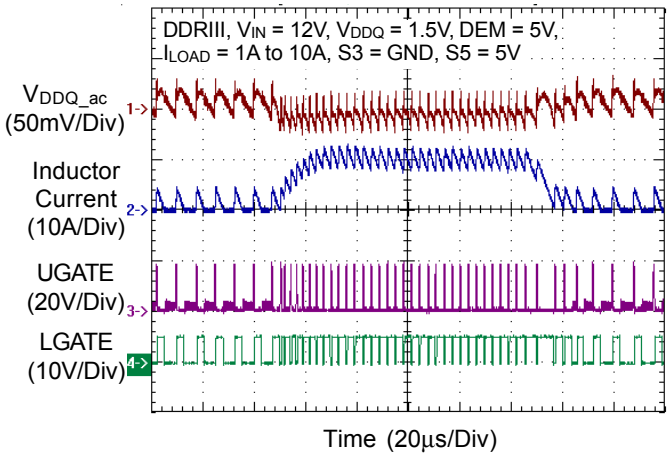
Shutdown



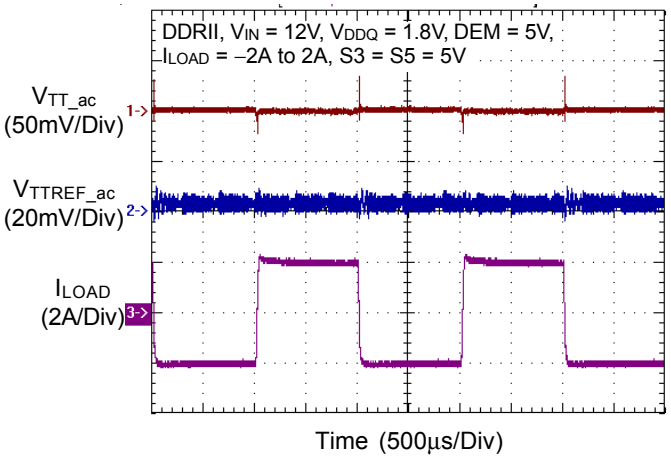
VDDQ Load Transient Response



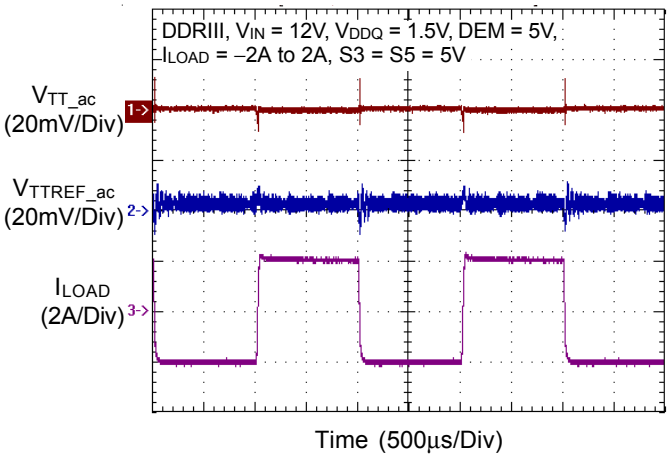
VDDQ Load Transient Response



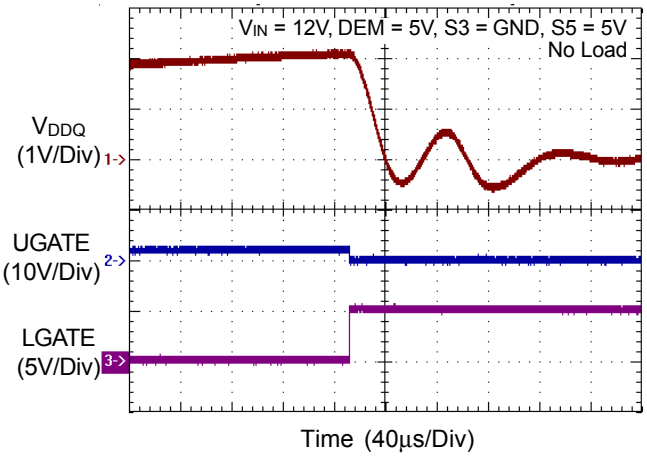
VTT Load Transient Response



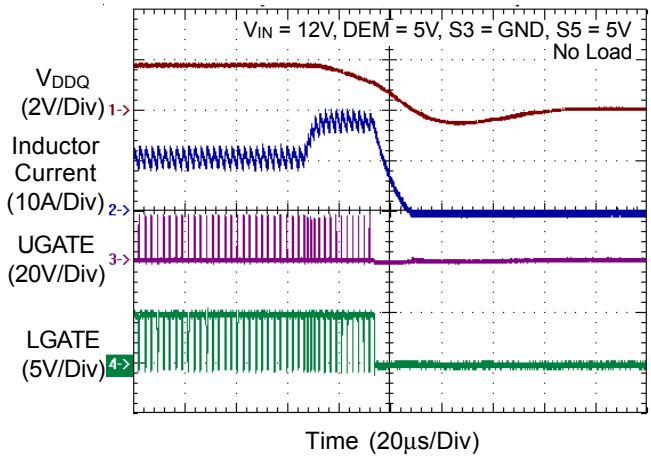
VTT Load Transient Response



OVP


VIN = 12V, DEM = 5V, S3 = GND, S5 = 5V
No Load
VDDQ
(1V/Div)
1->
UGATE
(10V/Div)
2->
LGATE
(5V/Div)
3->
Time (40µs/Div)

UVP


VIN = 12V, DEM = 5V, S3 = GND, S5 = 5V
No Load
VDDQ
(2V/Div)
1->
Inductor
Current
(10A/Div)
2->
UGATE
(20V/Div)
3->
LGATE
(5V/Div)
4->
Time (20µs/Div)

Application Information

The RT8207 PWM controller provides the high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high-voltage batteries to generate low-voltage chipset RAM supplies in notebook computers. Richtek's Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant- off-time PWM schemes. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

The 3A sink/source LDO maintains fast transient response only requiring 20μF of ceramic output capacitance. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The RT8207 supports all of the sleep state controls placing VTT at high-Z in S3 and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. Refer to the function diagrams of the RT8207, the synchronous high-side MOSFET will be tuned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET will be turned off. The pulse width of this one shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

On-Time Control (T_{ON})

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it into a current. This input voltage-proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VDDQ, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. The implementation results in a nearly constant switching frequency without the need of a clock generator.

T_{ON} = 3.85p x R_{TON} x V_{DDQ} / (V_{IN} – 0.5)

And then the switching frequency is :

f = V_{DDQ} / (V_{IN} x T_{ON})

R_{TON} is a resistor connected from the input supply (V_{IN}) to the TON pin.

Mode Selection (DEM) Operation

The DEM pin enables the supply. When the DEM pin is connected to VDD, the controller will be enabled and operated in diode-emulation mode. When the DEM pin is connected to GND, the RT8207 will operate in forced-CCM mode.

Diode-Emulation Mode (DEM = VDDP)

In diode-emulation mode, the RT8207 automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of the frequency is achieved smoothly and without increasing VDDQ ripple or load regulation. As the output current decreases from heavy-load condition, the inductor current will also be reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low-side MOSFET allows only partial of negative current when the inductor freewheeling current reaches negative. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level than requires the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conducting condition. The transition load point to the light-load operation can be calculated as follows (Figure 1) :

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{DDQ})}{2L} \times T_{ON}$$

where T_{ON} is On-time.

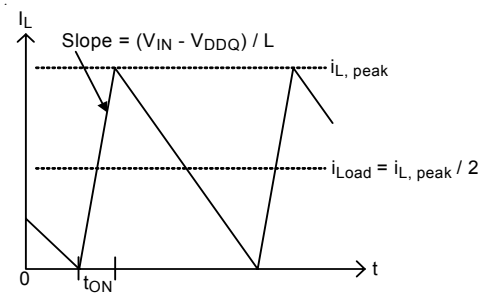


Figure 1. Boundary condition of CCM/DCM

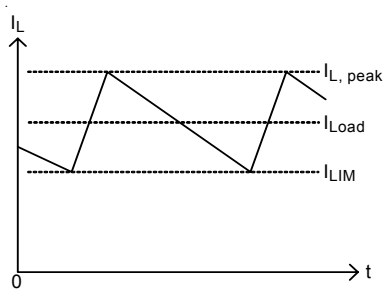


Figure 2. "valley" Current -Limit

The switching waveforms may appear noisy and asynchronous when light loading causes diode-emulation operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in DEM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degrades load-transient response (especially at low input-voltage levels).

Forced-CCM Mode (DEM = GND)

The low-noise, Forced-CCM mode (DEM = GND) disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop maintains a duty ratio of V_{DDQ}/V_{IN}. The benefit of Forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost : The no-load battery current can be up to 10mA to 40mA, depending on the external MOSFETs.

Current-Limit Setting for VDDQ (CS)

The RT8207 provides cycle-by-cycle current limiting control. The current-limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current-sense signal at the PHASE pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 2). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and battery and output voltage.

The RT8207 uses the on-resistance of the synchronous rectifier as the current-sense element. Use the worse-case maximum value for $R_{DS(ON)}$ from the MOSFET datasheet, and add a margin of 0.5%/°C for the rise in $R_{DS(ON)}$ with temperature.

The R_{ILIM} setting resistor between CS pin and VDD sets the current limit threshold. The resistor R_{ILIM} is connected to a 10μA current source from the CS pin. When the voltage drop across the low-side MOSFET equals the voltage across the R_{ILIM} setting resistor, positive current limit will be activated. The high-side MOSFET will not be turned on until the voltage drop across the MOSFET falls below the current limit threshold.

Choose a current limit setting resistor by following equation :

$R_{ILIM} = I_{LIM} \times R_{DS(ON)} / 10\mu A$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signal seen by the PHASE pin and PGND.

Current Protection for VTT

The LDO has an internally fixed constant over-current limiting of 4.5A while operating at normal condition. This over-current point is reduced to 2A before the output voltage comes within 5% of its set voltage or goes outside of 10% of its set voltage.

MOSFET Gate Driver (UGATE, LGATE)

The high-side driver is designed to drive high-current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver, the 5V bias voltage will be delivered from the VDDP supply. The average drive current is proportional to the gate charge at V_{GS} = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOT and PHASE pins.

A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on.

The low-side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). The internal pull-down transistor that drives LGATE low is robust, with a 0.4Ω typical on-resistance. A 5V bias voltage is delivered from VDDP supply. The instantaneous drive current is supplied by the flying capacitor between VDDP and PGND.

For high-current applications, some combinations of high- and low-side MOSFETs might be encountered that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with the BOOT pin, which increases the turn-on time of the high-side MOSFET without degrading the turn-off time (Figure 3).

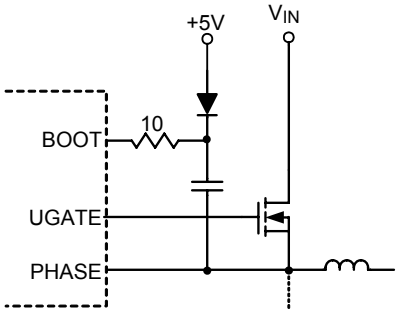


Figure 3. Reducing the UGATE Rise Time

Power-Good Output (PGOOD)

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 15% above or 10% below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to within these tolerances once more. In soft start, the PGOOD pin will be actively held low and is allowed to transition high until soft start is over and the output reaches 93% of its set voltage. There is a 2.5μs delay built into PGOOD circuitry to prevent the false transition.

UVLO Protection

The RT8207 has a VDDP supply under-voltage lockout protection (UVLO). When the VDDP voltage is lower than 4.3V (typ.), VDDQ, VTT and VTTREF will be shut off. This is a non-latch protection.

Soft-Start

A build-in soft-start of VDDQ is used to prevent surge current from power supply input after S5 is enabled. The maximum allowed current limit is segmented in 4 steps: 25%, 50%, 75% and 100% and each step duration is 128 cycles. The current limit steps can minimize the VDDQ folded-back in the soft-start duration when the fixed or adjustable output is determined by the RT8207.

The soft-start function of the VTT is achieved by the current clamp. The current limit threshold is also changed in two stages using an internal power-good signal dedicated for LDO. During VTT is below the power-good threshold, the current limit level is 2A. This allows the output capacitors to be charged with low and constant current that gives linear ramp up of the output. When the output comes up to the good state, the over-current limit is released to 4.5A.

Output Over voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage protection. When over voltage protection is enabled, if the output exceeds 15% of its set voltage threshold, over voltage protection will be triggered and the LGATE low-side gate drivers will be forced high. This activates the low-side MOSFET switch, which rapidly discharges the output capacitor and reduces the input voltage.

The RT8207 will be latched once the OVP is triggered and can only be released by VDD power-on reset or S5. There is a 20μs delay built into the over voltage protection circuit to prevent false transitions.

Note that LGATE latching high causes the output voltage to dip slightly negative when energy has been previously stored in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the over voltage condition is caused by a short in high-side switch, turning the low-side MOSFET on 100% creates an electrical short between the battery and GND, blowing the fuse and disconnecting the battery from the output.

Output Under voltage Protection (UVP)

The output voltage can be continuously monitored for under

voltage protection. When the under voltage protection is enabled, if the output is less than 70% of its set voltage threshold, the under voltage protection is triggered, then both UGATE and LGATE gate drivers are forced low while entering soft-discharge mode. During soft-start, the UVP will be blanked around 512 cycles.

Thermal Protection

The RT8207 monitors the temperature of itself. If the temperature exceeds the threshold value, +165°C (typ.), the PWM output, VTTREF and VTT will be shut off. The RT8207 is latched once the thermal shutdown is triggered and can only be released by VDD power-on reset or S5.

Output Voltage Setting (FB)

The RT8207 can be used for both of DDR2 (VDDQ = 1.8V) and DDR3 (VDDQ = 1.5V) power supply and it adjustable output voltage (0.75V < VDDQ < 3.3V) by connecting FB pin as shown in Table 1.

Table 1. FB and Output Voltage Setting

FB	VDDQ (V)	VTTREF and VTT	NOTE
VDD	1.8	V_{DDQ}/2	DDR2
GND	1.5	V_{DDQ}/2	DDR3
FB Resistors	Adjustable	V_{DDQ}/2	0.75V < V_{DDQ} < 3.3V

Connect a resistor voltage-divider at the FB between VDDQ and GND to adjust the respective output voltage between 0.75V and 3.3V (Figure 4). Choose R2 to be approximately 10kΩ and solve for R1 using the equation as follows :

$$V_{DDQ} = V_{REF} \times \left[1 + \left(\frac{R1}{R2}\right)\right]$$

where V_{REF} is 0.75V (typ.).

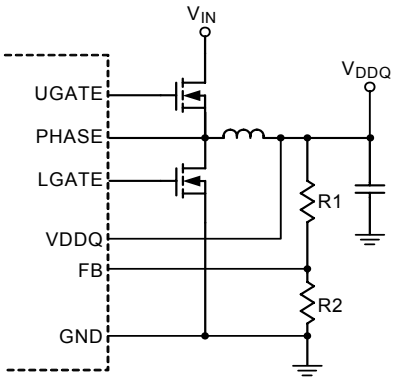


Figure 4. Setting VDDQ with a Resistor-Divider

VTT Linear Regulator and VTTREF

RT8207 integrates high performance low-dropout linear regulator that is capable of sourcing and sinking current up to 3A (VDDQ>= 1.8V). This VTT linear regulator employs ultimate fast response feedback loop so that small ceramic capacitors are enough to keep tracking the VTTREF within 40mV at all conditions including fast load transient. To achieve tight regulation with minimum effect of wiring resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of the VTT output capacitor(s) as a separate trace from the VTT pin. For stable operation, total capacitance of the VTT output terminal can be equal to or greater than 20μF. It is recommended to attach two 10μF ceramic capacitors in parallel to minimize the effect of ESR and ESL. If ESR of the output capacitor is greater than 2mΩ, insert an RC filter between the output and VTTSNS input to achieve loop stability. The RC filter time constant should be almost the same or slightly lower than the time constant made by the output capacitor and its ESR. The VTTREF block consists of on-chip 1/2 divider, LPF and buffer. This regulator also has sink and source capability up to 10mA. Bypass VTTREF to GND by a 33nF ceramic capacitor for stable operation.

Outputs Management by S3 and S5 Control

In DDRII/DDRIII memory applications, it is important to keep VDDQ always higher than VTT/VTTREF including both start-up and shutdown. The RT8207 provides this management by simply connecting both S3 and S5 terminals to the sleep-mode signals such as SLP_S3 and SLP_S5 in notebook PC system. All of VDDQ, VTTREF and VTT are turned on at S0 state (S3 = S5 = high). In S3 state (S3 = low, S5 = high), VDDQ and VTTREF voltages are kept on while VTT is turned off and left at high impedance (high-Z) state. The VTT output is floated and does not sink or source current in this state. In S4/S5 states (S3 = S5 = low), all of the three outputs are disabled. Outputs are discharged to ground according to the discharge mode selected by the MODE pin (see VDDQ and VTT Discharge Control section). Each state code represents as follows; S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF. (See Table 2)

Table 2. S3 and S5 Truth Table

STATE	S3	S5	VDDQ
S0	Hi	Hi	On
S3	Lo	Hi	On
S4/S5	Lo	Lo	Off (Discharge)

STATE	VTTREF	VTT
S0	On	On
S3	On	Off (Hi-Z)
S4/S5	Off (Discharge)	Off (Discharge)

VDDQ and VTT Discharge Control (MODE)

The RT8207 discharge VDDQ, VTTREF and VTT outputs during S3 and S5 are both low. There are two different discharge modes. The discharge mode can be set by connecting MODE pin as shown in Table 3.

Table 3. Discharge Selection

MODE	Discharge Mode
VDD	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

When in tracking discharge mode, the RT8207 discharges outputs through the internal VTT regulator transistors and VTT output tracks half of VDDQ voltage during this discharge. Note that VDDQ discharge current flows via VLDOIN to VTTGND, thus VLDOIN must be connected to VDDQ in this mode. The internal LDO can handle up to 3A and can be dischargeed quickly. After VDDQ is discharged down to 0.15V, the terminal LDO will be turned off and the operation mode will be changed to the non-tracking discharge mode.

When in non-tracking discharge mode, the RT8207 discharges outputs using internal MOSFETs which are connected to VDDQ and VTT. The current capability of these MOSFETs are limited to discharge slowly. Note that VDDQ discharge current flows from VDDQ to GND in this mode. In case of no discharge mode, the RT8207 does not discharge output charge at all.

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or L_{IR}) determine the inductor value as follows :

$$L = \frac{T_{ON} \times (V_{IN} - V_{DDQ})}{L_{IR} \times I_{LOAD(MAX)}}$$

where L_{IR} is the ratio of the peak to peak ripple current to the average inductor current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough to prevent it from saturating at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + [(L_{IR} / 2) \times I_{LOAD(MAX)}]$$

This inductor ripple current also impacts transient-response performance, especially at low VIN–VDDQ differences. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The peak amplitude of the output transient (V_{SAG}) is also a function of the output transient. The V_{SAG} is also features a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (T_{ON} + T_{OFF(MIN)})}{2 \times C_{OUT} \times V_{DDQ} \times \left[V_{IN} \times T_{ON} - V_{DDQ} \times \left(T_{ON} + T_{OFF(MIN)} \right) \right]}$$

Where minimum off-time ($T_{OFF(MIN)}$)=400ns(typical).

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{L_{IR} \times I_{LOAD(MAX)}}$$

where V_{P-P} is the peak-to-peak output voltage ripple.

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

For low input-to-output voltage differentials (VIN/VDDQ < 2), additional output capacitance is required to maintain stability and good efficiency in ultrasonic mode.

The amount of overshoot due to stored inductor energy can be calculated as :

$$V_{SOAR} = \frac{(I_{PEAK})^2 \times L}{2 \times C_{OUT} \times V_{DDQ}}$$

where I_{PEAK} is the peak inductor current.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high-value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high- ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting VDDQ or the FB divider close to the inductor.

Unstable operation manifests itself in two related and distinctly different ways: double-pulsing and feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can trip the over-voltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under- or over-shoot.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8207, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-24L 4x4 packages, the thermal resistance θ_{JA} is 54°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (52°C/W) = 1.923W for WQFN-24L 4x4 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8207 packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

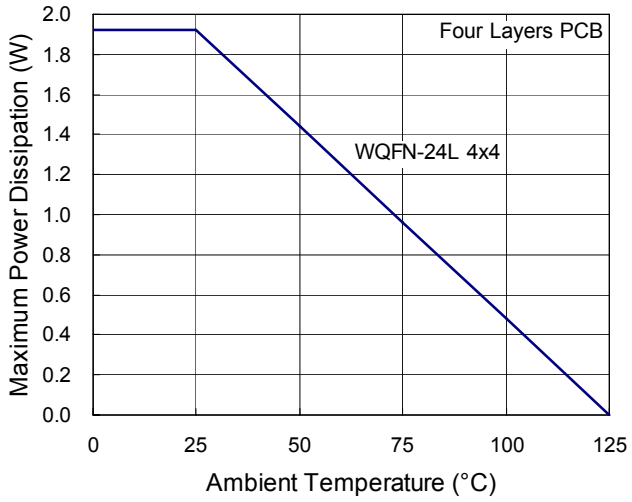


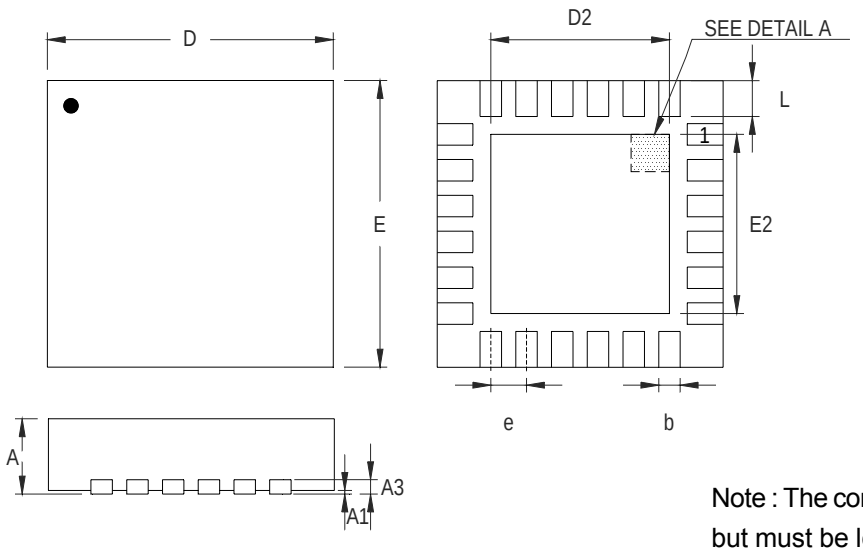
Figure 5. Derating Curves for RT8207 Packages

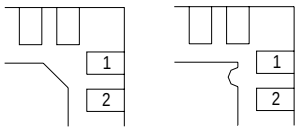
Layout Considerations

Layout is very important in high frequency switching converter design. If the IC is designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout for the RT8207.

- Connect an RC low-pass filter from VDDP to VDD, 1μF and 5.1Ω are recommended. Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VDDQ, FB, PGND, DEM, PGOOD, CS, VDD, and TON should be placed away from high-voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- VLDOIN should be connected to VDDQ output with short and wide trace. If different power source is used for VLDOIN, an input bypass capacitor should be placed to the pin as close as possible with short and wide trace.
- The output capacitor for VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between GND pin and the output capacitor(s).
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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