4V Drive Nch+Nch MOS FET

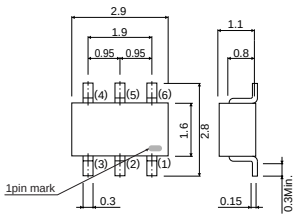
SM6K2

●Structure
Silicon N-channel
MOSFET transistor

●Features
1) Two RHU002N06 chips in a SMT package.
2) Mounting possible with SMT3 automatic mounting machines.
3) Transistor elements are independent, eliminating mutual interference.
4) Mounting cost and area can be cut in half.

●External dimensions (Unit : mm)

SMT6



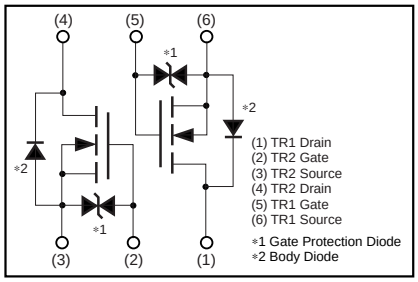
Each lead has same dimensions

Abbreviated symbol : K2

●Packaging specifications

Type	Package	Taping
	Code	T110
	Basic ordering unit (pieces)	3000
SM6K2		○

●Equivalent circuit



∗ A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use.
Use the protection circuit when fixed voltages are exceeded.

●Absolute maximum ratings (Ta=25°C)
<It is the same ratings for the Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	60	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	200	mA
	Pulsed	I_{DP} ∗1	800	mA
Drain reverse current	Continuous	I_{DR}	200	mA
	Pulsed	I_{DRP} ∗1	800	mA
Total power dissipation		P_D ∗2	300	mW / TOTAL
			200	mW / ELEMENT
Channel temperature		Tch	150	°C
Storage temperature		Tstg	−55 to +150	°C

∗1 Pw≤10µs, Duty cycle≤1%
∗2 With each pin mounted on the recommended lands.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a) ∗	416.7	°C / W / TOTAL
		625	°C / W / ELEMENT

∗ With each pin mounted on the recommended lands.

●**Electrical characteristics** (Ta=25°C)
<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate leakage current	I_{GSS}	–	–	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	60	–	–	V	I_D=1mA, V_{GS}=0V
Drain cutoff current	I_{DSS}	–	–	1	μA	V_{DS}=60V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1	–	2.5	V	V_{DS}=10V, I_D=1mA
Drain-source on-state resistance	$R_{DS\ (on)}$ *	–	1.7	2.4	Ω	I_D=200mA, V_{GS}=10V
		–	2.8	4.0		I_D=200mA, V_{GS}=4V
Forward transfer admittance	$\|Y_{fs}\|$ *	0.1	–	–	S	V_{DS}=10V, I_D=200mA
Input capacitance	C_{iss}	–	15	–	pF	V_{DS}=10V V_{GS}=0V f=1MHz
Output capacitance	C_{oss}	–	8	–	pF	
Reverse transfer capacitance	C_{rss}	–	4	–	pF	
Turn-on delay time	$t_{d\ (on)}$ *	–	6	–	ns	I_D=100mA, V_{DD}≒30V V_{GS}=10V R_L=300Ω R_G=10Ω
Rise time	t_r *	–	5	–	ns	
Turn-off delay time	$t_{d\ (off)}$ *	–	12	–	ns	
Fall time	t_f *	–	95	–	ns	
Total gate charge	Q_g *	–	2.2	4.4	nC	V_{DD}≒30V V_{GS}=10V I_D=200mA
Gate-source charge	Q_{gs} *	–	0.6	–	nC	
Gate-drain charge	Q_{gd} *	–	0.3	–	nC	

* Pulsed

●**Body diode characteristics** (Source-drain) (Ta=25°C)
<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	–	–	1.2	V	I_S=200mA, V_{GS}=0V

●**Electrical characteristic curves**

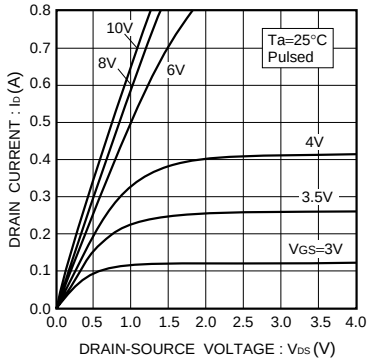


Fig.1 Typical output characteristics

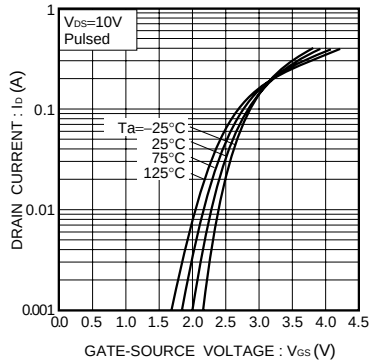


Fig.2 Typical transfer characteristics

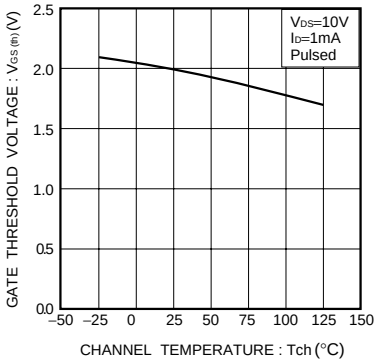


Fig.3 Gate threshold voltage vs. channel temperature

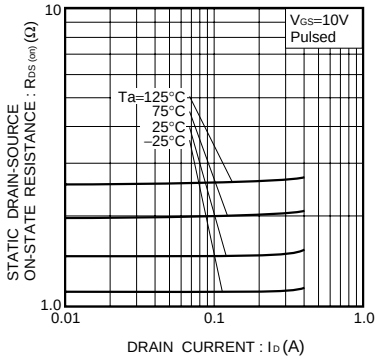


Fig.4 Static drain-source on-State resistance vs. drain current (I)

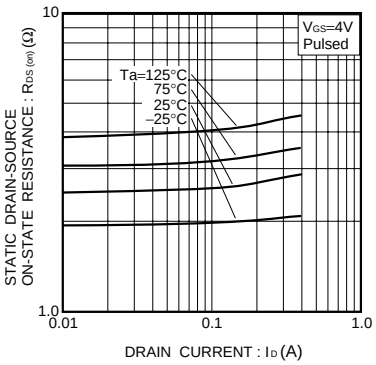


Fig.5 Static drain-source on-state resistance vs. drain current (II)

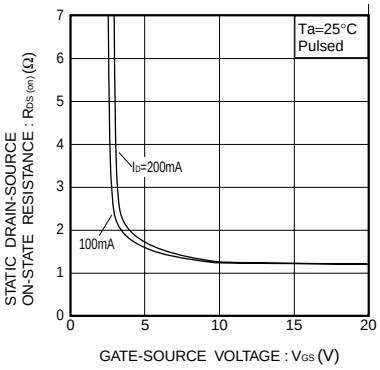


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

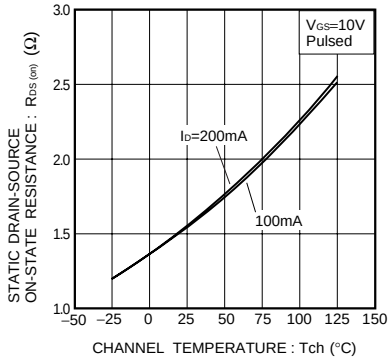


Fig.7 Static drain-source on-state resistance vs. channel temperature

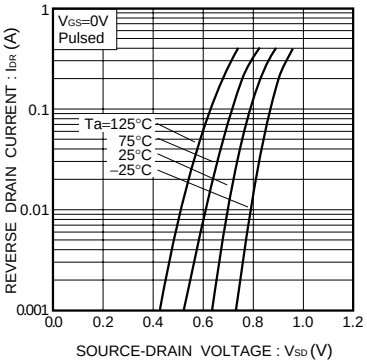


Fig.8 Reverse drain current vs. source-drain voltage (I)

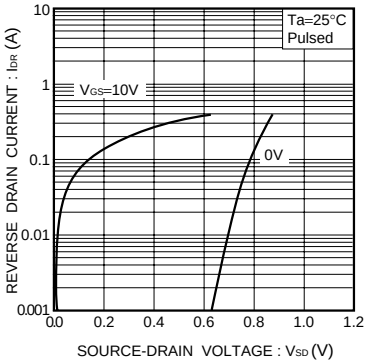


Fig.9 Reverse drain current vs. source-drain voltage (II)

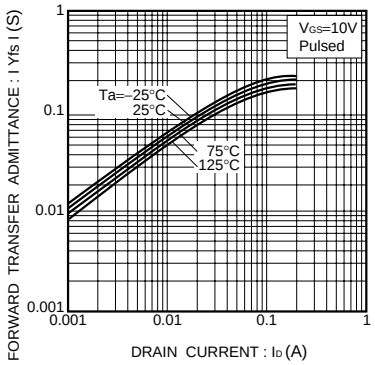


Fig.10 Forward transfer admittance vs. drain current

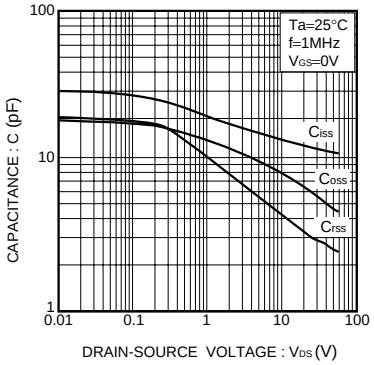


Fig.11 Typical capacitance vs. drain-source voltage

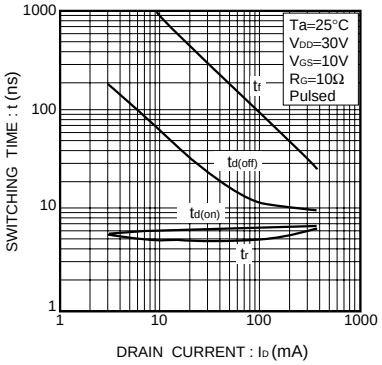


Fig.12 Switching characteristics

●Switching characteristics measurement circuit

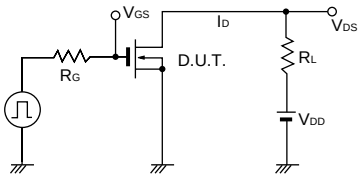


Fig.13 Switching time test circuit

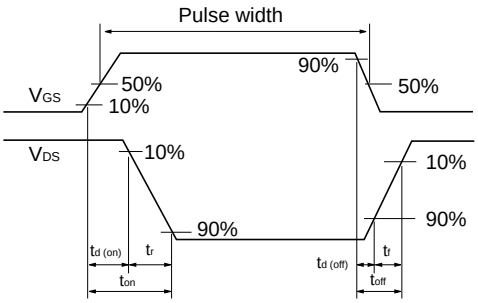


Fig.14 Switching time waveforms

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