

## OptiMOS® Power-Transistor

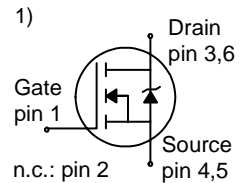
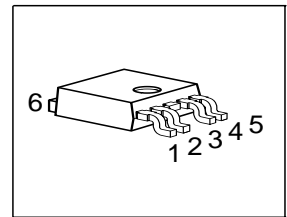
### Feature

- N-Channel
- Enhancement mode
- Logic Level
- Excellent Gate Charge x  $R_{DS(on)}$  product (FOM)
- Superior thermal resistance
- 175°C operating temperature
- Avalanche rated
- dv/dt rated

### Product Summary

$V_{DS}$	30	V
$R_{DS(on)}$	4.2	mΩ
$I_D$	100	A

P-TO252-5-1



Type	Package	Ordering Code	Marking
SPD100N03S2L-04	P-TO252-5-1	Q67042-S4128	PN03L04

### Maximum Ratings, at $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current $T_C=25\text{ °C}^2)$ $T_C=100\text{ °C}$	$I_D$	100 100	A
Pulsed drain current $T_C=25\text{ °C}$	$I_{D\text{ puls}}$	400	
Avalanche energy, single pulse $I_D=80\text{ A}$ , $V_{DD}=25\text{ V}$ , $R_{GS}=25\text{ Ω}$	$E_{AS}$	325	mJ
Avalanche energy, periodic limited by $T_{jmax}$	$E_{AR}$	15	
Reverse diode dv/dt $I_S=100\text{ A}$ , $V_{DS}=24\text{ V}$ , $di/dt=200\text{ A/μs}$ , $T_{jmax}=175\text{ °C}$	dv/dt	6	kV/μs
Gate source voltage	$V_{GS}$	±20	V
Power dissipation $T_C=25\text{ °C}$	$P_{tot}$	150	W
Operating and storage temperature	$T_j, T_{stg}$	-55... +175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	

**Thermal Characteristics**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Characteristics</b>					
Thermal resistance, junction - case	$R_{thJC}$	-	-	1	K/W
SMD version, device on PCB:	$R_{thJA}$				
@ min. footprint		-	-	75	
@ 6 cm <sup>2</sup> cooling area <sup>3)</sup>		-	-	50	

**Electrical Characteristics**, at  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Static Characteristics</b>					
Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$	$V_{(BR)DSS}$	30	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D = 100\ \mu A$	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current $V_{DS}=30V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=30V, V_{GS}=0V, T_j=125^\circ C$	$I_{DSS}$	-	0.01 10	1 100	$\mu A$
Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$	$I_{GSS}$	-	1	100	
Drain-source on-state resistance $V_{GS}=4.5V, I_D=50A$	$R_{DS(on)}$	-	5	6.3	$m\Omega$
Drain-source on-state resistance $V_{GS}=10V, I_D=50A$	$R_{DS(on)}$	-	3.4	4.2	

<sup>1</sup>pin 1 and 2 have to be connected together on the PCB as well as pin 4 and 5.

<sup>2</sup>Current limited by bondwire and calculated with max. source pin temperature of 85°C; with a  $R_{thJC} = 1K/W$  the chip is able to carry  $I_D = 146A$ .

<sup>3</sup>Device on 40mm\*40mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70  $\mu m$  thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics, at  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic Characteristics**

Transconductance	$g_{fs}$	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$ , $I_D = 100\text{A}$	59	118	-	S
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$	-	2590	3450	pF
Output capacitance	$C_{oss}$		-	1025	1360	
Reverse transfer capacitance	$C_{rss}$		-	205	310	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{V}$ , $V_{GS} = 10\text{V}$ , $I_D = 50\text{A}$ , $R_G = 2.7\Omega$	-	12	18	ns
Rise time	$t_r$		-	245	365	
Turn-off delay time	$t_{d(off)}$		-	45	67	
Fall time	$t_f$		-	24	36	

**Gate Charge Characteristics**

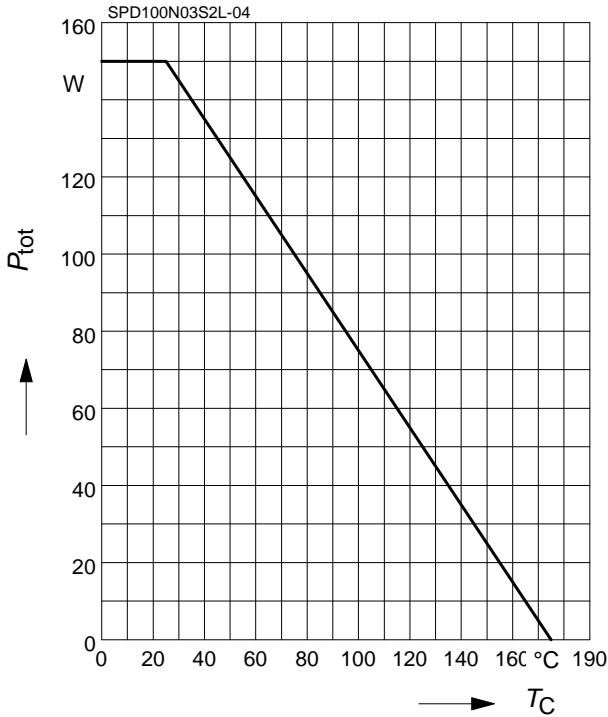
Gate to source charge	$Q_{gs}$	$V_{DD} = 24\text{V}$ , $I_D = 100\text{A}$	-	9.7	12.9	nC
Gate to drain charge	$Q_{gd}$		-	22.6	33.9	
Gate charge total	$Q_g$	$V_{DD} = 24\text{V}$ , $I_D = 100\text{A}$ , $V_{GS} = 0$ to $10\text{V}$	-	72	96	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 24\text{V}$ , $I_D = 100\text{A}$	-	3.6	-	V

**Reverse Diode**

Inverse diode continuous forward current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	100	A
Inverse diode direct current, pulsed	$I_{SM}$		-	-	400	
Inverse diode forward voltage	$V_{SD}$	$V_{GS} = 0\text{V}$ , $I_F = 80\text{A}$	-	0.9	1.3	V
Reverse recovery time	$t_{rr}$	$V_R = 15\text{V}$ , $I_F = I_S$ , $di_F/dt = 200\text{A}/\mu\text{s}$	-	48	72	ns
Reverse recovery charge	$Q_{rr}$		-	100	150	

### 1 Power dissipation

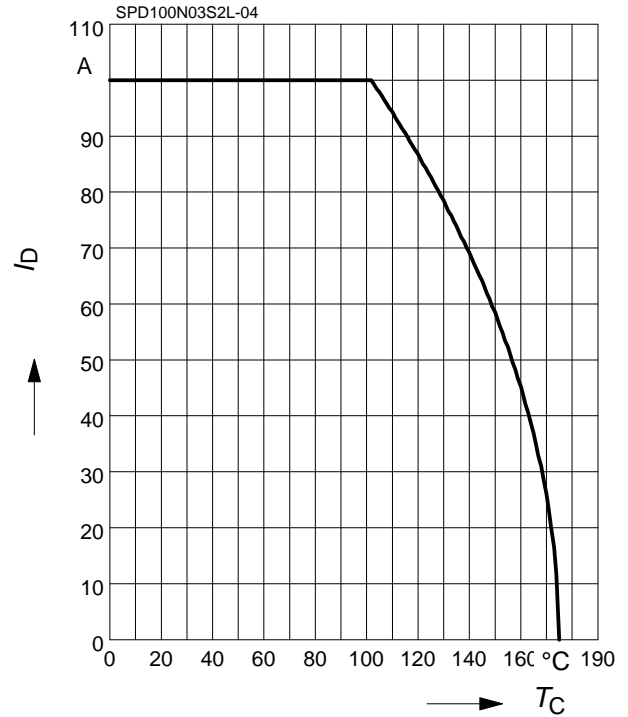
$$P_{tot} = f(T_C)$$



### 2 Drain current

$$I_D = f(T_C)$$

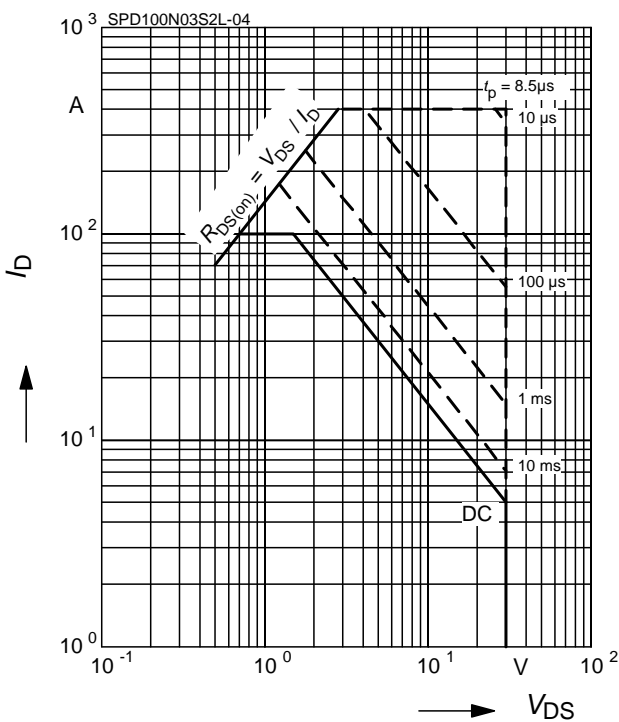
parameter:  $V_{GS} \geq 10\text{ V}$



### 3 Safe operating area

$$I_D = f(V_{DS})$$

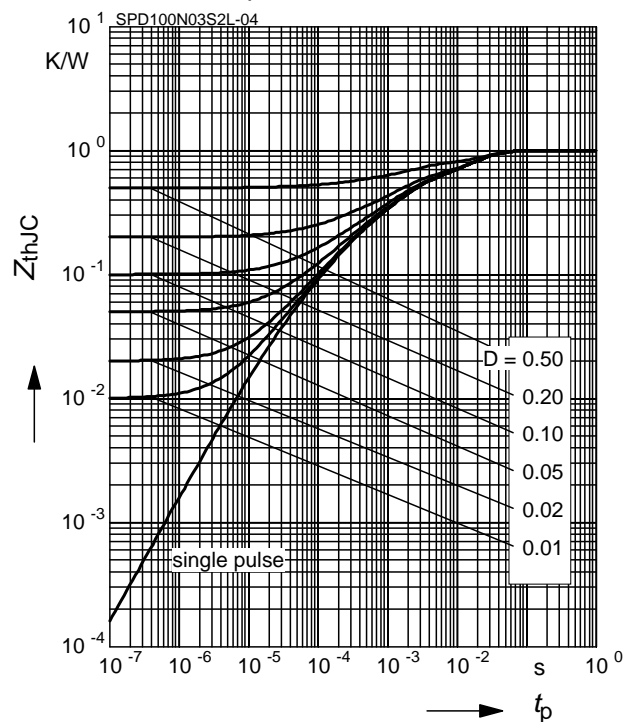
parameter:  $D = 0$ ,  $T_C = 25\text{ °C}$



### 4 Transient thermal impedance

$$Z_{thJC} = f(t_p)$$

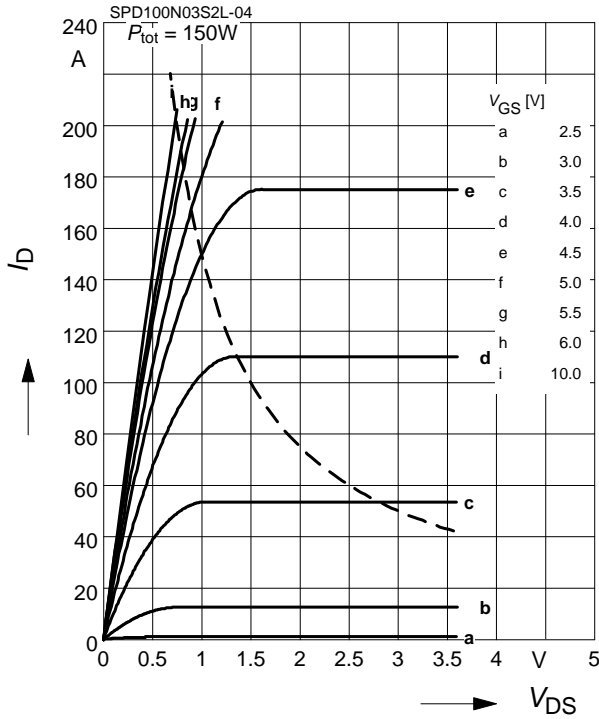
parameter:  $D = t_p/T$



**5 Typ. output characteristic**

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

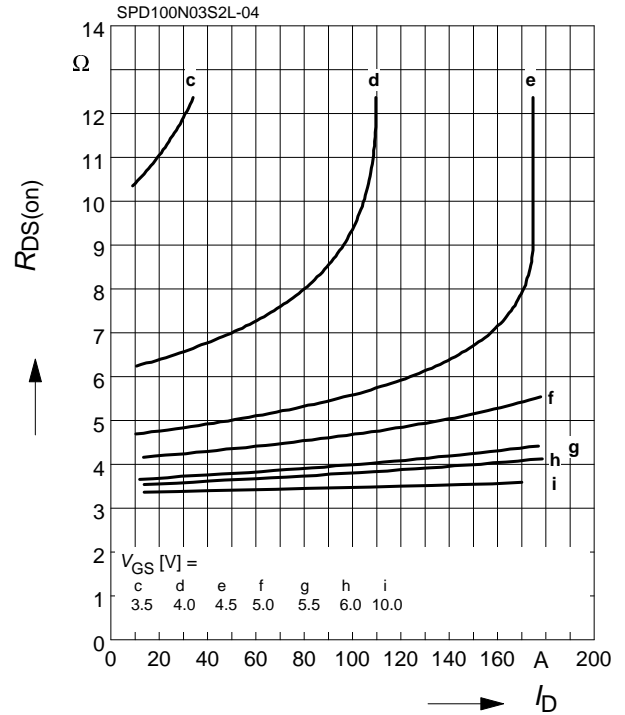
parameter:  $t_p = 80 \mu\text{s}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D)$

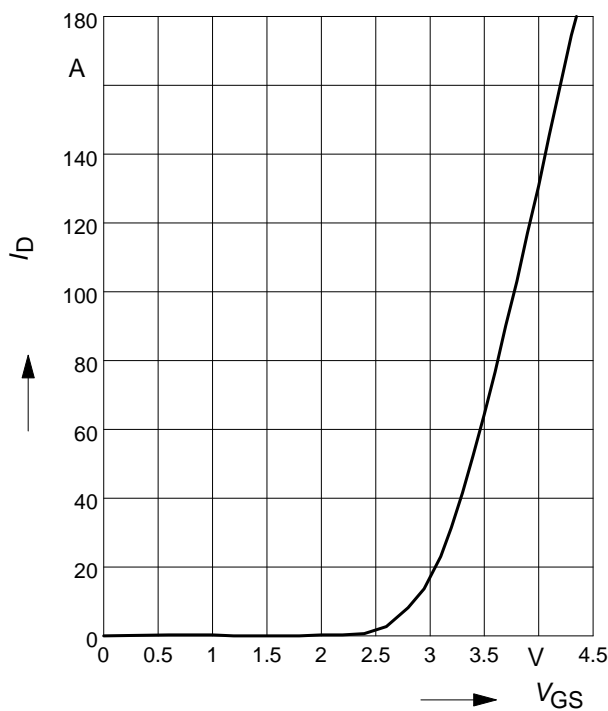
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

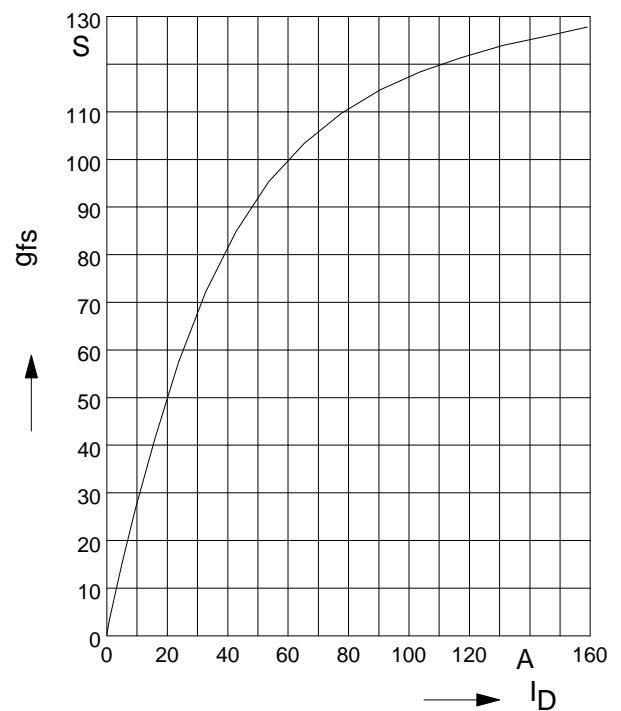
parameter:  $t_p = 20 \mu\text{s}$



**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

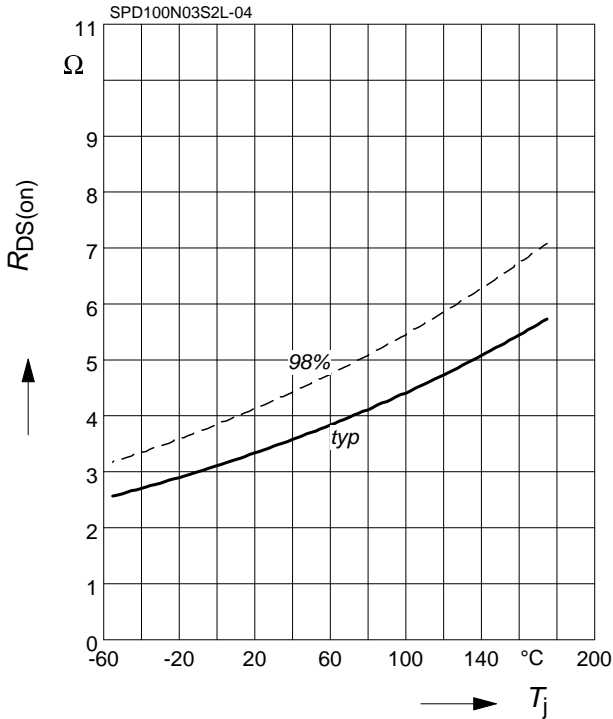
parameter:  $g_{fs}$



**9 Drain-source on-state resistance**

$$R_{DS(on)} = f(T_j)$$

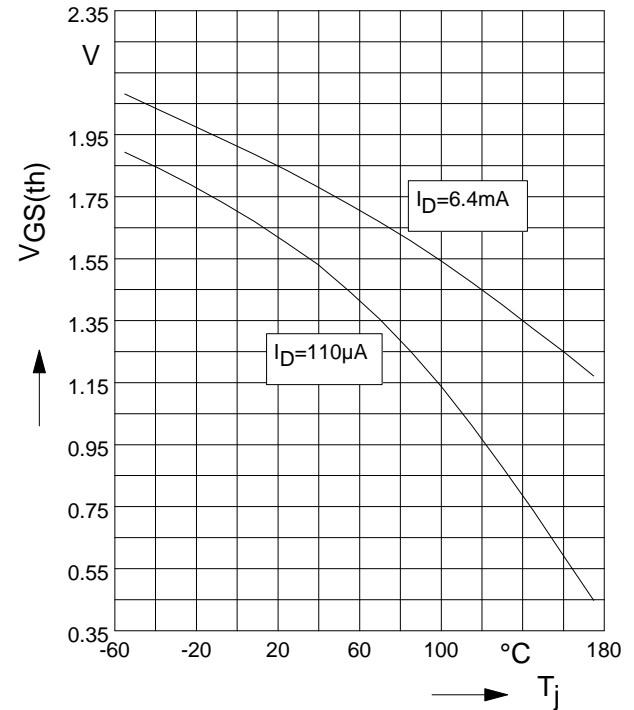
parameter :  $I_D = 50 \text{ A}$ ,  $V_{GS} = 10 \text{ V}$



**10 Typ. gate threshold voltage**

$$V_{GS(th)} = f(T_j)$$

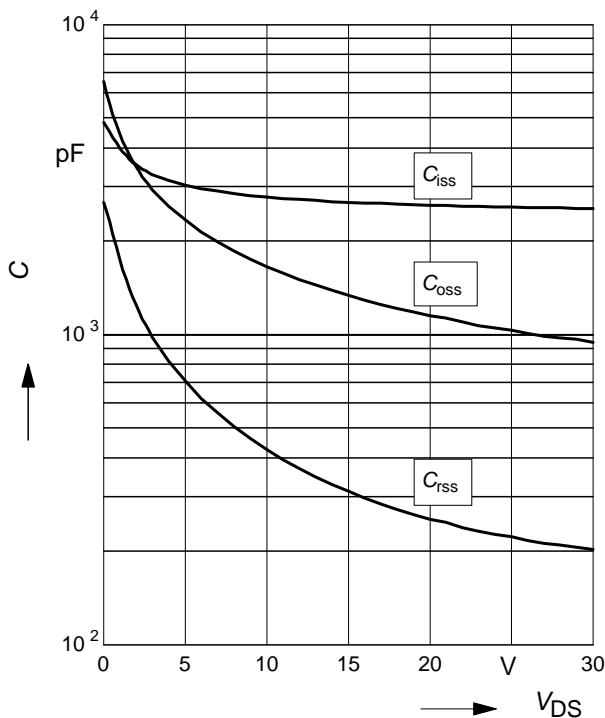
parameter:  $V_{GS} = V_{DS}$



**11 Typ. capacitances**

$$C = f(V_{DS})$$

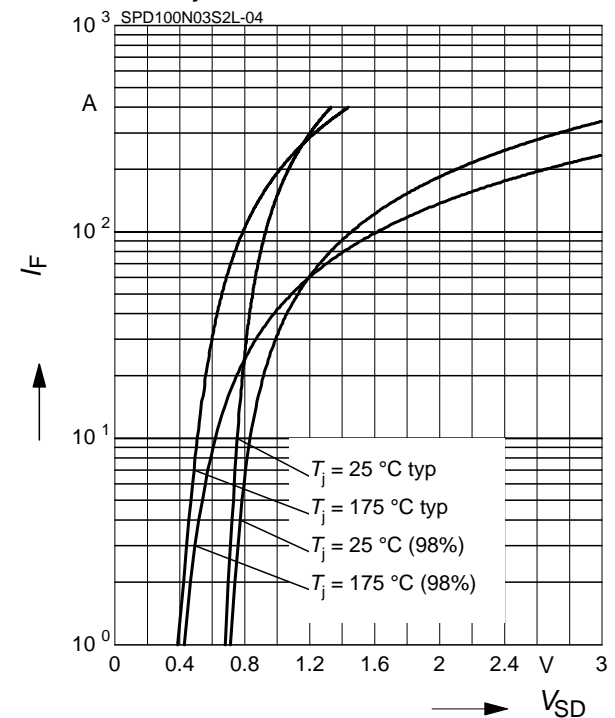
parameter:  $V_{GS} = 0 \text{ V}$ ,  $f = 1 \text{ MHz}$



**12 Forward character. of reverse diode**

$$I_F = f(V_{SD})$$

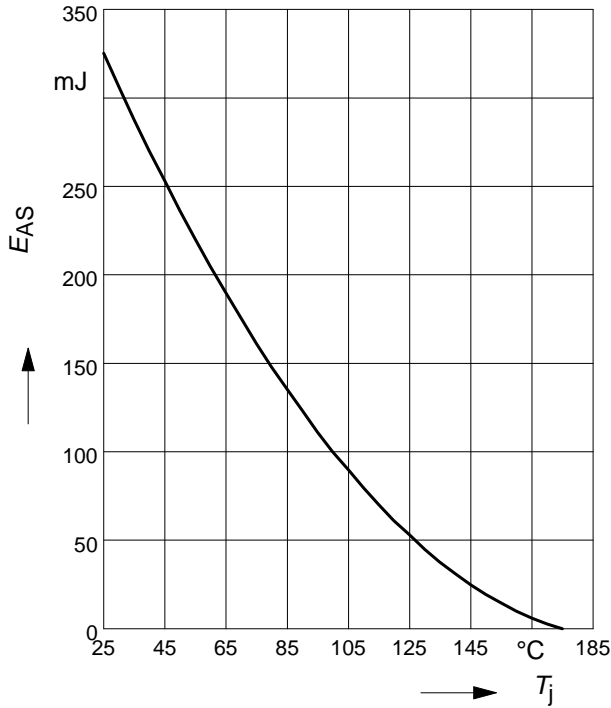
parameter:  $T_j$ ,  $t_p = 80 \mu\text{s}$



**13 Typ. avalanche energy**

$$E_{AS} = f(T_j)$$

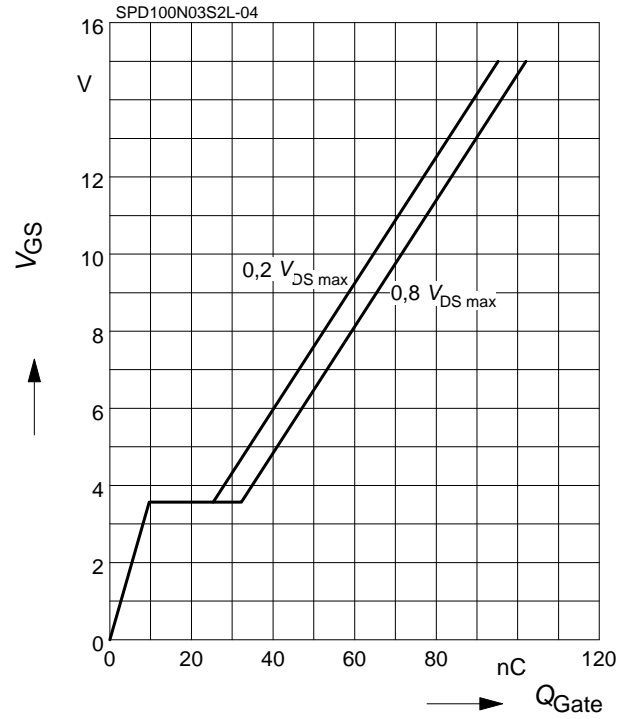
par.:  $I_D = 80 \text{ A}$ ,  $V_{DD} = 25 \text{ V}$ ,  $R_{GS} = 25 \Omega$



**14 Typ. gate charge**

$$V_{GS} = f(Q_{Gate})$$

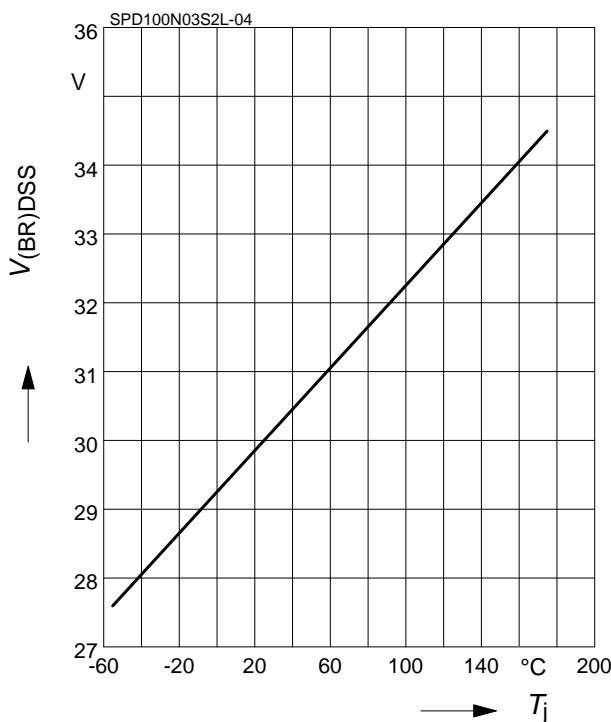
parameter:  $I_D = 100 \text{ A}$  pulsed



**15 Drain-source breakdown voltage**

$$V_{(BR)DSS} = f(T_j)$$

parameter:  $I_D = 10 \text{ mA}$



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**Further information**

Please notice that the part number is BSPD100N03S2L-04, for simplicity the device is referred to by the term SPD100N03S2L-04 throughout this documentation.



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