TPS22967 Single-Channel, Ultra-Low Resistance Load Switch

1 Features

- Integrated Single-Channel Load Switch
- Input Voltage Range: 0.8 V to 5.5 V
- Low R_{ON} Resistance
  - R_{ON} = 22 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 22 mΩ at V_{IN} = 3.6 V (V_{BIAS} = 5 V)
  - R_{ON} = 22 mΩ at V_{IN} = 1.8 V (V_{BIAS} = 5 V)
- 4-A Maximum Continuous Switch Current
- Low Quiescent Current (50 µA)
- Low Control Input Threshold Enables Use of 1.2-V, 1.8-V, 2.5-V, and 3.3-V Logic
- Configurable Rise Time
- Quick Output Discharge (QOD)
- WSON 8-Pin Package With Thermal Pad

2 Applications

- Ultrabooks™
- Notebooks and Netbooks
- Tablet PCs
- Consumer Electronics
- Set-Top Boxes and Residental Gateways
- Telecom Systems
- Solid-State Drives (SSD)

3 Description

The TPS22967 device is a small, ultra-low R_{ON}, single-channel load switch with controlled turnon. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of 4 A. The switch is controlled by an on/off input (ON), which can interface directly with low-voltage control signals. In the TPS22967, a 225-Ω pulldown resistor is added for quick output discharge when the switch is turned off.

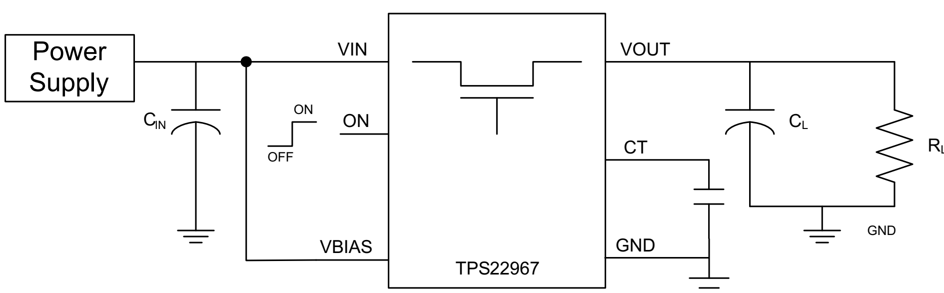
The TPS22967 is available in a small, space-saving 2-mm × 2-mm 8-pin WSON package (DSG) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22967	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Typical Application Schematic



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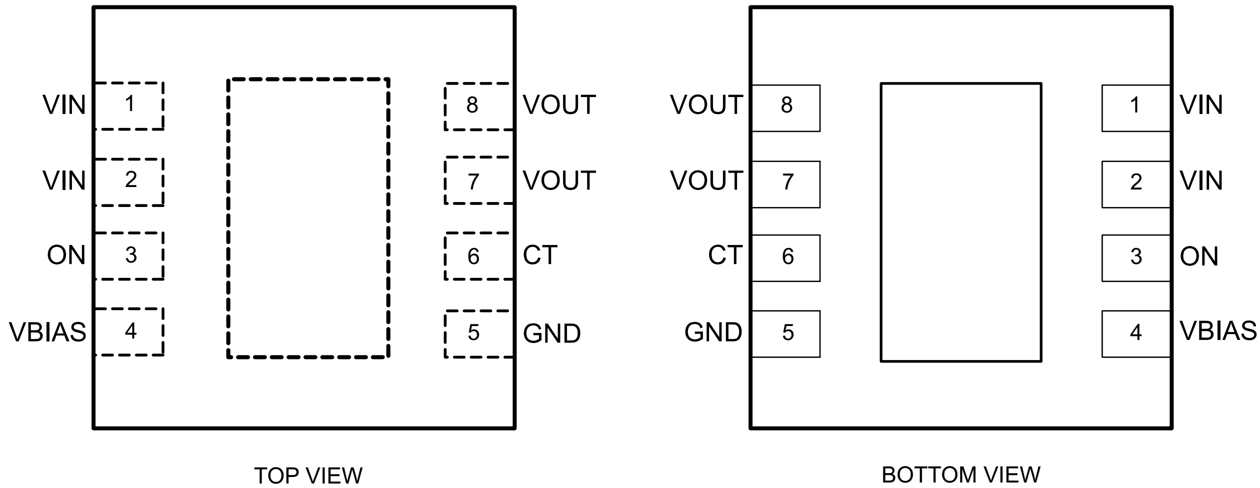
5 Revision History

Changes from Original (August 2013) to Revision A	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

6 Pin Configuration and Functions

DSG Package
8-Pin WSON



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	6	O	Switch slew rate control. Can be left floating. See *Application and Implementation* for more information.
GND	5	–	Device ground.
ON	3	I	Active high switch control input. Do not leave floating.
VBIAS	4	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.5 V. See Application Information section for more information.
VIN	1, 2	I	Switch input. Input capacitor recommended for minimizing V_{IN} dip. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8 V to V_{BIAS}.
VOUT	7, 8	O	Switch output.
Thermal Pad		–	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See *Layout Example* for layout guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT(2)
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{ON}	ON voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		4	A
I_{PLS}	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle		6	A
T_A	Operating free-air temperature(3)	–40	85	°C
T_J	Maximum junction temperature		125	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $TA_{(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		0.8		V_{BIAS}	V
V_{BIAS}	Bias voltage		2.5		5.5	V
V_{ON}	ON voltage		0		5.5	V
V_{OUT}	Output voltage				V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	1.2		5.5	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	0		0.5	V
C_{IN}	Input capacitor		1(1)			µF

(1) Refer to *Application Information*.

7.4 Thermal Information

THERMAL METRIC[(1)]		TPS22967 DSG [WSON] 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_{BIAS} = 5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ 85°C (Full) and V_{BIAS} = 5 V. Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 5 V		Full		50	75	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 5 V	Full		0.2	8	µA
			V_{IN} = 3.3 V			0.02	3	
			V_{IN} = 1.8 V			0.01	2	
			V_{IN} = 0.8 V			0.005	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5 V	V_{IN} = 5 V	25°C		22	33	mΩ
				Full			35	
			V_{IN} = 3.3 V	25°C		22	33	
				Full			35	
			V_{IN} = 1.8 V	25°C		22	33	
				Full			35	
			V_{IN} = 1.5 V	25°C		22	33	
				Full			35	
			V_{IN} = 1.2 V	25°C		22	33	
				Full			35	
			V_{IN} = 0.8 V	25°C		22	33	
				Full			35	
R_{PD}	Output pulldown resistance	V_{IN} = 5.0 V, V_{ON} = 0V, I_{OUT} = 15 mA		Full		225	300	Ω

7.6 Electrical Characteristics: V_{BIAS} = 2.5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ 85°C (Full) and V_{BIAS} = 2.5 V. Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 2.5 V		Full		20	30	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 2.5 V	Full		0.01	3	µA
			V_{IN} = 1.8 V			0.01	2	
			V_{IN} = 1.2 V			0.005	2	
			V_{IN} = 0.8 V			0.003	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		26	38	mΩ
				Full			40	
			V_{IN} = 1.8 V	25°C		26	38	
				Full			40	
			V_{IN} = 1.5 V	25°C		25	38	
				Full			40	
			V_{IN} = 1.2 V	25°C		24	38	
				Full			40	
			V_{IN} = 0.8 V	25°C		24	38	
				Full			40	
R_{PD}	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		Full		275	325	Ω

7.7 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (UNLESS OTHERWISE NOTED)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1325		µs
t_{OFF}	Turnoff time			10		
t_R	V_{OUT} rise time			1625		
t_F	V_{OUT} fall time			3.5		
t_D	ON delay time			500		
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (UNLESS OTHERWISE NOTED)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		600		µs
t_{OFF}	Turnoff time			80		
t_R	V_{OUT} rise time			300		
t_F	V_{OUT} fall time			5.5		
t_D	ON delay time			460		
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (UNLESS OTHERWISE NOTED)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2200		µs
t_{OFF}	Turnoff time			9		
t_R	V_{OUT} rise time			2275		
t_F	V_{OUT} fall time			3.1		
t_D	ON delay time			1075		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (UNLESS OTHERWISE NOTED)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1450		µs
t_{OFF}	Turn-off time			60		
t_R	V_{OUT} rise time			875		
t_F	V_{OUT} fall time			5.5		
t_D	ON delay time			1010		

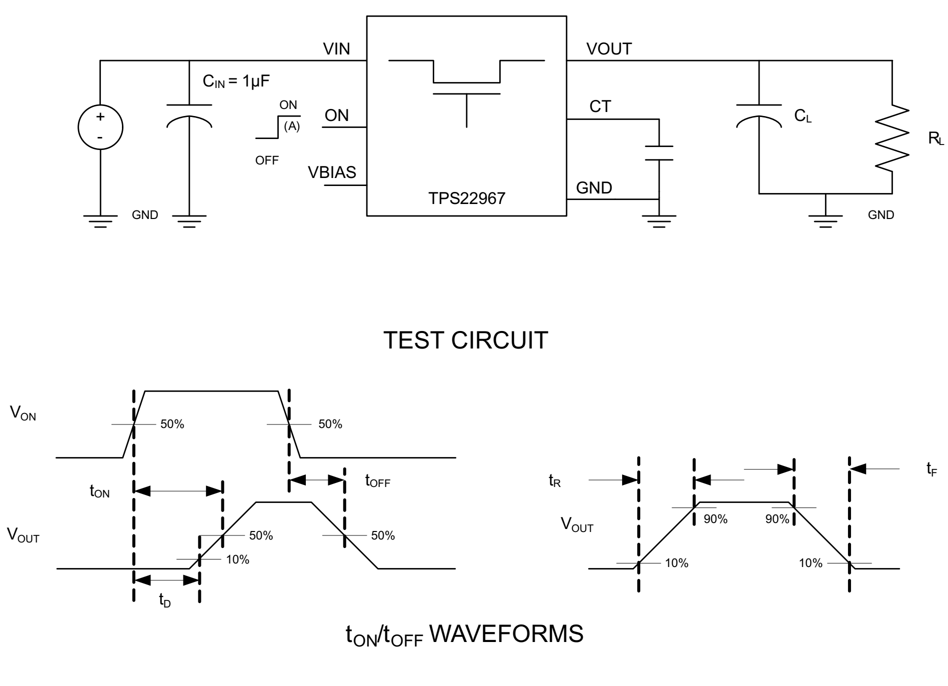


Figure 1. Test Circuit and Timing Waveforms

7.8 Typical Characteristics

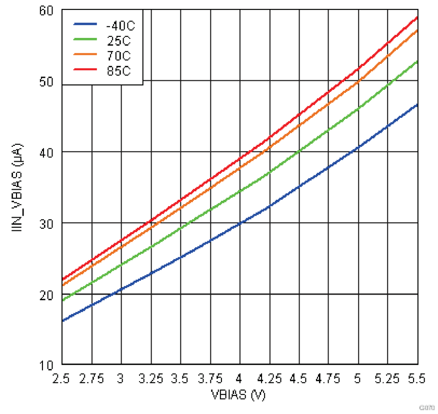


Figure 2. V_{BIAS} vs Quiescent Current

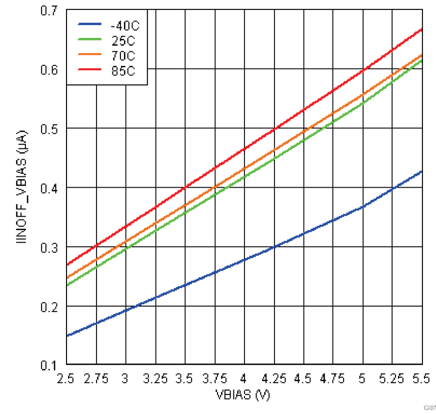


Figure 3. V_{BIAS} vs Shutdown Current

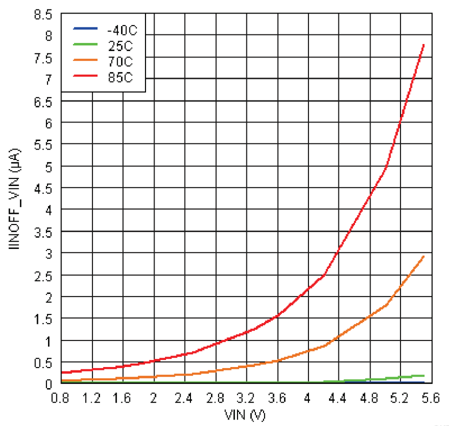


Figure 4. V_{IN} vs Off-State VIN Current

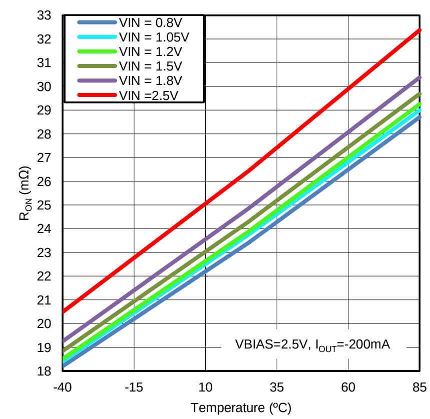


Figure 5. Temperature vs R_{ON} (V_{BIAS} = 2.5 V)

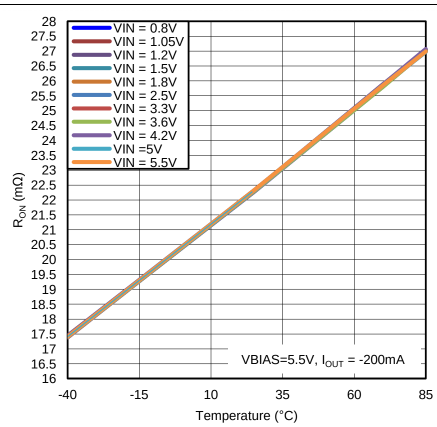


Figure 6. Temperature vs R_{ON} (V_{BIAS} = 5.5 V)

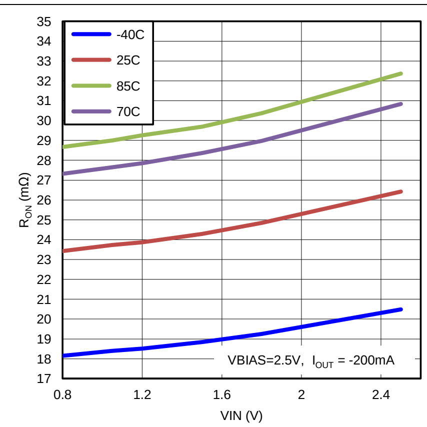


Figure 7. V_{IN} vs R_{ON} (V_{BIAS} = 2.5 V)

Typical Characteristics (continued)

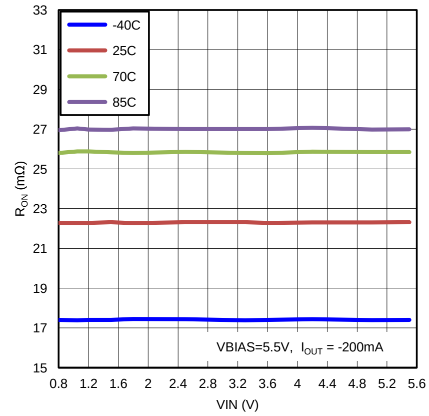


Figure 8. V_{IN} vs R_{ON} (V_{BIAS} = 5.5 V)

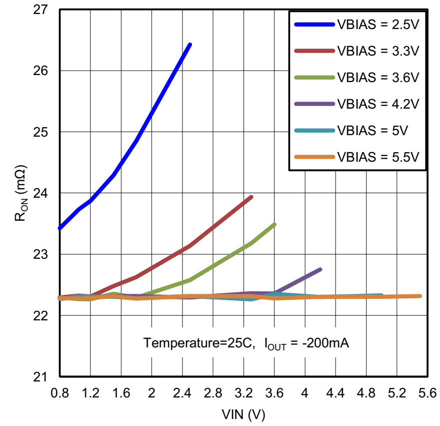


Figure 9. V_{IN} vs R_{ON} (T_A = 25°C)

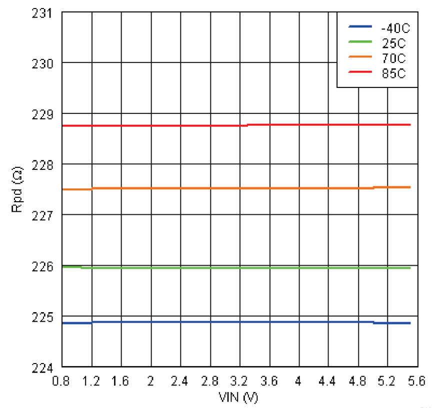


Figure 10. VIN vs R_{PD} (V_{BIAS} = 5.5 V)

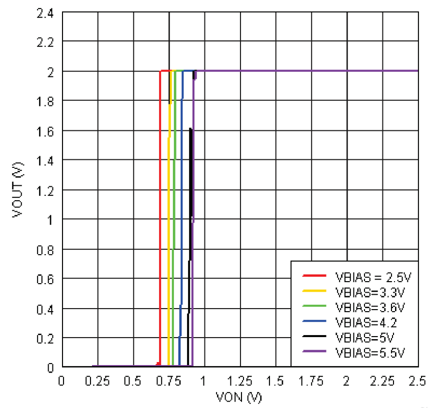


Figure 11. V_{ON} vs V_{OUT} (T_A = 25°C)

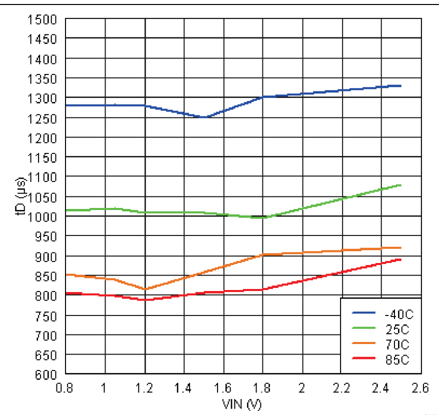


Figure 12. V_{IN} vs t_D (V_{BIAS} = 2.5 V, CT = 1 nF)

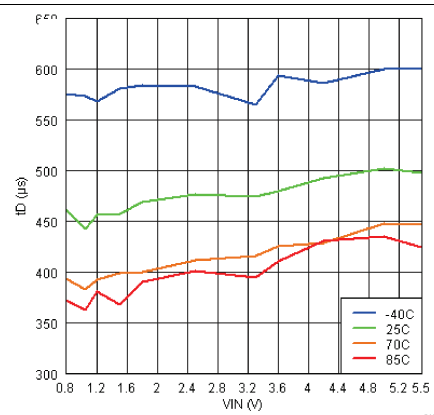


Figure 13. V_{IN} vs t_D (V_{BIAS} = 5.5 V, CT = 1 nF)

Typical Characteristics (continued)

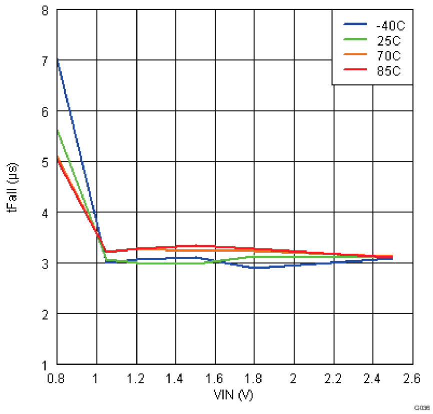


Figure 14. V_{IN} vs t_F (V_{BIAS} = 2.5 V, CT = 1 nF)

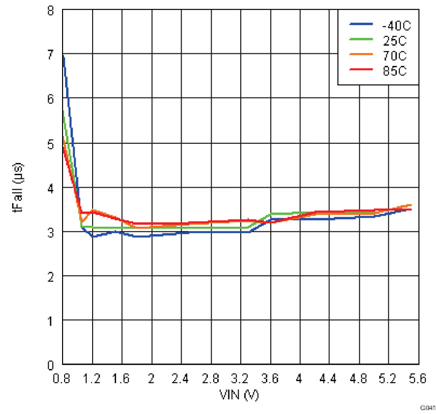


Figure 15. V_{IN} vs t_F (V_{BIAS} = 5.5 V, CT = 1 nF)

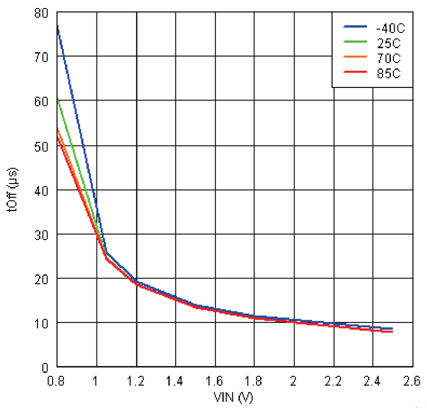


Figure 16. V_{IN} vs t_{OFF} (V_{BIAS} = 2.5 V, CT = 1 nF)

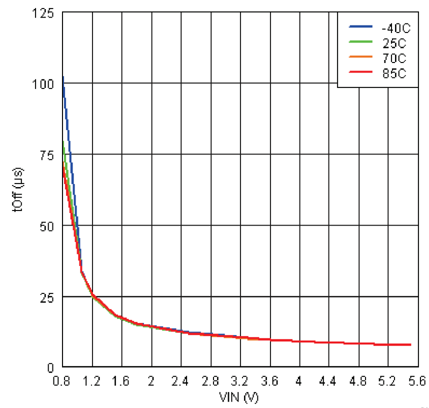


Figure 17. V_{IN} vs t_{OFF} (V_{BIAS} = 5.5 V, CT = 1 nF)

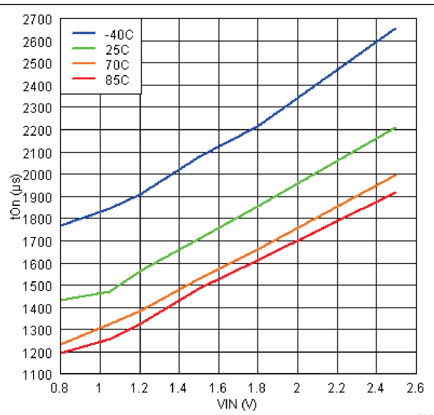


Figure 18. V_{IN} vs t_{ON} (V_{BIAS} = 2.5 V, CT = 1 nF)

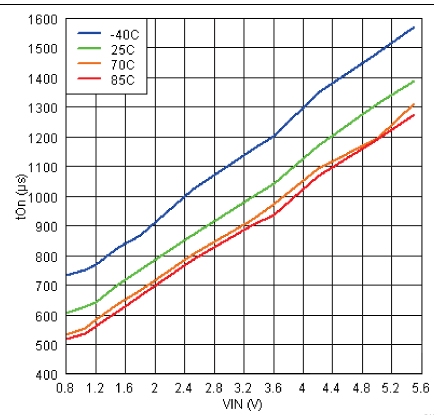


Figure 19. V_{IN} vs t_{ON} (V_{BIAS} = 5.5 V, CT = 1 nF)

Typical Characteristics (continued)

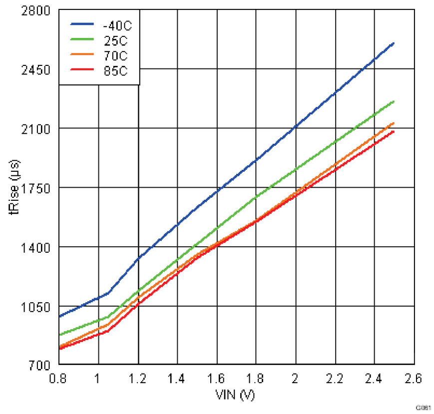


Figure 20. V_{IN} vs t_R (V_{BIAS} = 2.5 V, CT = 1 nF)

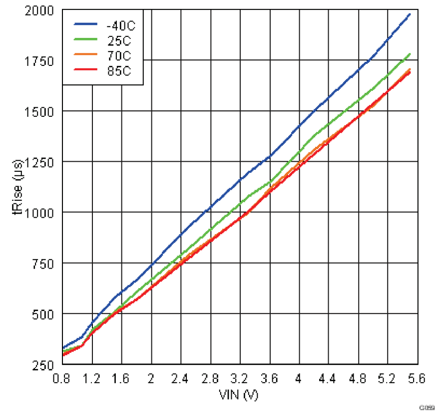


Figure 21. V_{IN} vs t_R (V_{BIAS} = 5.5 V, CT = 1 nF)

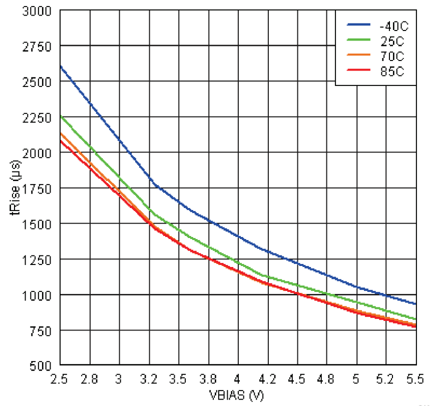


Figure 22. V_{BIAS} vs t_R (V_{IN} = 2.5 V, CT = 1 nF)

7.8.1 Typical AC Scope Captures at T_A = 25ºC, CT = 1 nF

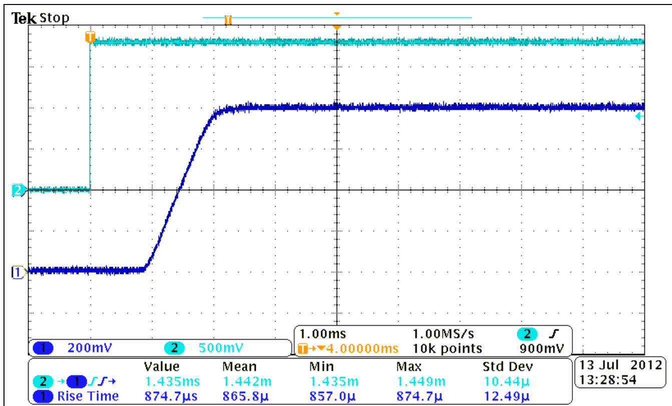


Figure 23. Turnon Response Time
(V_{IN} = 0.8 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)
CH1: VOUT, CH2: ON

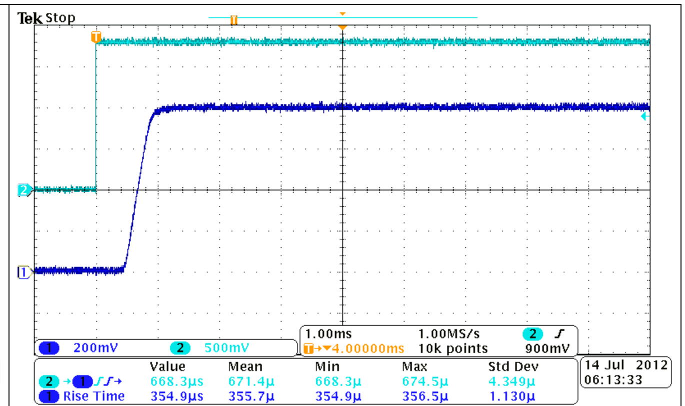


Figure 24. Turnon Response Time
(V_{IN} = 0.8 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)
CH1: VOUT, CH2: ON

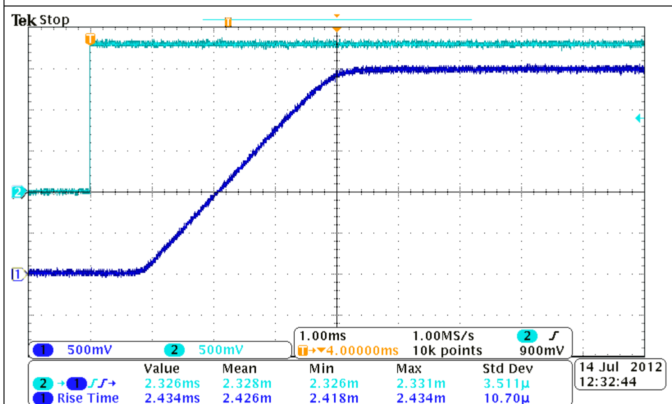


Figure 25. Turnon Response Time
(V_{IN} = 2.5 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)
CH1: VOUT, CH2: ON

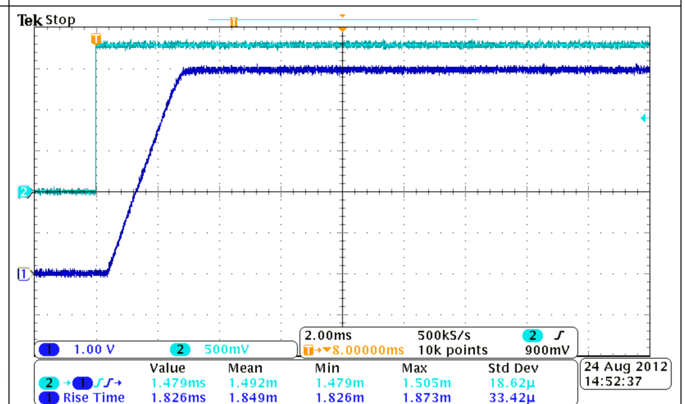


Figure 26. Turnon Response Time
(V_{IN} = 5 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)
CH1: VOUT, CH2: ON

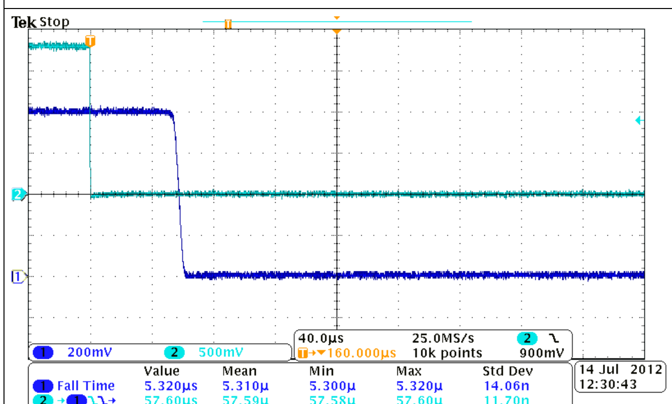


Figure 27. Turnoff Response Time
(V_{IN} = 0.8 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)
CH1: VOUT, CH2: ON

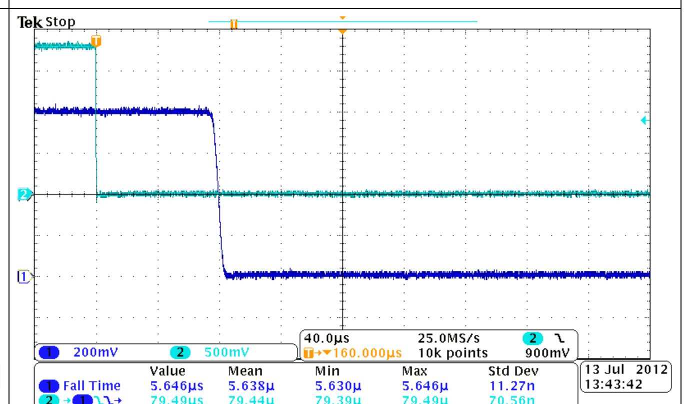


Figure 28. Turnoff Response Time
(V_{IN} = 0.8 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)
CH1: VOUT, CH2: ON

Typical AC Scope Captures at T_A = 25ºC, CT = 1 nF (continued)

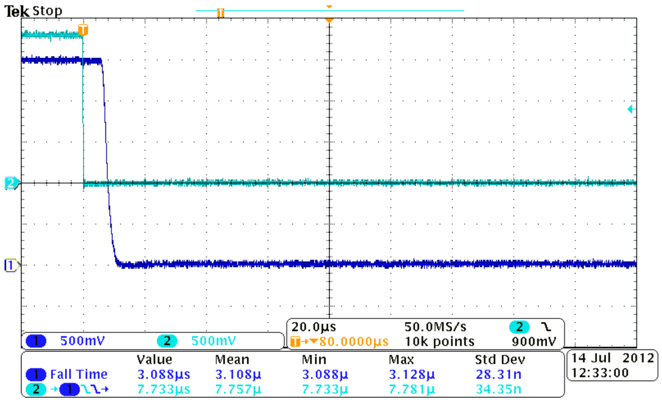


Figure 29. Turnoff Response Time (V_{IN} = 2.5 V, V_{BIAS} = 2.5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω) CH1: VOUT, CH2: ON

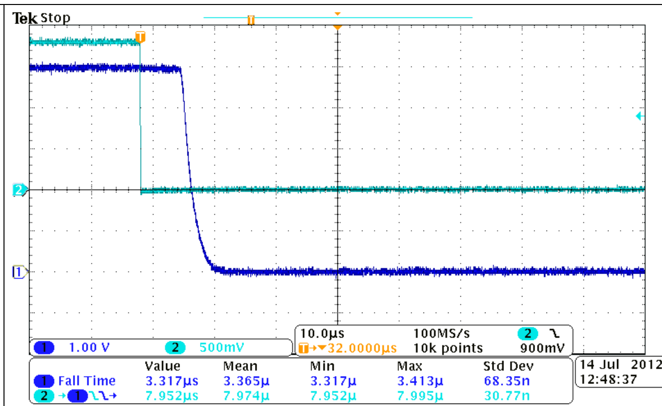


Figure 30. Turnoff Response Time (V_{IN} = 5 V, V_{BIAS} = 5 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω) CH1: VOUT, CH2: ON

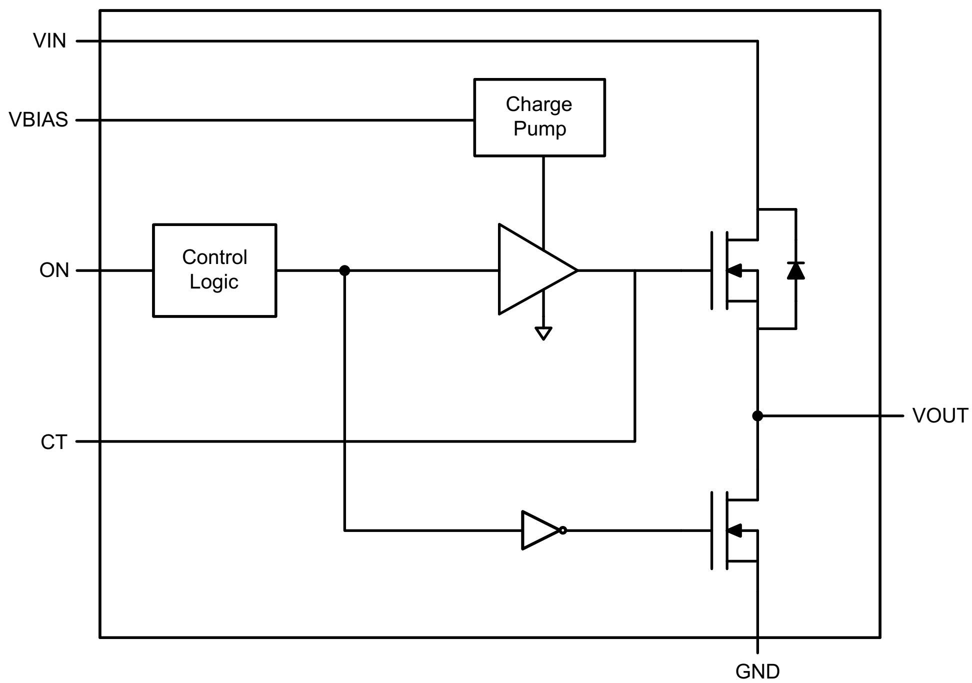
8 Detailed Description

8.1 Overview

The TPS22967 device is a single-channel, 4-A load switch in an 8-pin WSON package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise time.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

This section describes the integrated features for the TPS22967.

8.3.1 ON/OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

Feature Description (continued)

8.3.2 Adjustable Rise Time

A capacitor to GND on the CT pin sets the VOUT slew rate. The voltage on the CT pin can be as high as 12 V. Therefore, the minimum voltage rating for the CT capacitor must be 25 V for optimal performance. An approximate formula for the relationship between CT and slew rate is (Equation 1 accounts for 10% to 90% measurement on V_{OUT} and does NOT apply for CT = 0 pF. Use Table 1 to determine rise times for when CT = 0 pF):

$$SR = 0.39 \times CT + 13.4$$

where

- SR = slew rate (in µs/V).
- CT = the capacitance value on the CT pin (in pF).
- The units for the constant 13.4 is in µs/V. The units for the constant 0.39 are in µs/(V × pF). (1)

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and the ON pin is asserted high.

Table 1. Rise Times On a Typical Device

CTx (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω TYPICAL VALUES at 25°C, 25 V X7R 10% CERAMIC CAPACITOR						
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.8 V
0	127	93	62	55	51	46	42
220	475	314	188	162	141	125	103
470	939	637	359	304	255	218	188
1000	1869	1229	684	567	476	414	344
2200	4020	2614	1469	1211	1024	876	681
4700	8690	5746	3167	2703	2139	1877	1568
10000	18360	12550	6849	5836	4782	4089	3449

8.3.3 Quick Output Discharge

The TPS22967 includes a Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 225 Ω and prevents the output from floating while the switch is disabled.

8.4 Device Functional Modes

Table 2 describes the functional state of the load switch as determined by the ON pin.

Table 2. Functional Table

ON	VIN to VOUT	VOUT to GND
L	Off	On
H	On	Off

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section describes design considerations for the TPS22967 which can vary depending on the specific application.

9.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short circuit, a capacitor must be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current applications. When switching heavy loads, TI recommends having an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.1.2 Output Capacitor (Optional)

Because of the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during start-up; however, a 10-to-1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turnon due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see below).

9.1.3 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in the *Electrical Characteristics: V_{BIAS} = 5 V* table. See Figure 31 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Never exceed the maximum voltage rating for VIN and VBIAS.

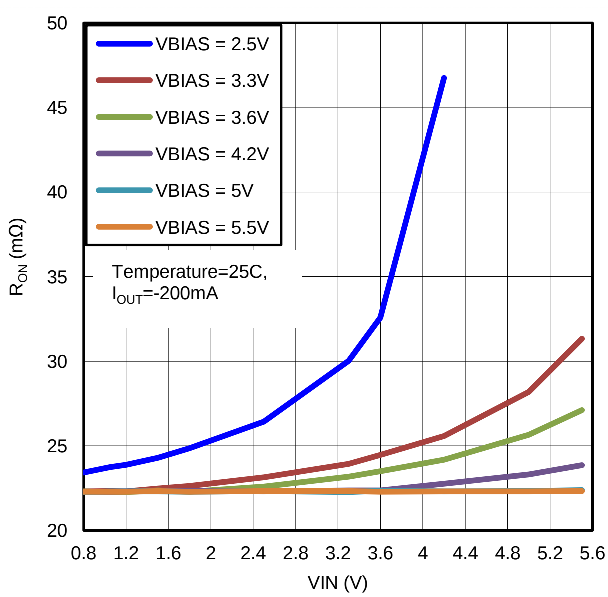
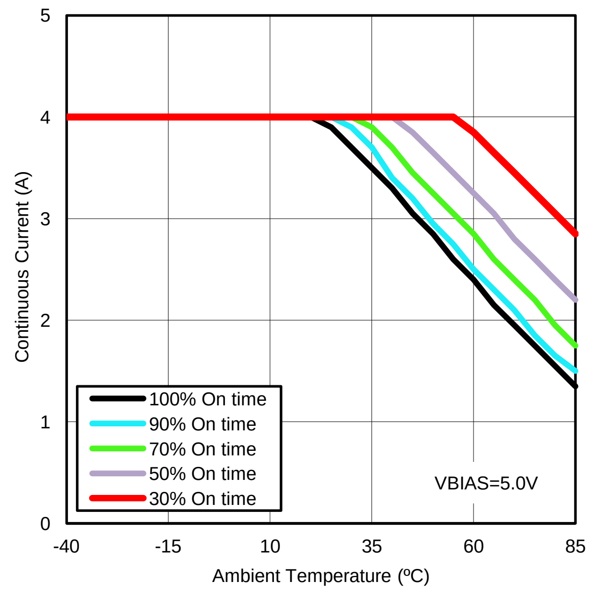


Figure 31. R_{ON} vs V_{IN} ($V_{IN} > V_{BIAS}$)

Application Information (continued)

9.1.4 Safe Operating Area (SOA)

The SOA curves show the continuous current carrying capability of the device versus ambient temperature (T_A) to ensure reliable operation over 70,000 hours of device lifetime. The different curves represent the *percentage On time* over device lifetime and can be used as a reference to understand the current carrying capability of TPS22967 under different use cases. TI recommends maintaining continuous current at or below the SOA curves shown in Figure 32.



On time is the duration of time that the device is enabled (ON ≥ V_{IH}) over 70,000 hour lifetime.

Figure 32. Safe Operating Area

9.2 Typical Application

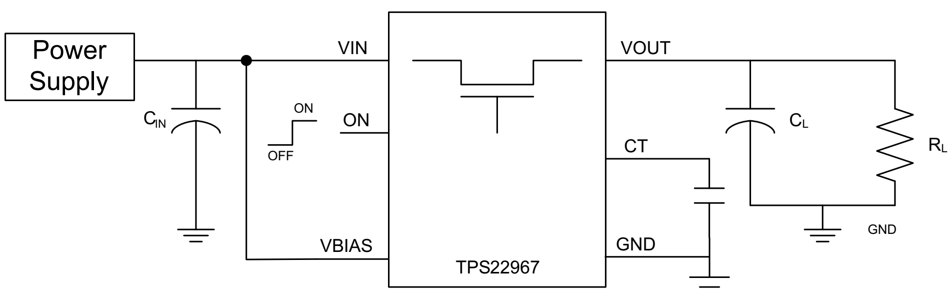


Figure 33. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	22 µF
Maximum Acceptable Inrush Current	400 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 2:

Inrush Current = C × dV/dt

where

- C = output capacitance.
- dV = output voltage.
- dt = rise time. (2)

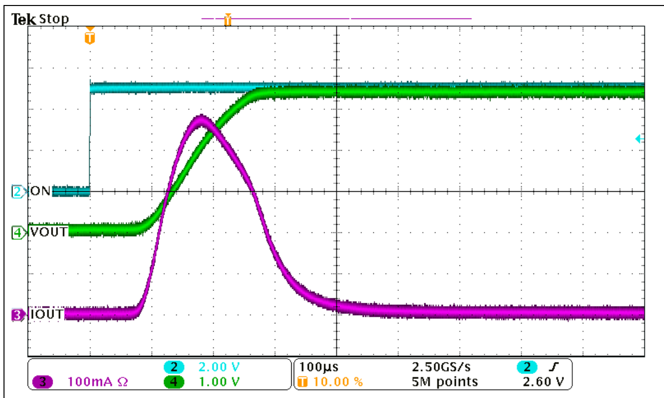
The TPS22967 offers adjustable rise time for VOUT. This feature lets the user control the inrush current during turnon. The appropriate rise time can be calculated using the design requirements and the inrush current equation.

$$400\ \text{mA} = 22\ \mu\text{F} \times 3.3\ \text{V/dt} \quad (3)$$

$$\text{dt} = 181.5\ \mu\text{s} \quad (4)$$

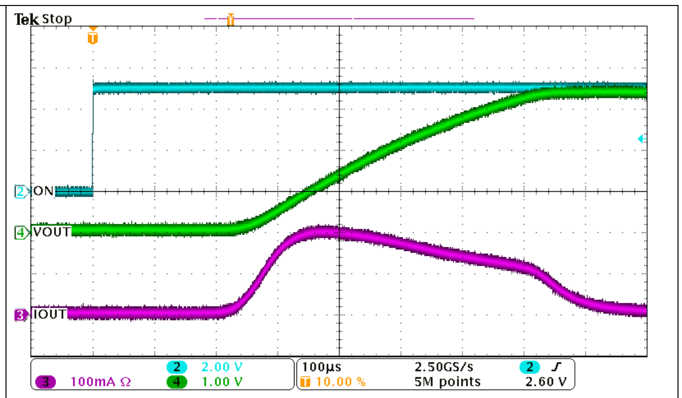
To ensure an inrush current of less than 400 mA, choose a CT value that will yield a rise time of more than 181.5 µs. See *Application Curves* for an example of how the CT capacitor can be used to reduce inrush current.

9.2.3 Application Curves



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 34. Inrush Current With CT = 0 pF



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 35. Inrush Current with CT = 220 pF

10 Power Supply Recommendations

The device is designed to operate from a VBIAS range of 2.5 V to 5.5 V and a VIN range of 0.8 V to 5.5 V. The power supply must be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This additional capacitance causes the load switch to turn on more slowly. Not only will this reduce transient inrush current, but it will also give the power supply more time to respond to the load current step.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 5 as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (5)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation.
- $T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22967).
- T_A = ambient temperature of the device.
- Θ_{JA} = junction to air thermal impedance. See *Thermal Information*. This parameter is highly dependent upon board layout.

Figure 36 shows an example of a layout. Notice the thermal vias under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

11.2 Layout Example

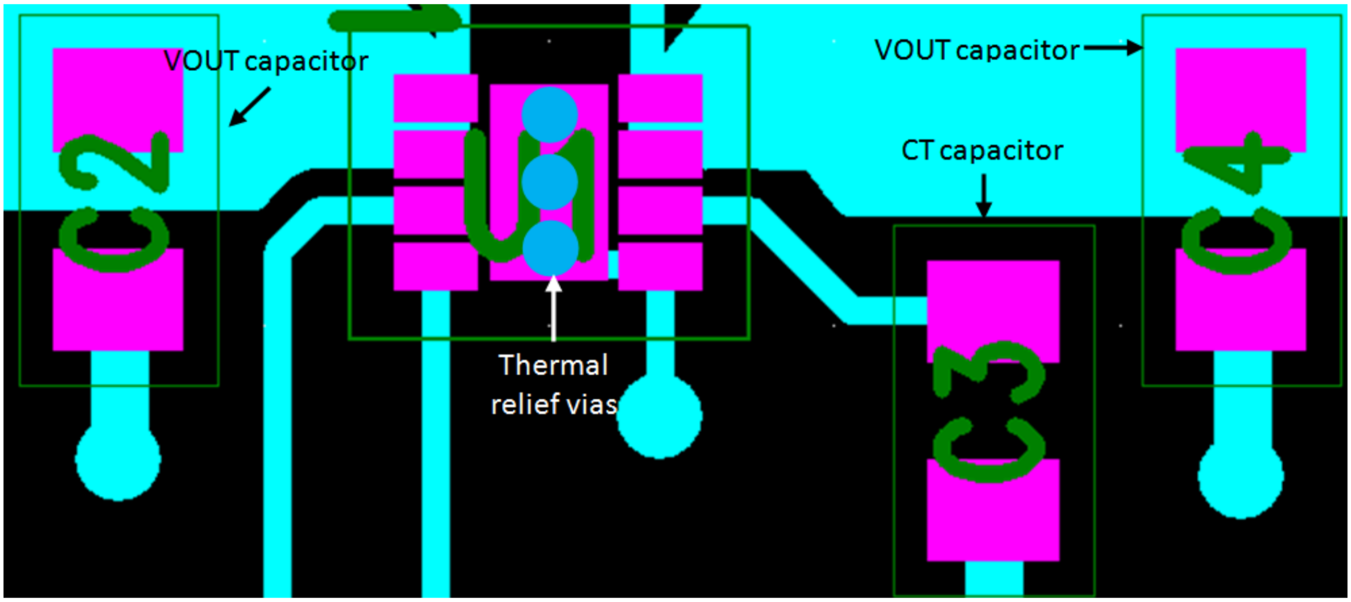


Figure 36. Layout Example

12 Device and Documentation Support

12.1 Trademarks

Ultrabooks is a trademark of Intel.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22967DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTU	Samples
TPS22967DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZTU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

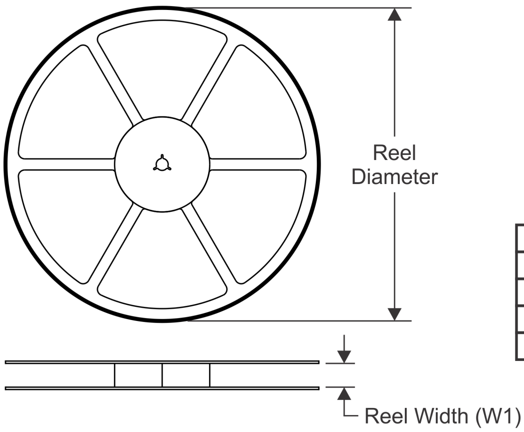
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

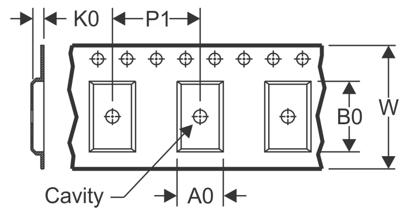
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

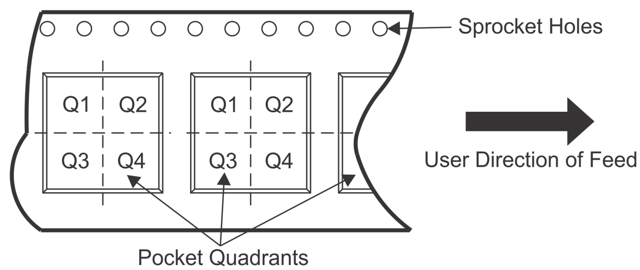


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

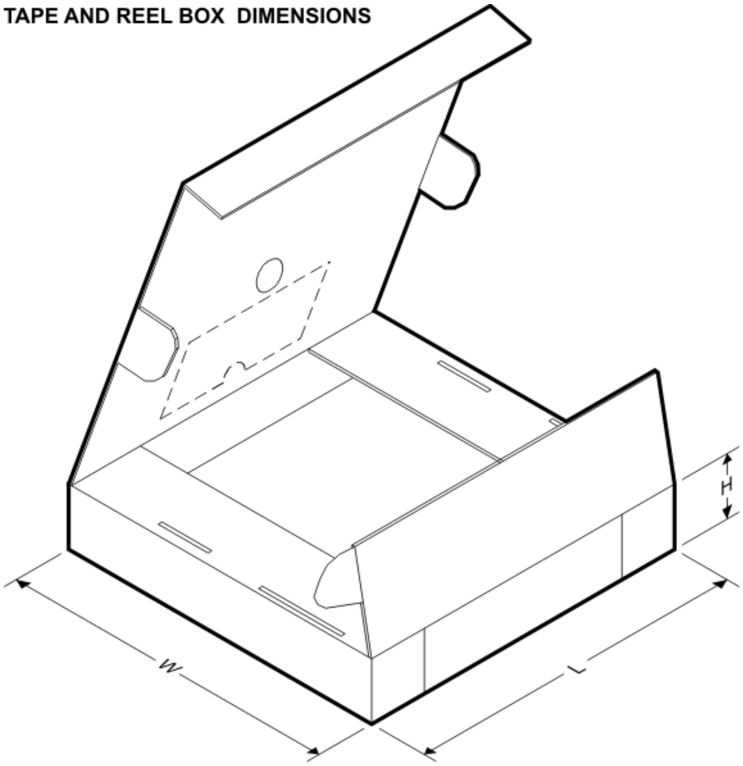
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22967DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22967DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

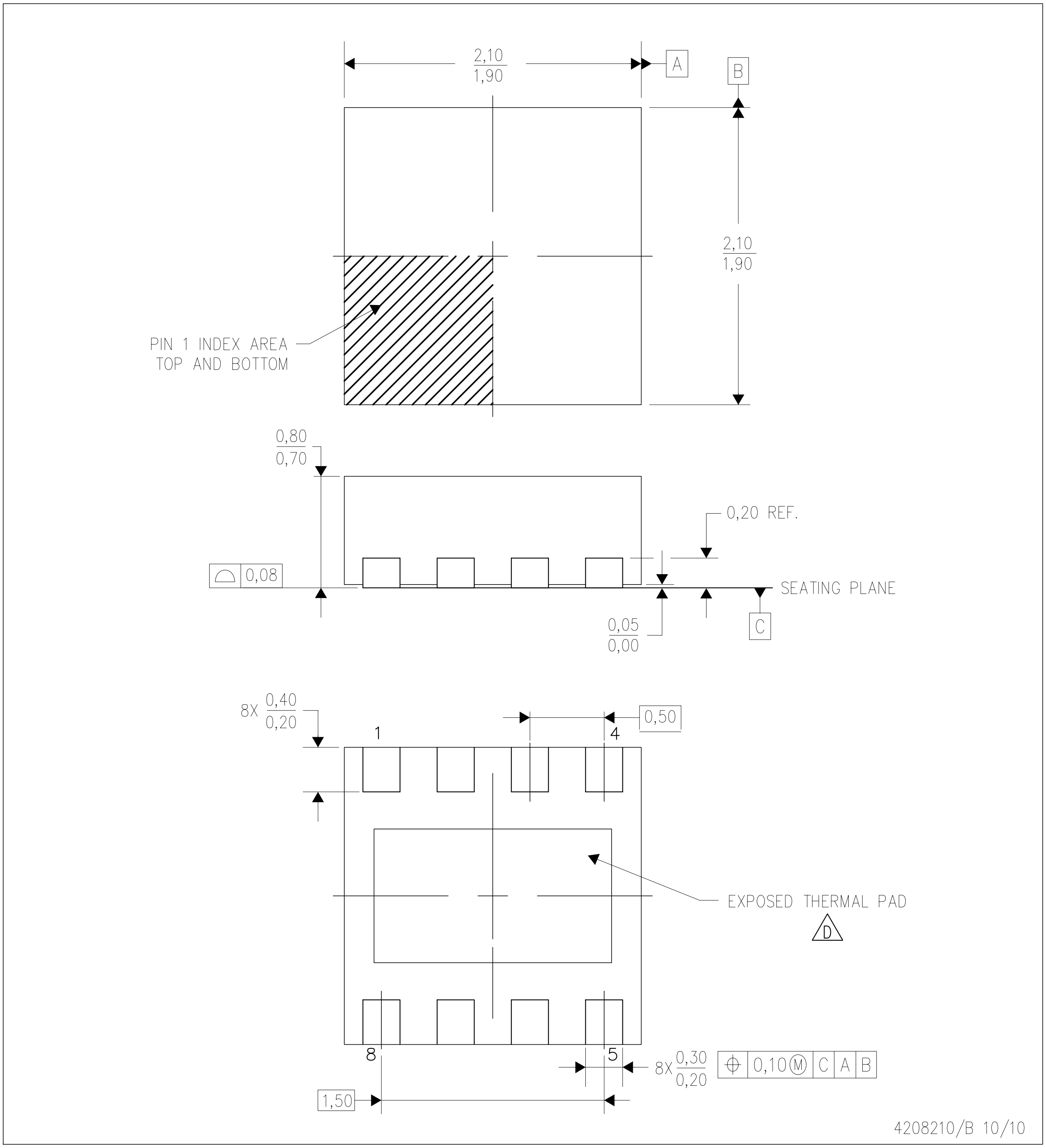
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22967DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22967DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

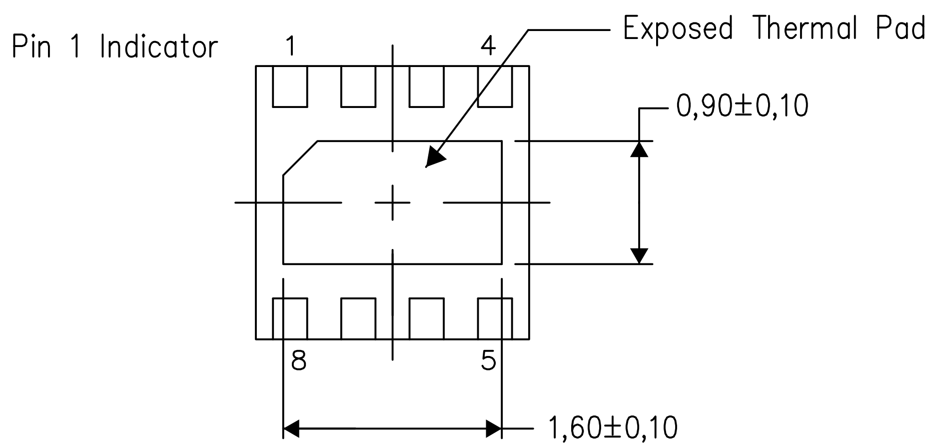
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



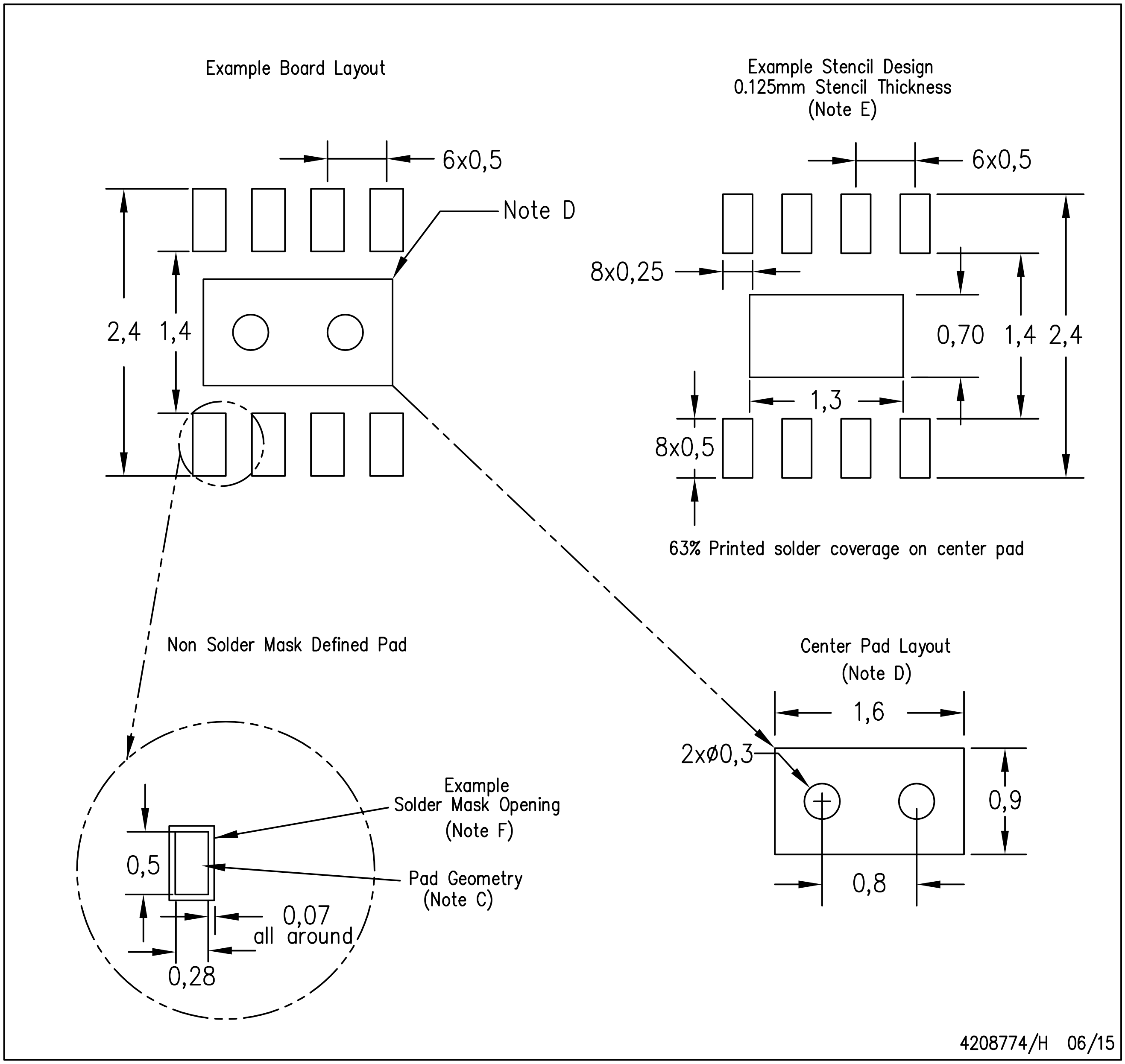
Bottom View

Exposed Thermal Pad Dimensions

4208347/I 06/15

NOTE: All linear dimensions are in millimeters

DSG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

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