SINGLE SYNCHRONOUS STEP-DOWN CONTROLLER

Check for Samples :TPS51117

FEATURES

- **High Efficiency, Low Power Consumption, 4.5-µA Typical Shutdown Current**
- ***Fixed Frequency Emulated* On-Time Control, Adjustable from 100 kHz to 550 kHz**
- **D-CAP™ Mode with 100-ns Load Step Response**
- **< 1% Initial Reference Accuracy**
- **Output Voltage Range: 0.75 V to 5.5 V**
- **Wide Input Voltage Range: 1.8 V to 28 V**
- **Selectable Auto-Skip/PWM-Only Operation**
- **Temperature Compensated (4500 ppm/°C) Low-Side $R_{DS(on)}$ Overcurrent Sensing**
- **Negative Overcurrent Limit**
- **Integrated Boost Diode**
- **Integrated OVP/UVP and Thermal Shutdown**
- **Power-Good Signal**
- **Internal 1.2-ms Voltage Softstart**
- **Integrated Output Discharge (Softstop)**

APPLICATIONS

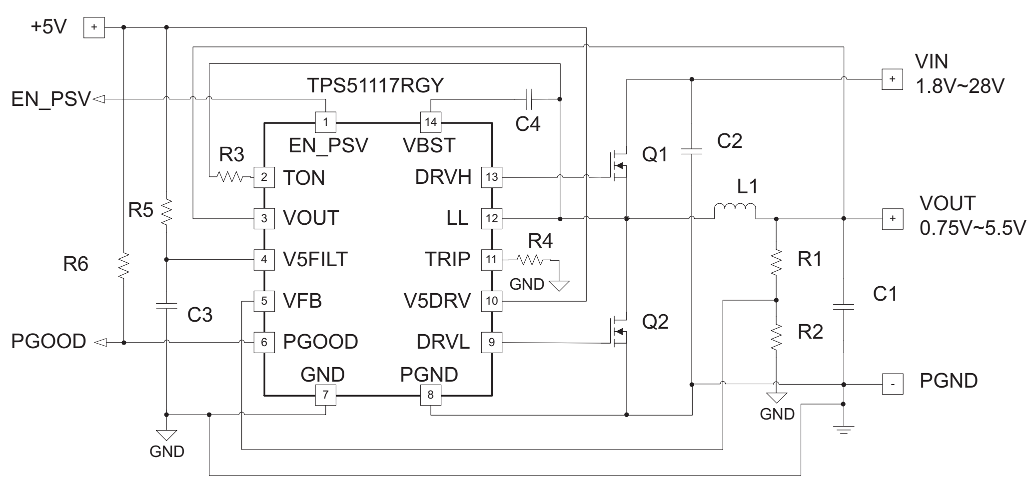
- **Notebook Computers**
- **I/O Supplies**
- **System Power Supplies**

DESCRIPTION

The TPS51117 is a cost effective, synchronous buck controller for POL voltage regulation in notebook PC applications. The controller is dedicated for Adaptive On-Time D-CAP™ Mode operation that provides *ease of use*, low external component count, and fast transient response. Auto-skip mode for high efficiency down to the milli-ampere load range, or PWM-only mode for low noise operation is selectable.

The current sensing scheme for positive overcurrent and negative overcurrent protection is loss-less low-side $R_{DS(on)}$ sensing plus temperature compensation. The device receives a 5-V (4.5 V to 5.5 V) supply from another regulator such as the TPS51120 or TPS51020. The conversion input can be either VBAT or a 5-V rail, ranging from 1.8 V to 28 V, and the output voltage range is from 0.75 V to 5.5 V.

The TPS51117 is available in a 14-pin QFN or a 14-pin TSSOP package and is specified from –40°C to 85°C.



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D-CAP is a trademark of Texas Instruments.

ORDERING INFORMATION(1) (2)

T_A	PACKAGE	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY	MINIMUM ORDER QUANTITY	ECO PLAN
–40°C to 85°C	PLASTIC TSSOP (PW)	TPS51117PW	14	Tube	90	Green (RoHS & no Sb/Br)
		TPS51117PWR		Tape-and-Reel	2000	
	PLASTIC QFN (RGY)	TPS51117RGYT	14	Tape-and-Reel	250	Green (RoHS & no Sb/Br)
		TPS51117RGYR			1000	

(1) All packaging options have Cu NIPDAU lead/ball finish.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Input voltage range	VBST	–0.3 to 36	V
	VBST (with respect to LL)	–0.3 to 6	
	EN_PSV, TRIP, V5DRV, V5FILT	–0.3 to 6	
	VOUT	–0.3 to 6	
	TON	–0.3 to 6	
Output voltage range	DRVH	–1 to 36	V
	DRVH (with respect to LL)	–0.3 to 6	
	LL	–1 to 30	
	PGOOD, DRVL	–0.3 to 6	
	PGND	–0.3 to 0.3	
T_A	Operating free-air temperature	–40 to 85	°C
T_{stg}	Storage temperature range	–55 to 150	°C
T_J	Junction temperature range	–40 to 125	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	Ta <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
14 Pin TSSOP	750 mW	7.5 mW/°C	300 mW
14 Pin QFN	1.3 W	13.0 mW/°C	520 mW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply input voltage range		4.5	5.5	V
Input voltage range	VBST	4.5	34	V
	VBST (with respect to LL)	4.5	5.5	
	EN_PSV, TRIP, V5DRV, V5FILT	–0.1	5.5	
	VOUT	–0.1	5.5	
	TON	–0.1	5.5	

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Output voltage range	DRVH	–0.8	34	V
	DRVH (with respect to LL)	–0.1	5.5	
	LL	–0.8	28	
	PGOOD, DRVL	–0.1	5.5	
	PGND	–0.1	0.1	
Operating free-air temperature, T_A		–40	85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{V5FILTPWM}$	Supply current	V5FILT + V5DRV current, PWM, EN_PSV = float, VFB = 0.77V, LL = –0.1 V		400	750	µA
$I_{V5FILTSKIP}$	Supply current	V5FILT + V5DRV current, auto-skip, EN_PSV = 5 V, VFB = 0.77V, LL = 0.5 V		250	470	µA
$I_{V5DRVSDN}$	V5DRV shutdown current	V5DRV current, EN_PSV = 0 V		0	1	µA
$I_{V5FILTSDN}$	V5FILT shutdown current	V5FILT current, EN_PSV = 0 V		4.5	7.5	µA
VOUT AND VFB VOLTAGES						
V_{OUT}	Output voltage	Adjustable output range	0.75		5.5	V
V_{VFB}	VFB regulation voltage			750		mV
V_{VFB_TOL}	VFB regulation voltage tolerance	T_A = 25°C, bandgap initial accuracy	–0.9%		0.9%	
		T_A = 0°C to 85°C	–1.3%		1.3%	
		T_A = -40°C to 85°C	–1.6%		1.6%	
I_{VFB}	VFB input current	V_{FB} = 0.75 V, absolute value		0.02	0.1	µA
R_{Dischg}	VOUT discharge resistance	EN_PSV = 0 V, V_{OUT} = 0.5 V		20	32	Ω
ON-TIME TIMER AND INTERNAL SOFT START						
T_{ONN}	Nominal on time	V_{LL} = 12 V, V_{OUT} = 2.5 V, R_{TON} = 250 kΩ		750		ns
T_{ONF}	Fast on time	V_{LL} = 12 V, V_{OUT} = 2.5 V, R_{TON} = 100 kΩ	264	330	396	ns
T_{ONS}	Slow on time	V_{LL} = 12 V, V_{OUT} = 2.5 V, R_{TON} = 400 kΩ		1169		ns
$T_{ON(MIN)}$	Minimum on time	V_{OUT} = 0.75 V, R_{TON} = 100 kΩ to 28 V [(1)]	80	110	140	ns
$T_{OFF(MIN)}$	Minimum off time	V_{FB} = 0.7 V, LL = -0.1 V, TRIP = open		440		ns
T_{SS}	Internal soft start time	Time from EN_PSV > 3 V to V_{FB} regulation value = 0.735 V	0.82	1.2	1.5	ms
OUTPUT DRIVERS						
R_{DRVH}	DRVH resistance	Source, $V_{VBST-DRVH}$ = 0.5 V		5	7	Ω
		Sink, $V_{DRVH-LL}$ = 0.5 V		1.5	2.5	Ω
R_{DRVL}	DRVL resistance	Source, $V_{V5DRV-DRVL}$ = 0.5 V		5	7	Ω
		Sink, $V_{DRVL-PGND}$ = 0.5 V		1.5	2.5	Ω
T_D	Dead time	DRVH-low (DRVH = 1 V) to DRVL-high (DRVL = 4 V), LL = –0.05 V	10	20	50	ns
		DRVL-low (DRVL = 1 V) to DRVH-high (DRVH = 4V), LL = –0.05 V	30	40	60	ns

(1) Design constraint, ensure actual on-time is larger than the max value (i.e., design R_{TON} such that the min tolerance is 100 kΩ).

ELECTRICAL CHARACTERISTICS (Continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL BST DIODE						
V_{FBST}	Forward voltage	$V_{V5DRV-VBST}$, IF = 10 mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakage current	VBST = 34 V, LL = 28 V		0.1	1	μA
UVLO/LOGIC THRESHOLD						
V_{UVLO}	V5FILT UVLO Threshold	Wake up	3.7	3.9	4.1	V
		Hysteresis	200	300	400	mV
V_{EN_PSV}	EN_PSV logic input voltage	EN_PSV low	0.7	1.0	1.3	V
		Hysteresis	150	200	250	mV
		EN_PSV float (set PWM_only mode)	1.7	1.95	2.25	V
		EN_PSV high (set Auto_skip mode)	2.4	2.65	2.9	V
		Hysteresis	100	175	250	mV
I_{EN_PSV}	EN_PSV source current	EN_PSV = GND, absolute value(1)		1		μA
POWERGOOD COMPARATOR						
V_{THPG}	PG threshold	PG in from lower (PGOOD goes high)	92.5%	95%	97.5%	
		PG low hysteresis (PGOOD goes low)	–4%	–5.5%	–7%	
		PG in from higher (PGOOD goes high)	102%	105%	107%	
		PG high hysteresis (PGOOD goes low)	4%	5.5%	7%	
I_{PGMAX}	PG sink current	PGOOD = 0.5 V	2.5	7.5		mA
T_{PGDEL}	PG delay	Delay for PGOOD in	45	63	85	μs
CURRENT SENSE						
I_{TRIP}	TRIP source current	V_{TRIP} < 0.3 V, T_A = 25°C	9	10	11	μA
T_{CITRIP}	ITRIP temperature coefffecient	On the basis of 25°C		4500		ppm/°C
V_{Rtrip}	Current limit threshold range setting range	$V_{TRIP-GND}$ voltage(1), all temperatures	30		200	mV
V_{OCLoff}	Overcurrent limit comparator offset	($V_{TRIP-GND}$-$V_{PGND-LL}$) voltage $V_{TRIP-GND}$ = 60 mV	–10	0	10	mV
V_{UCLoff}	Negative overcurrent limit comparator offset	($V_{TRIP-GND}$-$V_{LL-PGND}$) voltage $V_{TRIP-GND}$ = 60 mV, EN_PSV = float	–9.5	0.5	10.5	mV
V_{ZCoff}	Zero crossing comparator offset	$V_{PGND-LL}$ voltage, EN_PSV = 3.3 V	–9.5	0.5	10.5	mV
UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	VFB OVP trip threshold	OVP detect	111%	115%	119%	
T_{OVPDEL}	VFB OVP propagation delay	See (1)		1.5		μs
V_{UVP}	VFB UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis		10%		
T_{UVPDEL}	VFB UVP delay		22	32	42	μs
T_{UVPEN}	UVP enable delay	After 1.7 × T_{SS}, UVP protection engaged	1.4	2	2.6	ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		160		°C
		Hysteresis(1)		12		°C

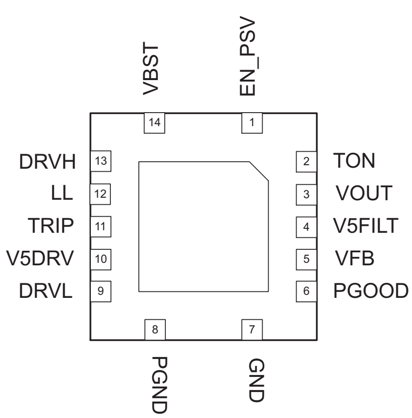
(1) Ensured by design. Not production tested.

DEVICE INFORMATION

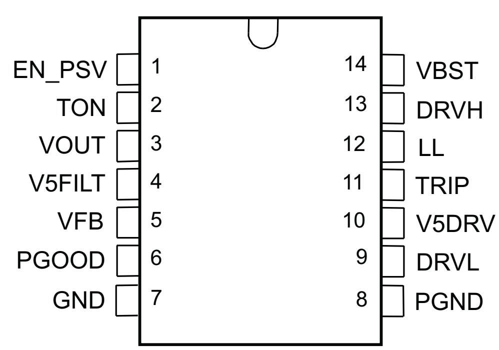
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DRVH	13	O	High-side NFET gate driver output. Source 5 Ω, sink 1.5 Ω LL-node referenced driver. Drive voltage corresponds to VBST to LL voltage.
DRVL	9	O	Rectifying (low-side) NFET gate driver output. Source 5 Ω, sink 1.5 Ω PGND referenced driver. Drive voltage is V5DRV voltage.
EN_PSV	1	I	Enable/power save pin. Connect to ground to disable SMPS. Connect to 3.3 V or 5 V to turn on SMPS and activate skip mode. Float to turn on SMPS but disable skip mode (forced continuous conduction mode).
GND	7	I	Signal ground pin.
LL	12	I/O	High-side NFET gate driver return. Also serves as anode of overcurrent comparator.
PGND	8	I/O	Ground return for rectifying NFET gate driver. Also cathode of overcurrent protection and source node of the output discharge switch.
PGOOD	6	O	Power-good window comparator, open-drain, output. Pull up to 5-V rail with a pull-up resistor. Current capability is 7.5 mA.
TON	2	I	On-time / frequency adjustment pin. Connect to LL with 100-kΩ to 600-kΩ resistor.
TRIP	11	I	Overcurrent trip point set input. Connect resistor from this pin to signal ground to set threshold for both overcurrent and negative overcurrent limit.
VBST	14	I	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to LL-node. An internal PN diode is connected between V5DRV to this pin. Designer can add external schottky diode if forward drop is critical to drive the power NFET.
VFB	5	I	SMPS voltage feedback input. Connect the resistor divider here for adjustable output.
VOUT	3	I	Connect to SMPS output. This terminal serves two functions: output voltage monitor for on-time adjustment, and input for the output discharge switch.
V5DRV	10	I	5-V Power supply input for FET gate drivers. Internally connected to VBST by a PN diode. Connect 1 μF or more between this pin and PGND to support instantaneous current for gate drivers.
V5FILT	4	I	5-V Power supply input for all the control circuitry except gate drivers. Supply 5-V ramp rate should be 17 mV/μs or less and T_j < 85°C to secure safe start-up of the internal reference circuit. Apply RC filter consists of 300 Ω + 1 μF or 100 Ω + 4.7 μF at the pin input.

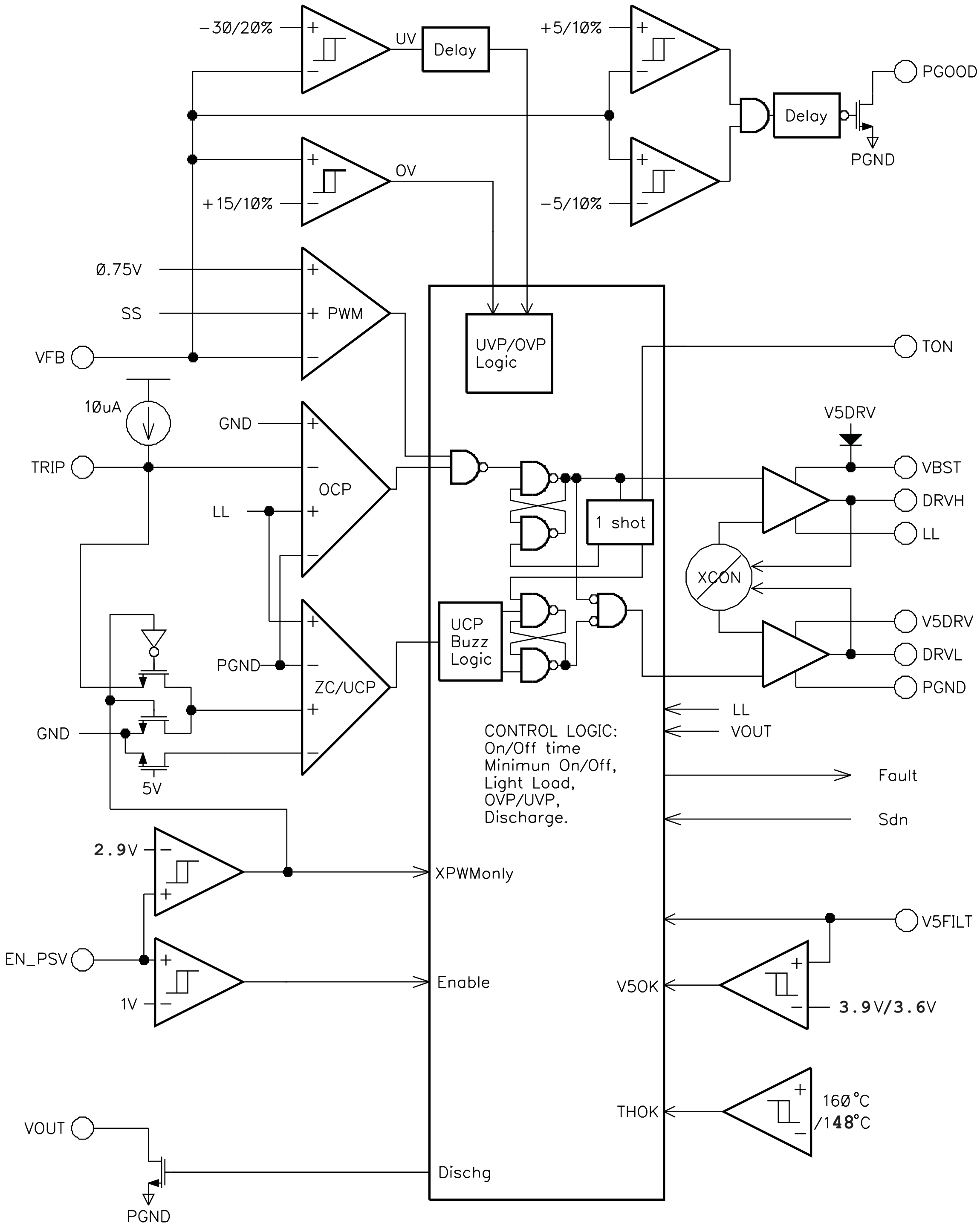
QFN (RGY) PACKAGE (BOTTOM VIEW)



TSSOP (PW) PACKAGE (TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

PWM OPERATION

The main control loop of the TPS51117 is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports proprietary D-CAP™ Mode that uses an internal compensation circuit and is suitable for minimal external component count configuration when an appropriate amount of ESR at the output capacitor(s) is allowed. Basic operation of D-CAP Mode can be described as follows.

DETAILED DESCRIPTION (continued)

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or becomes *ON* state. This MOSFET is turned off, or becomes *OFF* state, after the internal one shot timer expires. This one shot is determined by V_{IN} and V_{OUT} to keep the frequency fairly constant over the input voltage range at steady state, hence it is called adaptive on-time control or *fixed frequency emulated* on-time control (see *PWM frequency and Adaptive On-Time Control*). The MOSFET is turned on again when both feedback information, monitored at V_{FB} voltage, indicates insufficient output voltage *AND* inductor current information indicates below the overcurrent limit. Repeating the operation in this manner, the controller regulates the output voltage. The synchronous low-side or *rectifying* MOSFET is turned on each *OFF* state to keep the conduction loss to a minimum.

The TPS51117 supports selectable PWM-only and auto-skip operation modes. If EN_PSV is grounded, the switching regulator is disabled. If the EN_PSV pin is connected to 3.3 V or 5 V, the regulator is enabled with auto-skip mode selected. The rectifying MOSFET is turned off when inductor current information detects zero level. This enables a seamless transition to reduced frequency operation during a light load condition so that high efficiency is maintained over a broad range of load currents. If the EN_PSV pin is floated, it is internally pulled up to 1.95 V, and the regulator is enabled with PWM-only mode selected. The rectifying MOSFET is not turned off when inductor current reaches zero. The converter runs forced continuous conduction mode for the entire load range. System designers may want to use this mode to avoid a certain frequency during a light load condition but with the cost of low efficiency. However, be aware the output has the capability to both source and sink current in this mode. If the output terminal is connected to a voltage source higher than the regulator's target, the converter sinks current from the output and boosts the charge into the input capacitor. This may cause unexpected high voltage at VIN and may damage the power FETs.

DC output voltage can be set by the external resistor divider as follows (refer to Figure 23, Figure 24, and Figure 25).

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times 0.75\ V \tag{1}$$

LIGHT LOAD CONDITION WITH AUTO-SKIP FUNCTION

If auto-skip mode is selected, the TPS51117 automatically reduces the switching frequency during a light load condition to maintain high efficiency. This reduction of frequency is achieved smoothly and without an increase of V_{out} ripple or load regulation. Detailed operation is described as follows. As the output current decreases from a heavy load condition, the inductor current is also reduced and eventually comes to the point that its *valley* touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when this zero inductor current is detected. Since the output voltage is still higher than the reference at this moment, both high-side and low-side MOSFETs are turned off and wait for the next cycle. As the load current decreases further, the converter runs in discontinuous conduction mode, taking longer time to discharge the output capacitor below the reference voltage. Note the ON time is kept the same as during the heavy load condition. In reverse, when the output current increases from a light load to a heavy load, the switching frequency increases to the preset value as the inductor current reaches to the continuous conduction. The transition load point to light load operation, $I_{OUT(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode), can be calculated as follows:

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{2}$$

where f_{sw} is the PWM switching frequency.

Switching frequency versus output current in the light load condition is a function of L, f_{sw}, V_{IN} and V_{OUT}, but it decreases almost proportional to the output current from the $I_{OUT(LL)}$ given above. For example, it is about 60 kHz at $I_{OUT(LL)}/5$ if the PWM switching frequency is 300 kHz.

DETAILED DESCRIPTION (continued)

PWM FREQUENCY AND ADAPTIVE ON-TIME CONTROL

The TPS51117 employs an adaptive on-time control scheme and does not have a dedicated oscillator on board. However, the device emulates a constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The ON time is controlled inverse proportional to the input voltage, and proportional to the output voltage, so that the duty ratio is kept as V_{OUT}/V_{IN} technically with the same cycle time. Equation 3 shows a simplified calculation of the on time.

$$T_{ON} = 19 \times 10^{-12} \times R_{TON}\left(\frac{(2/3)V_{OUT} + 100\text{ mV}}{V_{IN}}\right) + 50\text{ ns} \tag{3}$$

Here, R_{TON} is the external resistor connected from TON pin to the LL node. In the equation, 19 pF represents the internal timing capacitor with some typical parasitic capacitance at the TON pin. Also, 50 nsec is the turn-off delay time contributed by the internal circuit and that of the high-side MOSFET. Although this equation provides a good approximation to start with, the accuracy depends on each design and selection of the high-side MOSFET. Figure 1 shows the relationship of R_{TON} to the switching frequency.

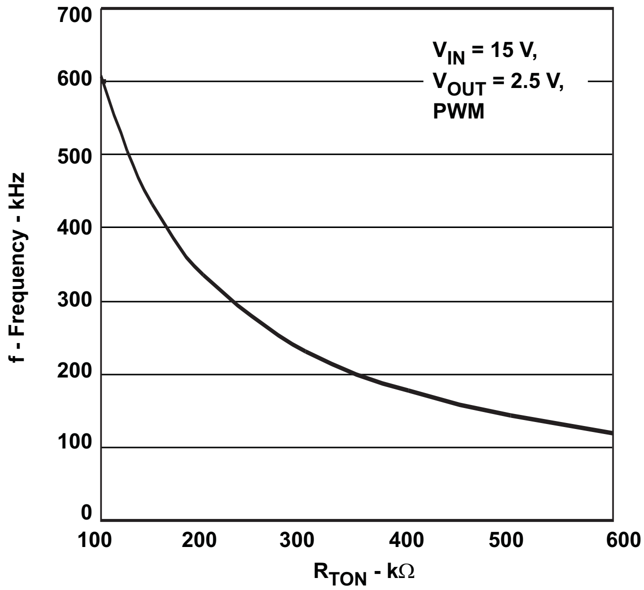


Figure 1. Switching Frequency vs R_{TON}

The TPS51117 does not have a pin connected to VIN, but the input voltage information comes from the switch node (LL node) during the *ON* state. An advantage of LL monitoring is that the loss in the high-side NFET is now a part of the on-time calculation, thereby making the frequency more stable with load.

Another consideration about frequency is jitter. Jitter may be caused by many reasons, but the constant on-time D-CAP mode scheme has some amount of inherent jitter. Since the output voltage ripple height is in the range of a couple of tens of milli-volts. A milli-volt order of noise on the feedback signal can affect the frequency by a few to ten percent. This is normal operation and has little harm to the power supply performance.

LOW-SIDE DRIVER

The low-side driver is designed to drive high-current, low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which is 5 Ω for V5DRV to DRVL and 1.5 Ω for DRVL to PGND. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. A 5-V bias voltage is delivered from V5DRV supply. The average drive current is calculated by the FET gate charge at V_{gs} = 5 V times the switching frequency. The instantaneous drive current is supplied by an input capacitor connected between V5DRV and GND.

DETAILED DESCRIPTION (continued)

HIGH-SIDE DRIVER

The high-side driver is designed to drive high-current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, 5-V bias voltage is delivered from V5DRV supply. An internal PN diode is connected between V5DRV to VBST. The designer can add an external schottky diode if forward drop is critical to drive the high-side NFET or to achieve the last one percent efficiency improvement. The average drive current is also estimated by the gate charge at V_{gs} = 5 V times the switching frequency. The instantaneous drive current is supplied by the flying capacitor between the VBST pin and LL pin. The drive capability is represented by its internal resistance, which is 5 Ω for VBST to DRVH and 1.5 Ω for DRVH to LL.

SOFTSTART

The TPS51117 has an internal, 1.2-ms, voltage servo softstart with overcurrent limit. When the EN_PSV pin becomes high, an internal DAC begins ramping up the reference voltage to the error amplifier. Smooth control of the output voltage is maintained during start up.

POWERGOOD

The TPS51117 has power-good output. PGOOD is an open drain 7.5-mA pull-down output. This pin should be typically connected to a 5-V power supply node through a 100-kΩ resistor. The power-good function is activated after the soft start has finished. If the output voltage becomes within ±5% of the target value, internal comparators detect the power-good state and the power-good signal becomes high after a 64-µs internal delay. If the output voltage goes outside ±10% of the target value, the power-good signal becomes low immediately.

OUTPUT DISCHARGE CONTROL (SOFTSTOP)

The TPS51117 discharges output when EN_PSV is low or the converter is in a fault condition (UVP, OVP, UVLO, or thermal shutdown). The TPS51117 discharges output using an internal 20-Ω MOSFET which is connected to VOUT and PGND. The discharge time-constant is a function of the output capacitance and resistance of the discharge transistor.

OVERCURRENT LIMIT

The TPS51117 has cycle-by-cycle overcurrent limiting control. Inductor current is monitored during the *OFF* state and the controller keeps the *OFF* state when inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and a cost effective solution, the TPS51117 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. The TRIP terminal sources 10-µA I_{TRIP} current, and the trip level is set to the OCL trip voltage, V_{TRIP} as in the following equation.

$$V_{TRIP}(mV) = R_{TRIP}(k\Omega) \times 10\ (\mu A) \tag{4}$$

Inductor current is monitored by the voltage between the PGND pin and the LL pin so the LL pin should be connected to the drain terminal of the low-side MOSFET. I_{TRIP} has 4500 ppm/°C temperature coefficient to compensate the temperature dependency of the $R_{DS(on)}$. PGND is used as the positive current sensing node so PGND should be connected to the source terminal of the bottom MOSFET.

As the comparison is done during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at overcurrent threshold, I_{ocp}, can be calculated as follows;

$$I_{ocp} = V_{TRIP}/R_{DS(on)} + I_{ripple}/2 = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{5}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall. Eventually it crosses the undervoltage protection threshold and shutdown.

DETAILED DESCRIPTION (continued)

NEGATIVE OVERCURRENT LIMIT (PWM-ONLY MODE)

The TPS51117 also supports cycle-by-cycle negative overcurrent limiting in PWM-only mode. The overcurrent limit is set to be negative but is the same absolute value as the positive overcurrent limit. If output voltage continues to rise, the bottom MOSFET stays on, thus inductor current is reduced and reverses direction after it reaches zero. When there is too much negative current in the inductor, the bottom MOSFET is turned off and the current flows to VIN through the body diode of the top MOSFET. Because this protection reduces current to discharge the output capacitor, output voltage tends to rise, eventually hitting the overvoltage protection threshold and shutdown. In order to prevent false OVP from triggering, the bottom MOSFET is turned on again 400 ns after it is turned off. If the device hits the negative overcurrent threshold again before output voltage is discharged to the target level, the bottom MOSFET is turned off and the process repeats, which is called *NOCL Buzz*. It ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output voltage is discharged to the target level before the NOCL threshold is reached, the bottom MOSFET is turned off, the top MOSFET is then turned on, and the device resumes normal operation.

OVERVOLTAGE PROTECTION

The TPS51117 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage condition. When the feedback voltage becomes higher than 115% of the target value, the top MOSFET is turned off and the bottom MOSFET is turned on immediately. The output is also discharged by the internal 20-Ω transistor. Also, the TPS51117 monitors VOUT terminal voltage directly and if it becomes greater than 5.75 V, it turns off the top MOSFET driver.

UNDERVOLTAGE PROTECTION

When the feedback voltage becomes lower than 70% of the target value, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 32 μs, the TPS51117 latches off the high-side and low-side MOSFETs and discharges the output with the internal 20-Ω transistor. This function is enabled after 2 ms from when EN_PSV is brought high, i.e., UVP is disabled during start up.

START UP SEQUENCE

Referring to Figure 2 which illustrates the timing sequence, to guarantee the proper startup the TPS51117, always ensure that V_{EN_PSV} is less or equal to that of V_{V5FILT} prior to V_{V5FILT} reaching V_{UVLO}.

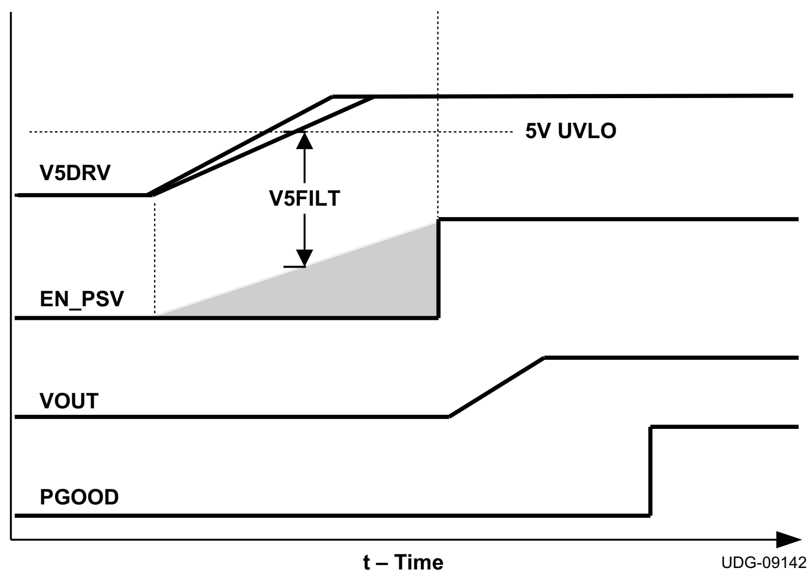


Figure 2. Startup Timing Sequence

DETAILED DESCRIPTION (continued)

UVLO PROTECTION

The TPS51117 has V5FILT undervoltage lockout protection (UVLO). When the V5FILT voltage is lower than the UVLO threshold voltage, the TPS51117 is shut off. This is a nonlatched protection.

THERMAL SHUTDOWN

The TPS51117 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 160°C), the TPS51117 shuts itself off. Both top and bottom gate drivers are tied low with output discharged through the VOUT terminal. This is also a nonlatched protection. The device recovers once the temperature has decreased approximately 12°C.

TYPICAL CHARACTERISTICS

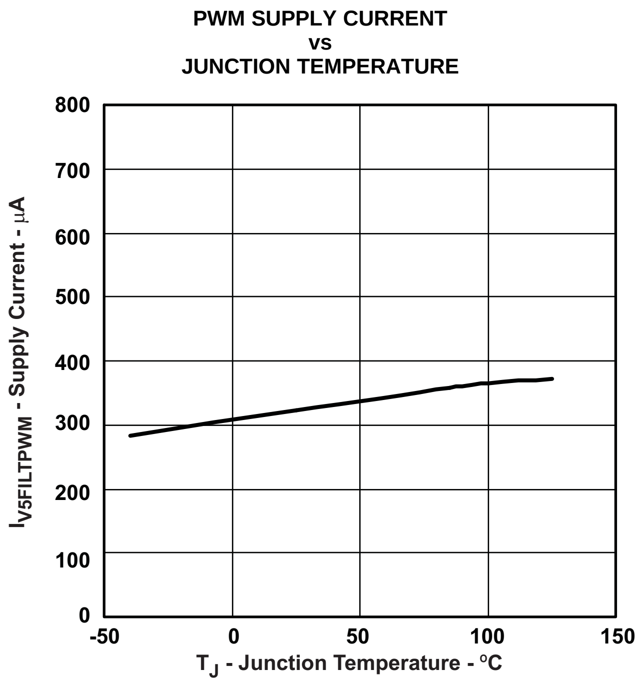


Figure 3.

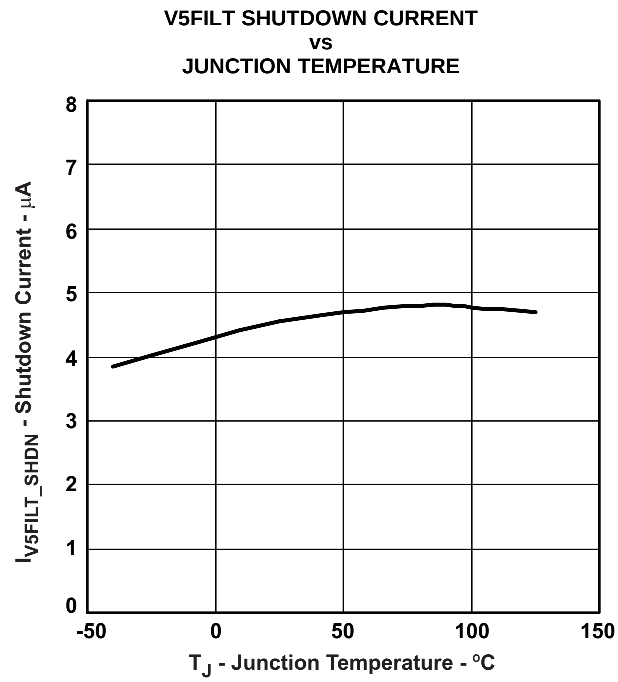


Figure 4.

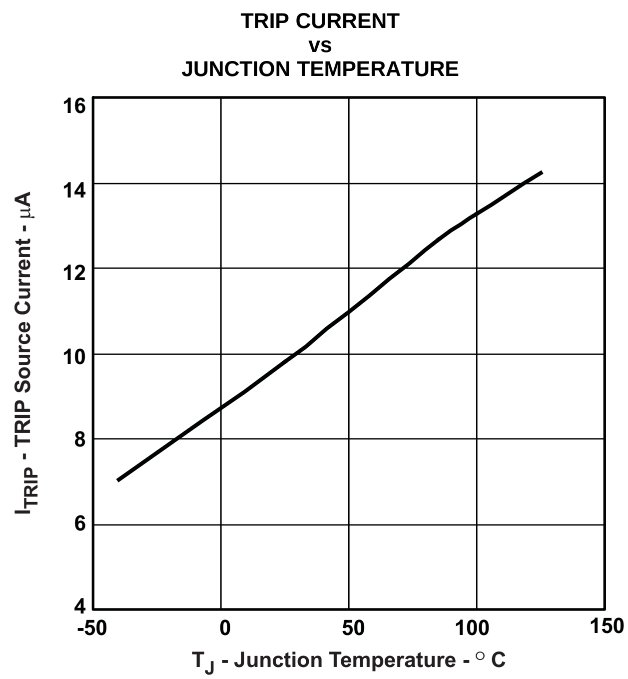


Figure 5.

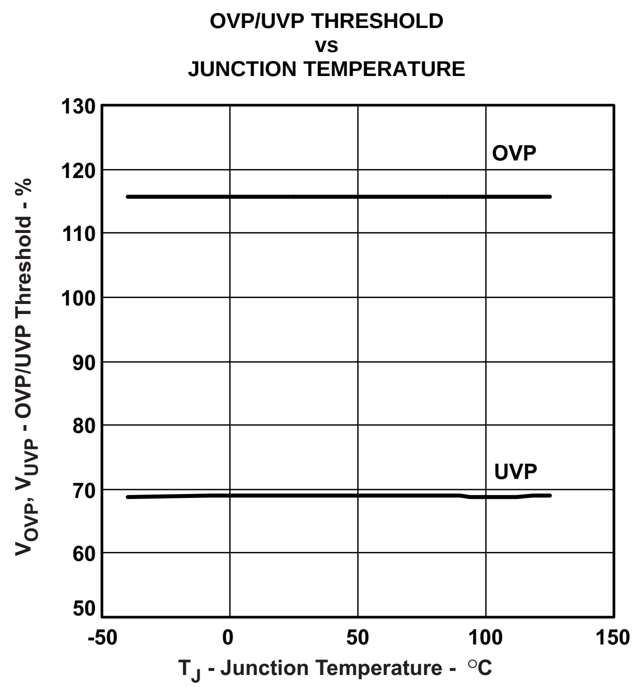


Figure 6.

TYPICAL CHARACTERISTICS (continued)

MEASURED SWITCHING FREQUENCY vs TON RESISTANCE

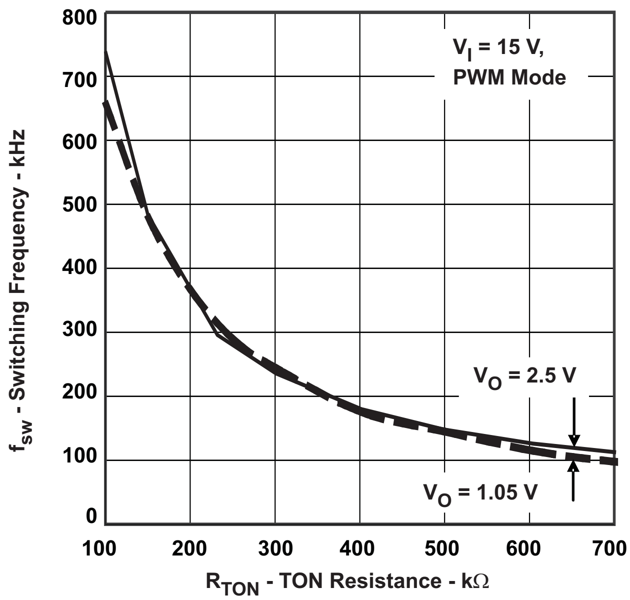


Figure 7.

SWITCHING FREQUENCY vs INPUT VOLTAGE

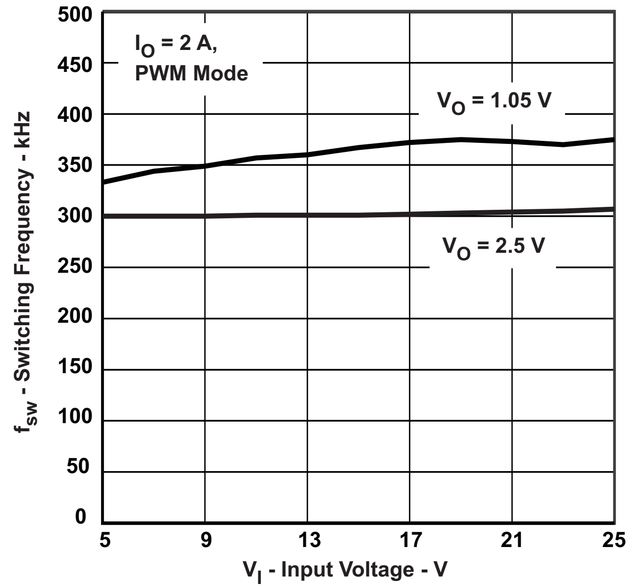


Figure 8.

SWITCHING FREQUENCY vs OUTPUT CURRENT (1.05 V)

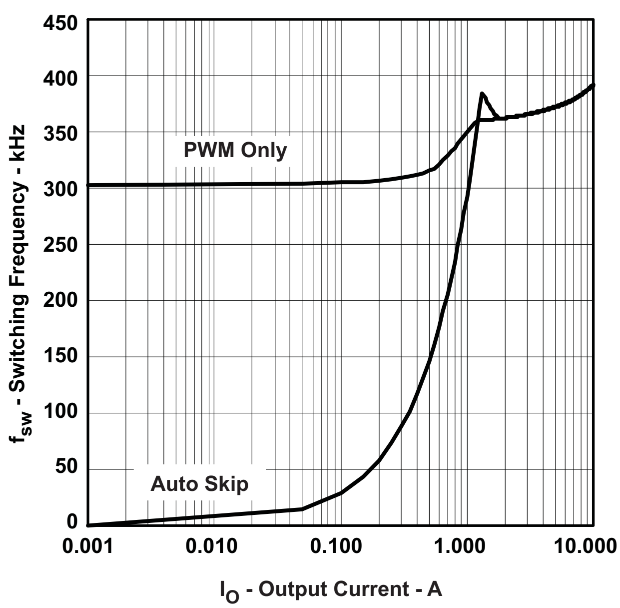


Figure 9.

SWITCHING FREQUENCY vs OUTPUT CURRENT (2.5 V)

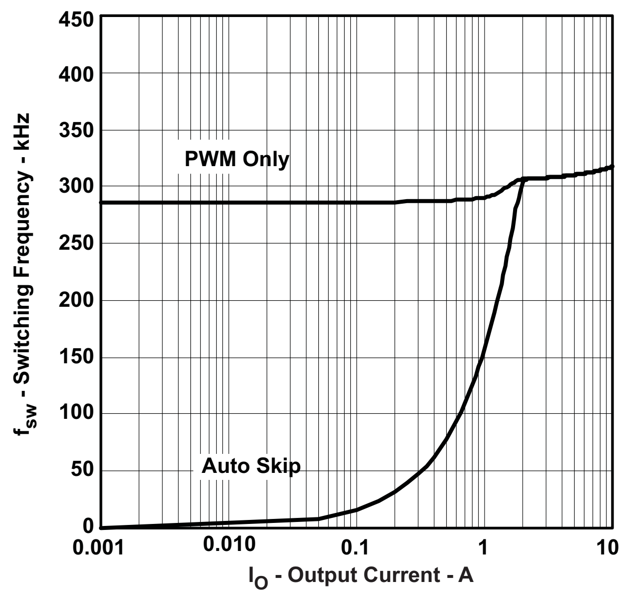


Figure 10.

TYPICAL CHARACTERISTICS (continued)

1.05 V OUTPUT VOLTAGE vs OUTPUT CURRENT

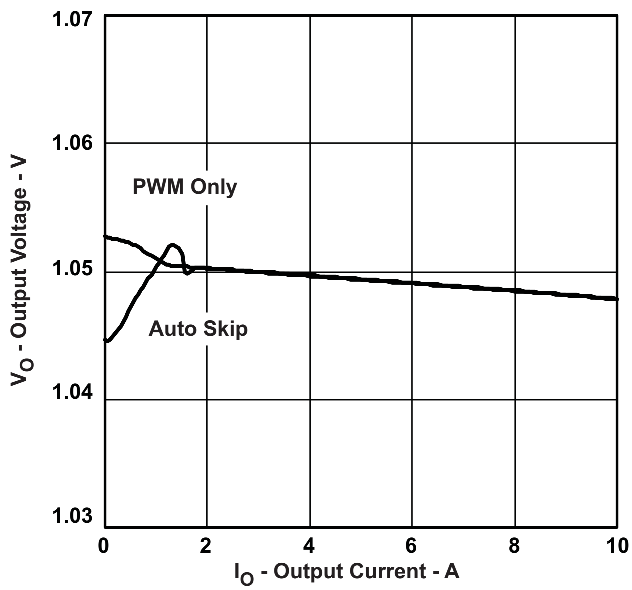


Figure 11.

2.5 V OUTPUT VOLTAGE vs OUTPUT CURRENT

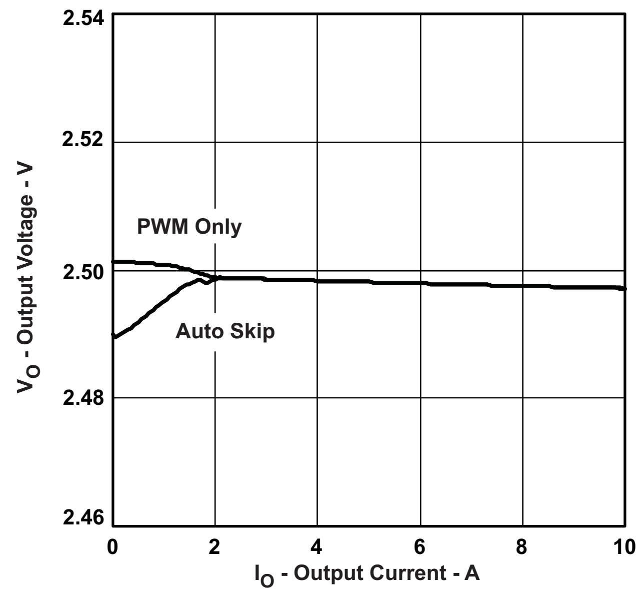


Figure 12.

1.05 V OUTPUT VOLTAGE vs INPUT VOLTAGE

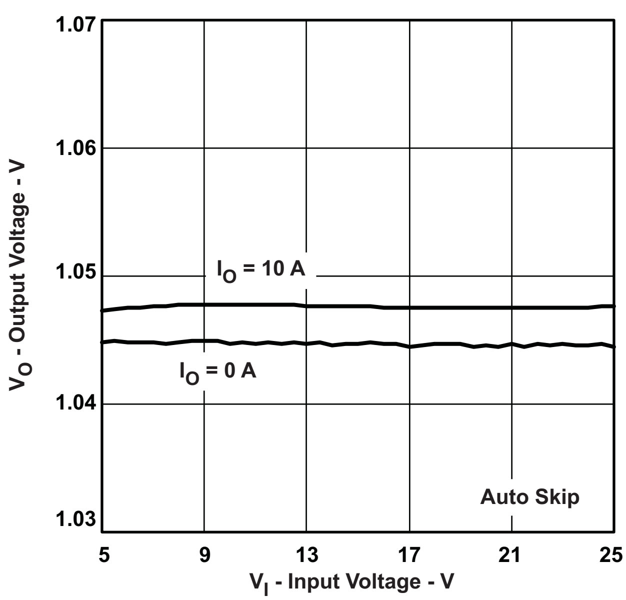


Figure 13.

2.5 V OUTPUT VOLTAGE vs INPUT VOLTAGE

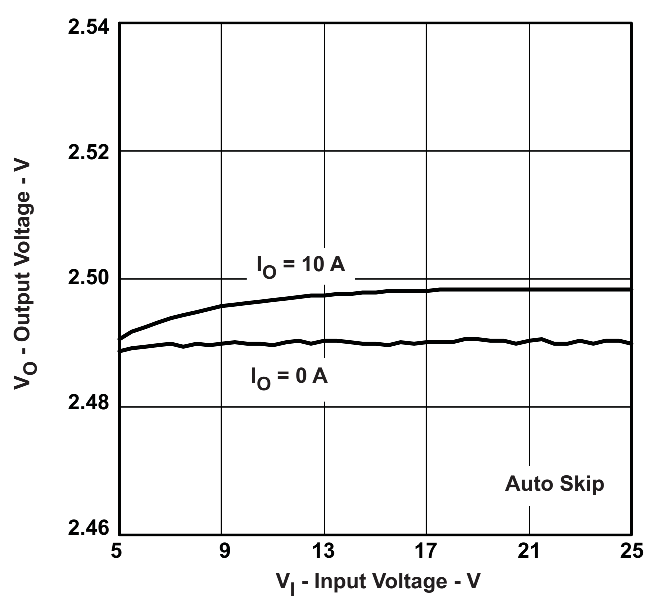


Figure 14.

TYPICAL CHARACTERISTICS (continued)

1.05 V EFFICIENCY vs OUTPUT CURRENT

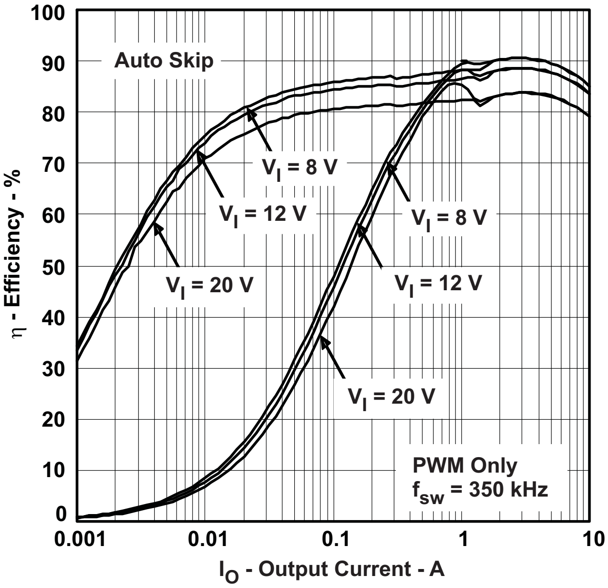


Figure 15.

2.5 V EFFICIENCY vs OUTPUT CURRENT

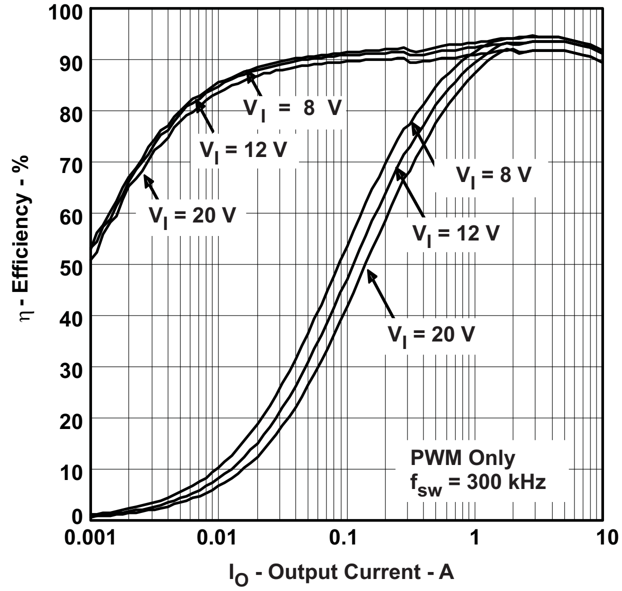


Figure 16.

1.05 V LOAD TRANSIENT RESPONSE

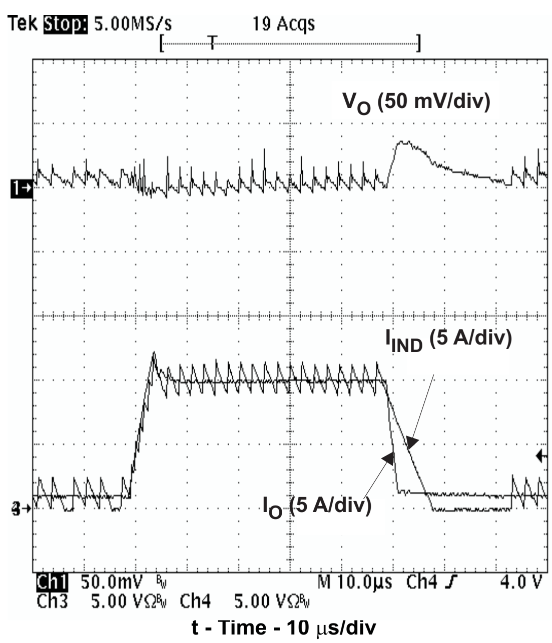


Figure 17.

2.5 V LOAD TRANSIENT RESPONSE

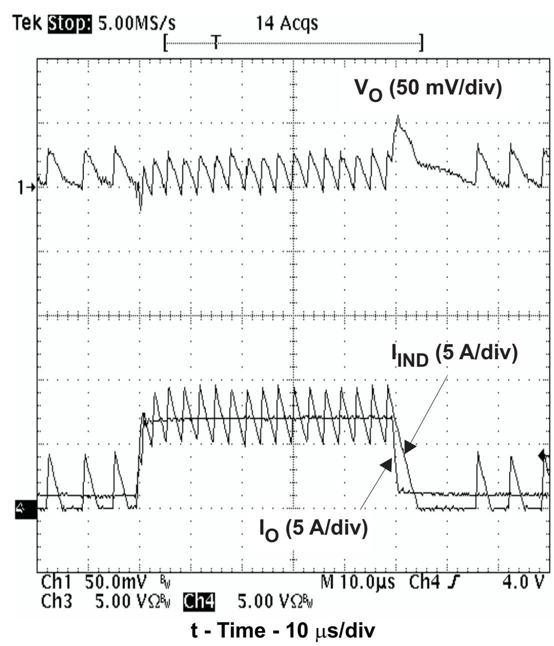


Figure 18.

TYPICAL CHARACTERISTICS (continued)

MODE TRANSITION AUTO-SKIP TO PWM

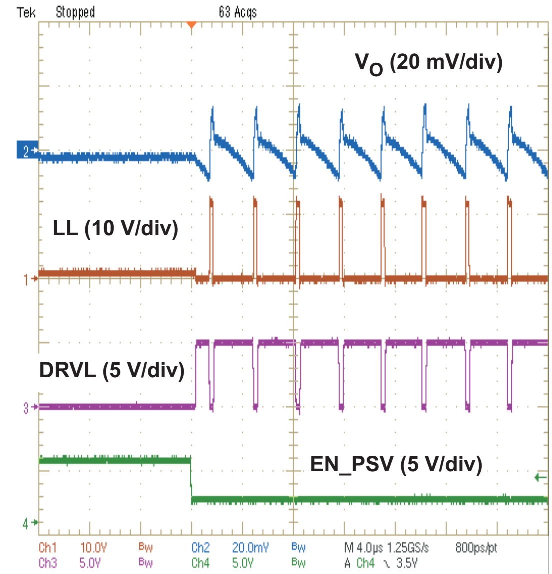


Figure 19.

MODE TRANSITION PWM TO AUTO-SKIP

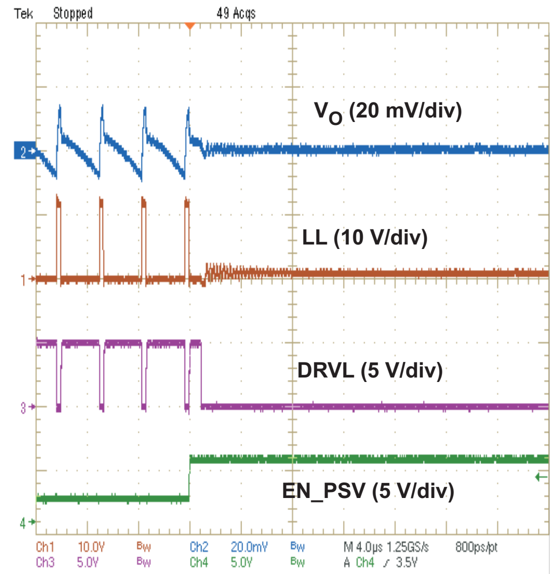
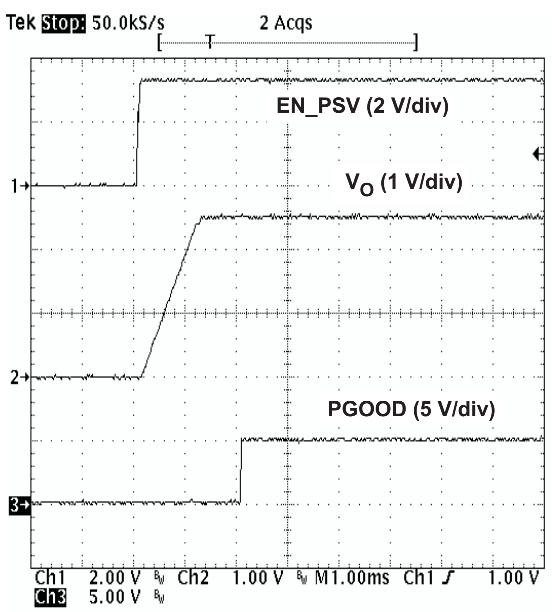


Figure 20.

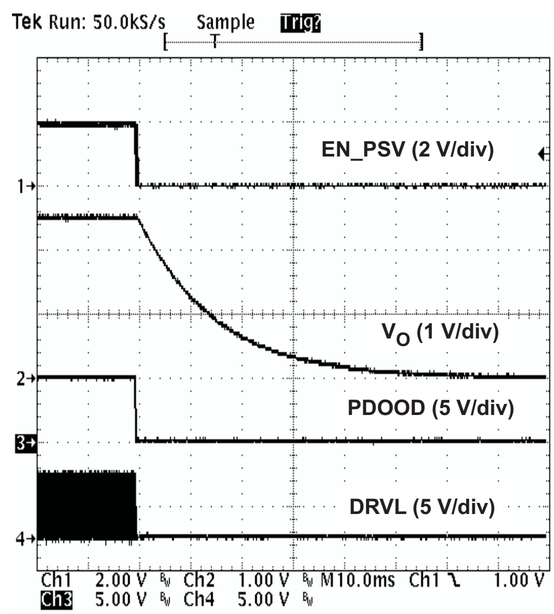
2.5 V START-UP WAVEFORMS



t - Time - 1 ms/div

Figure 21.

2.5 SHUTDOWN WAVEFORMS



t - Time - 10 ms/div

Figure 22.

APPLICATION INFORMATION

LOOP COMPENSATION AND EXTERNAL PARTS SELECTION

D-CAP™ Mode Operation

A buck converter system using D-CAP™ Mode can be simplified as shown in Figure 23.

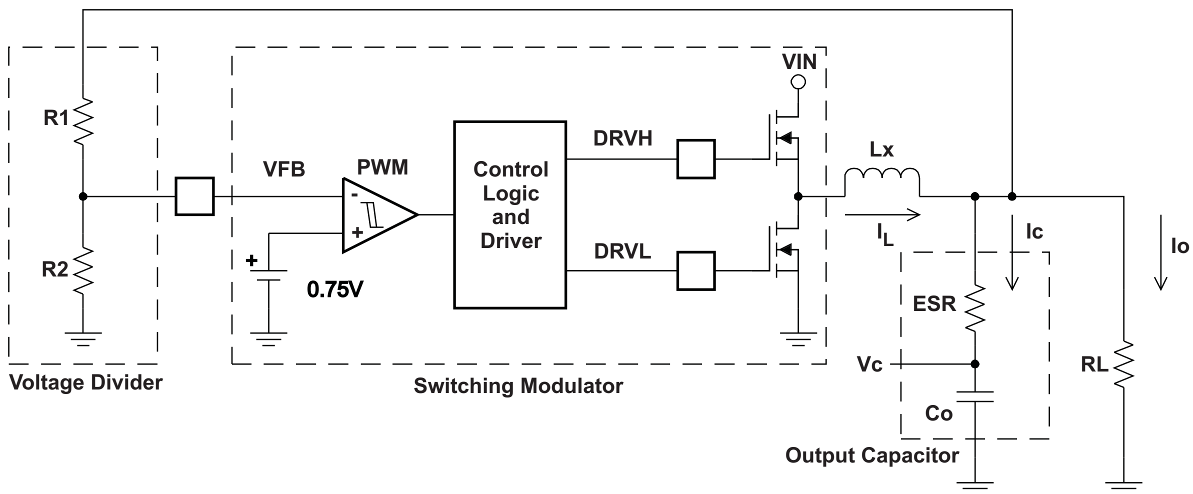


Figure 23. Simplified Diagram of the Modulator

The VFB voltage is compared with the internal reference voltage after the divider resistors. The PWM comparator determines the timing to turn on the top MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The DC output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increases.

For loop stability, the 0 dB frequency, f_0, defined in the follow equation must be lower than 1/4 of the switching frequency.

$$f_O = \frac{1}{2\pi \times ESR \times Co} \le \frac{f_{SW}}{4} \quad (6)$$

As f_0 is determined solely by the output capacitor characteristics, loop stability of D-CAP™ Mode is determined by capacitor chemistry. For example, specialty polymer capacitors (SP-CAP) have Co in the order of several 100 µF and ESR in range of 10 mΩ. These values make f_0 in the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this operational mode.

Although D-CAP™ Mode provides many advantages such as ease-of-use, minimum external component configuration, and extremely short response time, due to not employing an error amplifier in the loop, a sufficient feedback signal needs to be provided by an external circuit to reduce the jitter level. The required signal level is approximately 15 mV at the comparing point. This generates $V_{ripple} = (V_{OUT}/0.75) \times 15$ mV at the output node. The output capacitor ESR should meet this requirement.

The external component selection is simple in D-CAP™ Mode:

1. Determine the value of R1 and R2

   The recommended R2 value is 10 kΩ to 100 kΩ. Calculate R1 by Equation 7.

$$R1 = \frac{\left(V_{OUT} - 0.75\right)}{0.75} \times R2 \quad (7)$$

2. Choose R_{TON}

Switching frequency is usually determined by the overall view of the DC-DC converter design of: size, efficiency or cost, and mostly dictated by external component constraints such as the size of inductor and/or output capacitor. In the case where an extremely low or high duty factor is expected, the minimum on-time or off-time also needs to be considered to satisfy the required duty factor. Once the switching frequency is decided, R_{TON} can be determined by Equation 8 and Equation 9,

$$T_{ON(max)} = \frac{1}{f} \times \frac{V_{OUT}}{V_{IN(min)}} \tag{8}$$

$$R_{TON} = \frac{3}{2} \times \frac{\left(T_{ON(max)} - 50\text{ ns}\right)}{19 \times 10^{-12}} \times \frac{V_{IN(min)}}{\left(V_{OUT} + 150\text{ mV}\right)}\ [\Omega] \tag{9}$$

3. Choose inductor

A good starting point inductance value is where the ripple current is approximately 1/4 to 1/2 of the maximum output current.

$$L_{IND} = \frac{1}{I_{IND(ripple)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{10}$$

For applications that require fast transient response with minimum V_{OUT} overshoot, consider a smaller inductance than above. The cost of a small inductance value is higher steady state ripple, larger line regulation, and higher switching loss.

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated as follows.

$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{L \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{11}$$

4. Choose output capacitor(s)

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine ESR to meet the required ripple voltage above. A quick approximation is shown in Equation 12.

$$ESR = \frac{V_{OUT} \times 0.015}{I_{ripple} \times 0.75} \approx \frac{V_{OUT}}{I_{OUT(max)}} \times 60\ [m\Omega] \tag{12}$$

5. Choose MOSFETs

Loss-less current sensing and overcurrent protection of the TPS51117 is determined by $R_{DS(on)}$ of the low-side MOSFET. So, $R_{DS(on)}$ times the inductor current value at the overcurrent point should be in the range of 30 mV to 200 mV for the entire operational temperature range. Assuming a 20% guard band, $R_{DS(on)}$ in the following equation should satisfy the full temperature range.

$$\frac{30\text{ mV}}{1.2 \times I_{OUT(max)} - 0.5 \times I_{ripple}} \le R_{DS(on)} \le \frac{200\text{ mV}}{1.2 \times I_{OUT(max)} - 0.5 \times I_{ripple}} \tag{13}$$

6. Choose R_{trip}

Once the low-side FET is decided, select an appropriate R_{trip} value that provides V_{trip} equal to $R_{DS(on)}$ times I_{peak}.

7. LPF for V5FILT

In order to reject high frequency noise and also secure safe start-up of the internal reference circuit, apply 1 µF of MLCC closely at the V5FILT pin with a 300-Ω resistor to create a LPF between +5-V supply and the pin.

8. VBST capacitor, VBST diode

Apply 0.1-μF MLCC between VBST and the LL node as the flying capacitor for the high-side FET driver. The TPS51117 has its own boost diode on-board between V5DRV and VBST. This is a PN junction diode and strong enough for most typical applications. However, in case efficiency has priority over cost, the designer may add a Schottky diode externally to improve gate drive voltage of the high-side FET. A Schottky diode has a higher leakage current, especially at high temperature, than a PN junction diode. A low leakage diode should be selected in order to maintain VBST voltage during low frequency operation in skip mode.

THERMAL CONSIDERATION

Power dissipation of the TPS51117 is mainly generated from the FET drivers. Average drive current can be estimated by gate charge, Q_g, times the switching frequency.

$$I_G = Q_g \times f_{SW} \tag{14}$$

Q_g is the charge needed to charge gate capacitance up to the V5DRV voltage of 5 V. Actual values are shown on MOSFET datasheets provided by the manufacturer. Total power dissipation, therefore, to drive the top and bottom MOSFETs can be calculated by the following equation Equation 15.

$$W_{DRIVE} = V_{V5DRV} \times \left(Q_{g(top)} + Q_{g(btm)}\right) \times f_{SW} \tag{15}$$

This power plus a small amount of dissipation (less than 5 mW) from controller circuitry needs to be effectively dissipated from the package. Maximum power dissipation allowed for the package is calculated by:

$$W_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}} \tag{16}$$

Where

- $T_{J(max)}$ is 125°C
- $T_{A(max)}$ is the maximum ambient temperature in the system
- θ_{JA} is the thermal resistance from the silicon junction to the ambient

This thermal resistance strongly depends on board layout. The TPS51117 is assembled in a standard TSSOP package and the heat mainly moves to the board through its leads.

LAYOUT CONSIDERATIONS

Certain points must be considered before starting a layout work using the TPS51117.

- Connect the RC low-pass filter from 5-V supply to V5FILT, 300 Ω and 1 μF are recommended. Place the filter capacitor close to the device, within 12 mm (0.5 inches) if possible.
- Connect the overcurrent setting resistors from TRIP to GND close to the device, right next to the device, if possible. The trace from TRIP to resistor and resistor to GND should avoid coupling to a high voltage switching node.
- The discharge path (VOUT) should have a dedicated trace to the output capacitor(s); separate from the output voltage sensing trace, and use a 1,5 mm (60 mils) or wider trace with no loops. Make sure the feedback current setting resistor (the resistor between VFB to GND) is tied close to the device GND. The trace from this resistor to the VFB pin should be short and thin. Place on the component side and avoid vias between this resistor and the device.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use a 0.65 mm (25 mils) or wider trace.
- All sensitive analog traces and components such as VOUT, VFB, GND, EN_PSV, PGOOD, TRIP, V5FILT, and TON should be placed away from high-voltage switching nodes such as LL, DRVL, DRVH or VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- Gather the ground terminals of the V_{IN} capacitor(s), V_{OUT} capacitor(s), and the source of the low-side MOSFETs as close as possible. GND (signal ground) and PGND (power ground) should be connected strongly together near the device. The PCB trace defined as LL node, which connects to the source of the high-side MOSFET, the drain of the low-side MOSFET, and the high-voltage side of the inductor, should be as short and wide as possible.

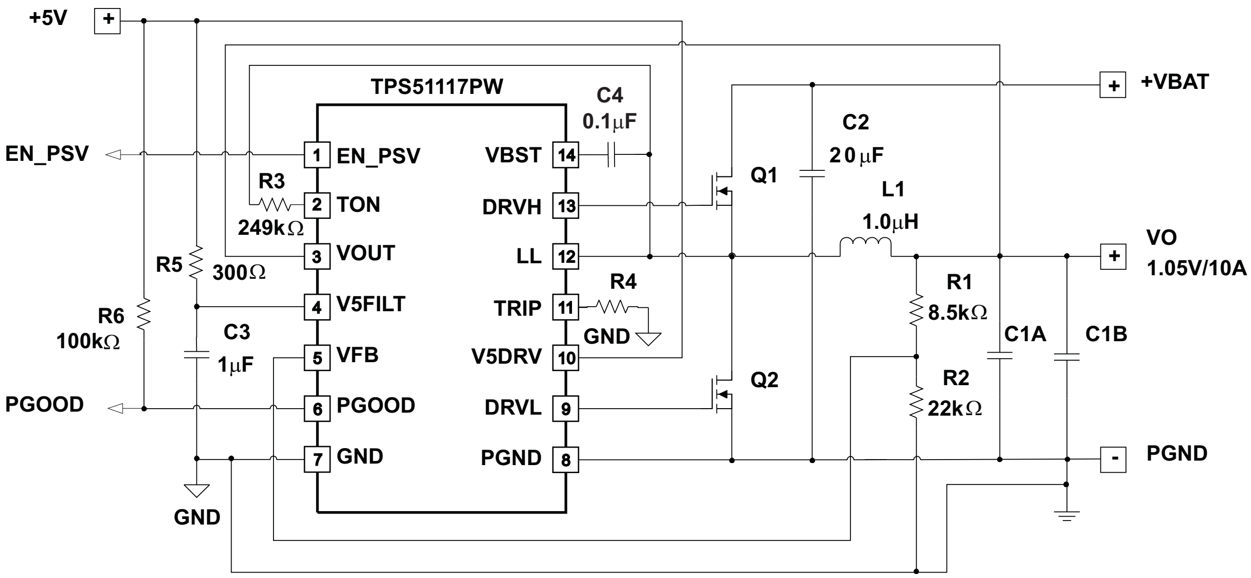


Figure 24. 1.05-V/10-A Application From VBAT (PW Package)

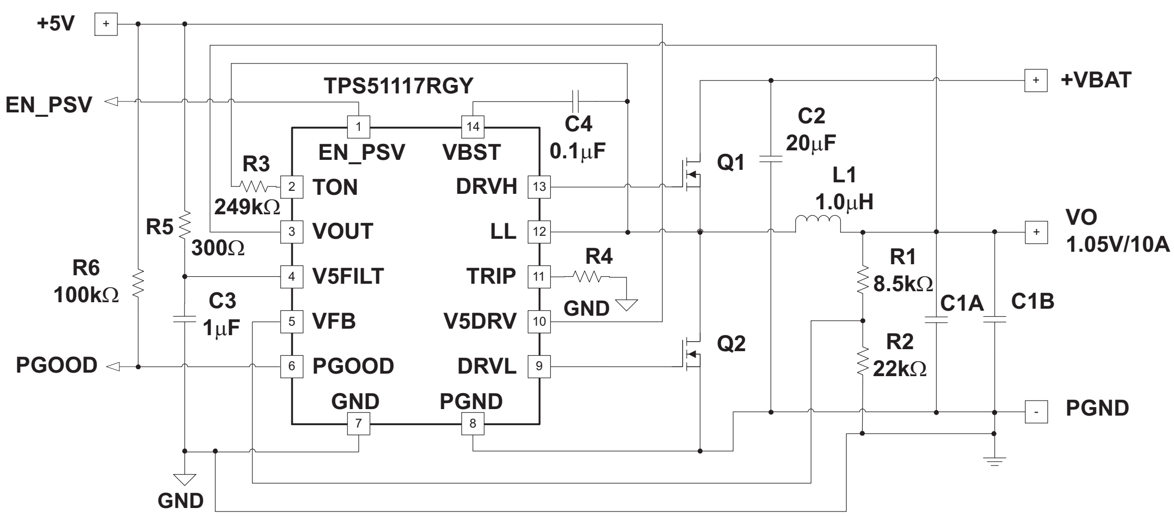


Figure 25. 1.05-V/10-A Application From VBAT (RGY Package)

Table 1. Typical Application Circuit Components

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C1A, C1B	470 µF, 2.5 V, 12 mΩ	SANYO	2R5TPE470MC
C2	10 µF, 25 V, 2 pcs	Murata	GRM31CR61E106KA12B
L1	1.0 µH	Vishay, Toko	IHLP-5050, FDA1254-1R0M
Q1	30V, 13 mΩ	International Rectifier	IRF7821
Q2	30 V, 5.8 mΩ	International Rectifier	IRF8113
R4	8.06 kΩ	—	Std

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June, 2009) to Revision B **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS51117PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS51117PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS51117PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS51117PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS51117RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS51117RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS51117RGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS51117RGYTG4	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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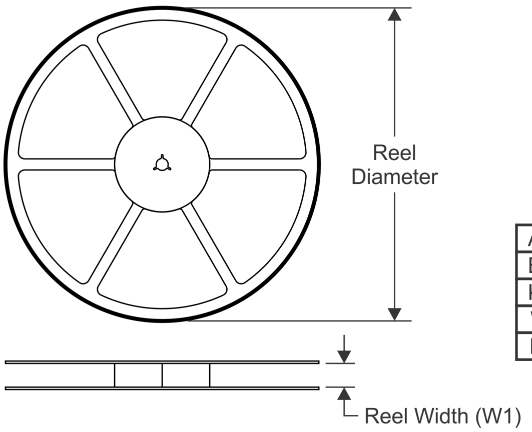
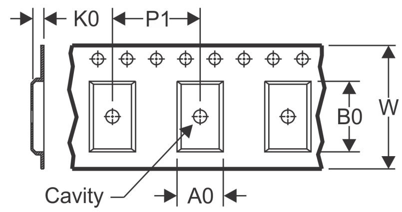
TAPE AND REEL INFORMATION

REEL DIMENSIONS

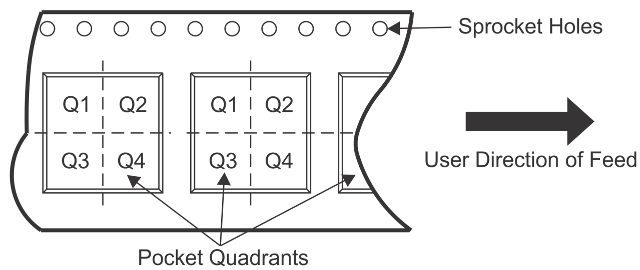


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

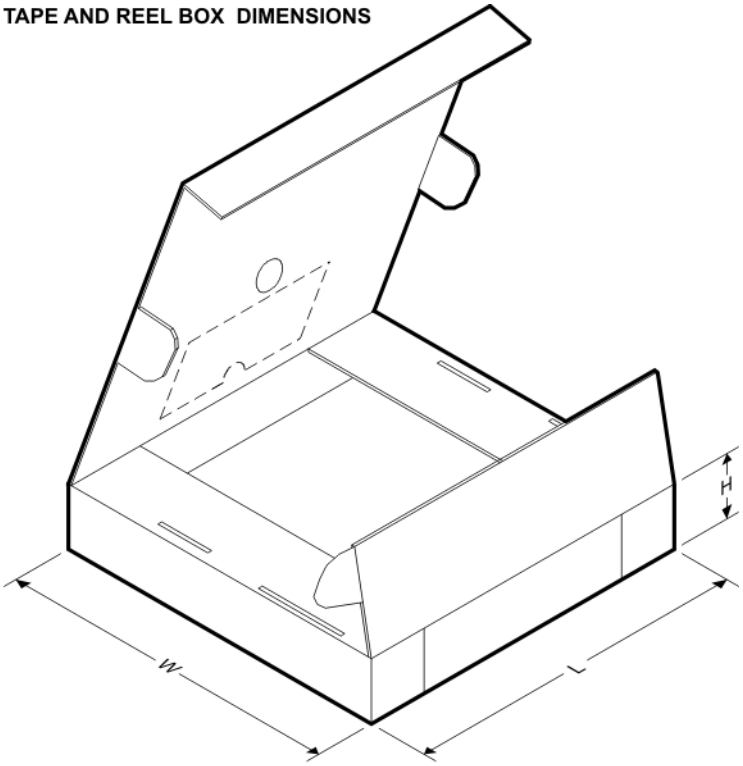
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51117PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS51117RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS51117RGYT	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TPS51117RGYT	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

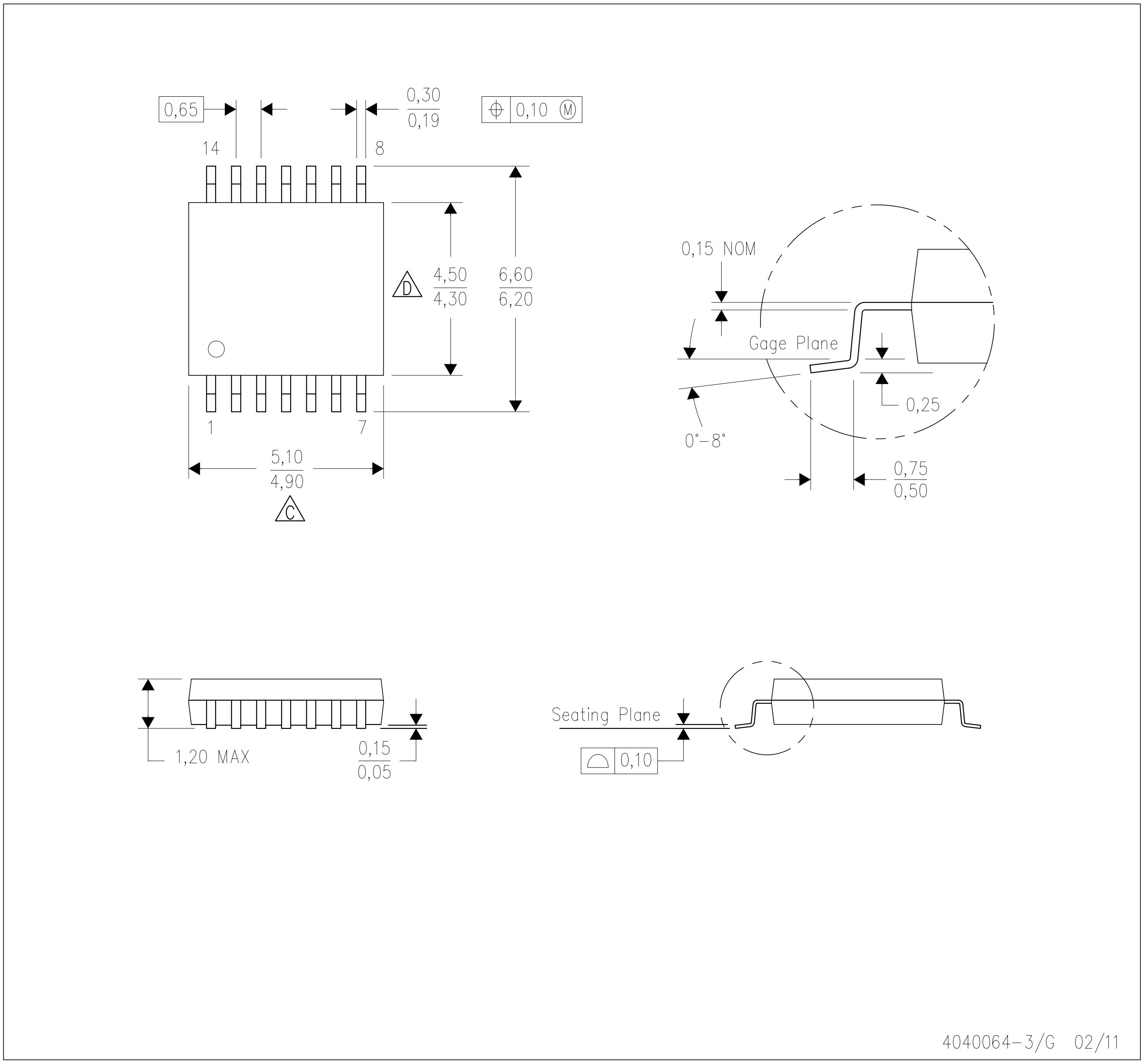
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

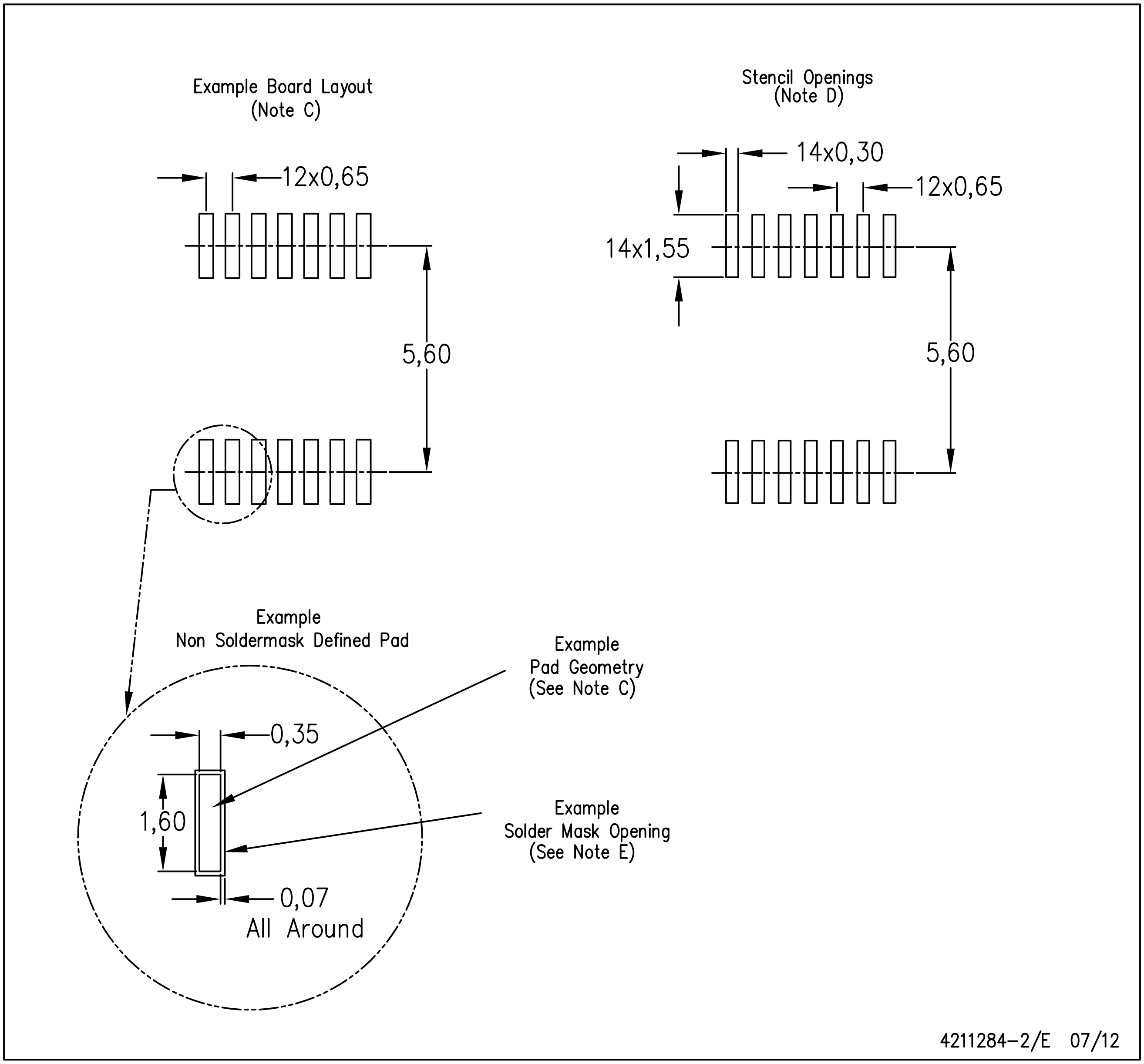
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51117PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TPS51117RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
TPS51117RGYT	VQFN	RGY	14	250	210.0	185.0	35.0
TPS51117RGYT	VQFN	RGY	14	250	210.0	185.0	35.0

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



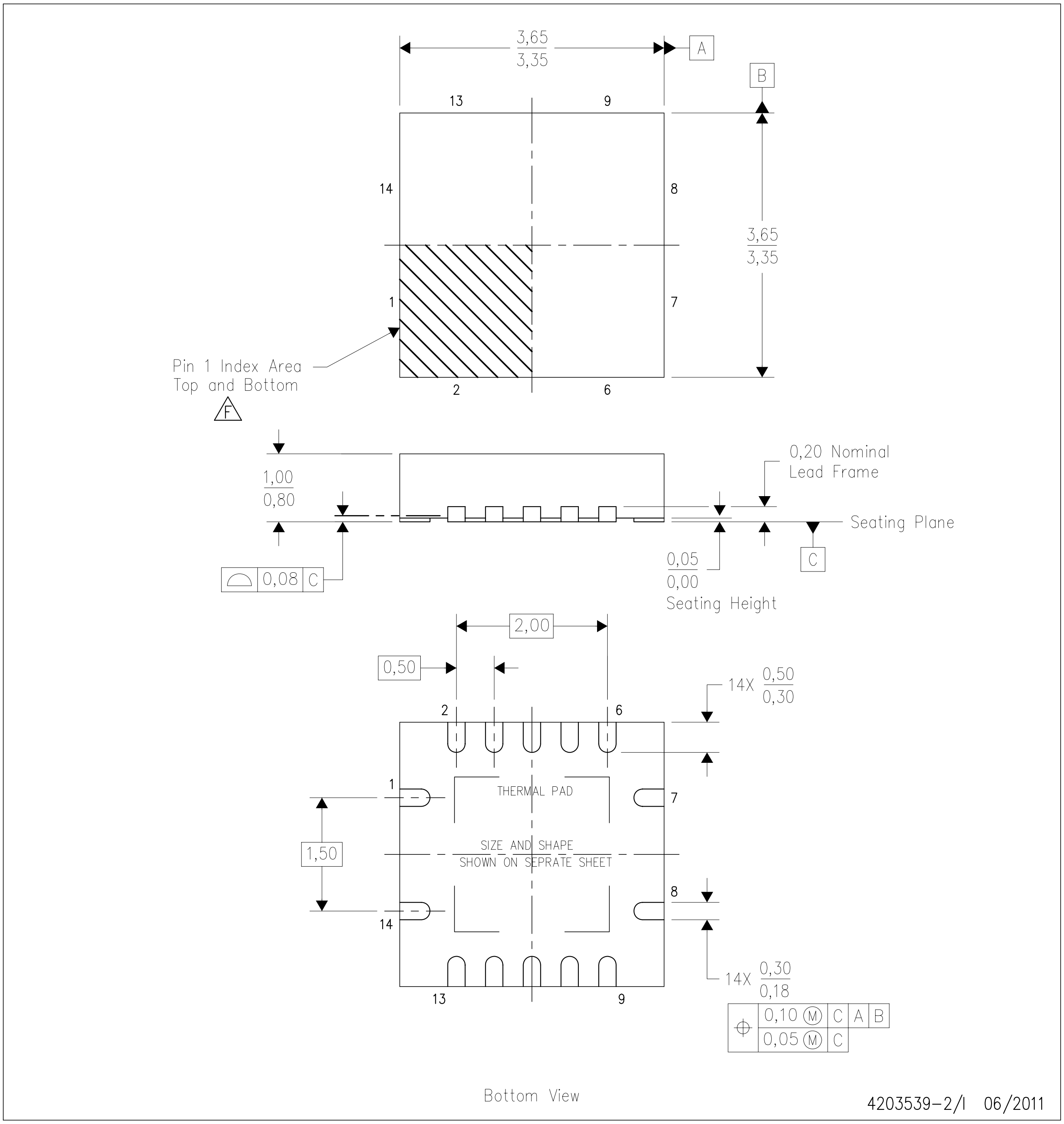
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

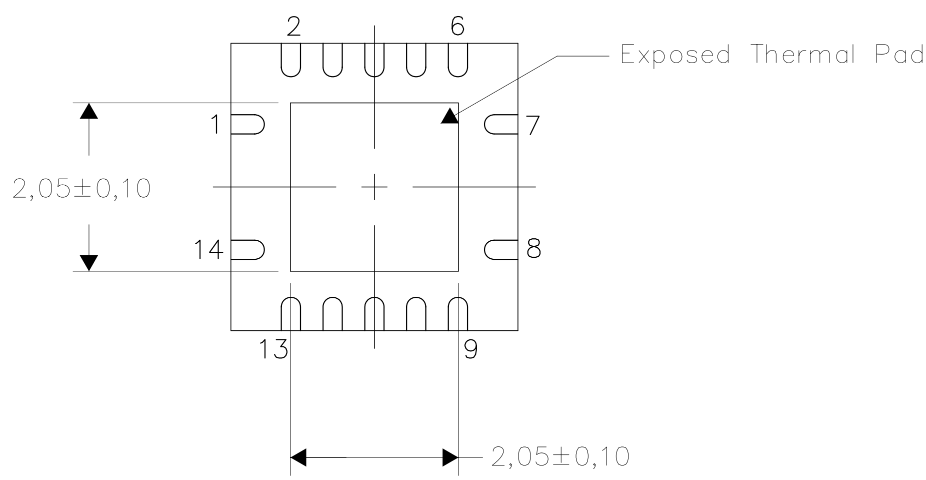
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



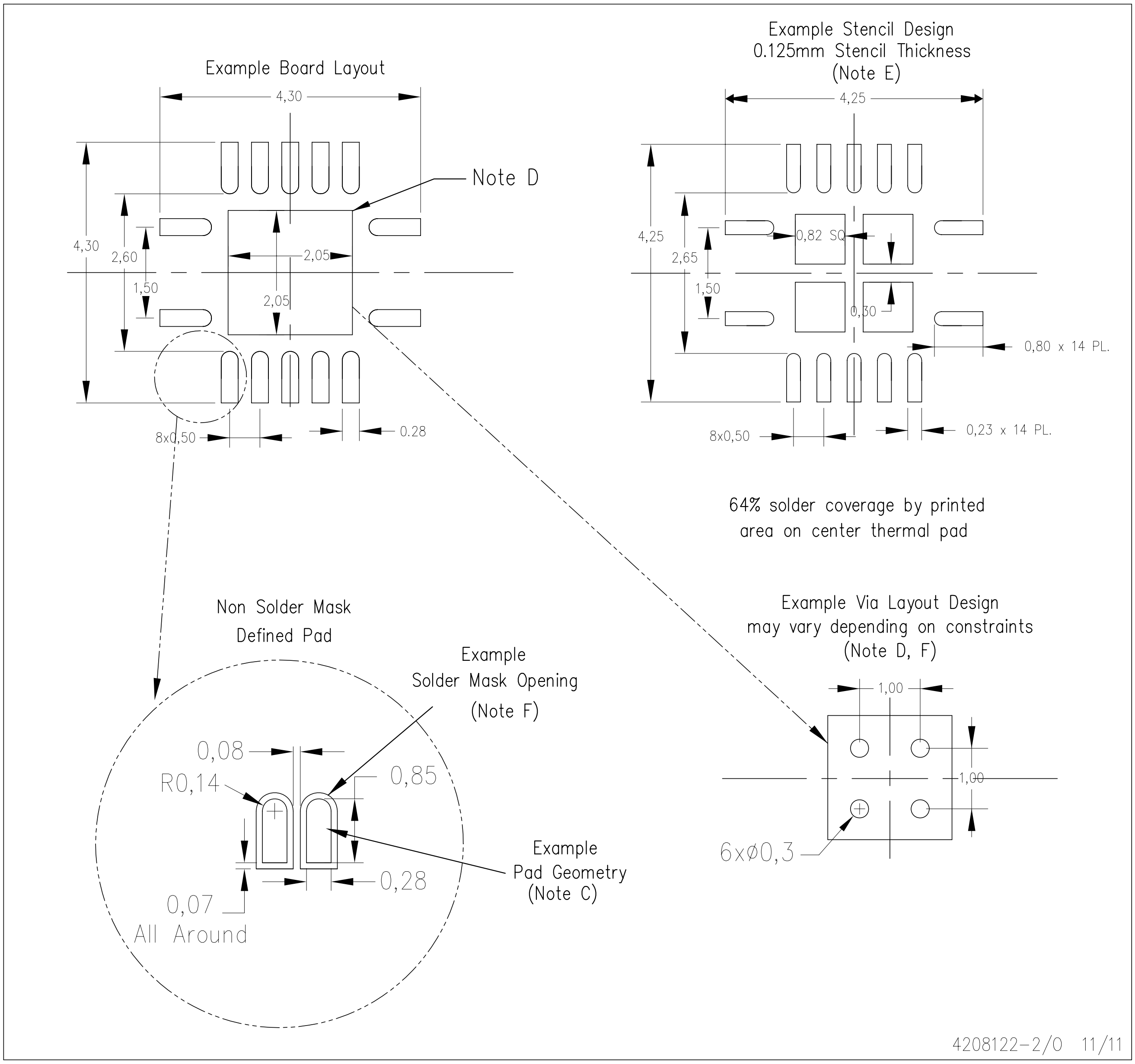
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/O 11/11

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.