TPS51125 Dual-Synchronous, Step-Down Controller With Out-of-Audio™ Operation and 100-mA LDOS for Notebook System Power

1 Features

- Wide Input Voltage Range: 5.5 V to 28 V
- Output Voltage Range: 2 V to 5.5 V
- Built-In 100-mA, 5-V and 3.3-V LDO With Switches
- Built-In 1% 2-V Reference Output
- With or Without Out-of-Audio™ Mode Selectable Light-Load and PWM-Only Operation
- Internal 1.6-ms Voltage Servo Soft-Start
- Adaptive On-Time Control Architecture With Four Selectable Frequency Setting
- 4500 ppm/°C $R_{DS(on)}$ Current Sensing
- Built-In Output Discharge
- Powergood Output
- Built-In OVP/UVP/OCP
- Thermal Shutdown (Nonlatch)
- QFN, 24-Pin (RGE)

2 Applications

- Notebook Computers
- I/O Supplies
- System Power Supplies

3 Description

The TPS51125 is a cost-effective, dual-synchronous buck controller targeted for notebook system power supply solutions. The device provides 5-V and 3.3-V LDOs and requires few external components. The 270-kHz VCLK output can be used to drive an external charge pump, thus generating gate drive voltage for the load switches without reducing the efficiency of the main converter. The TPS51125 supports high-efficiency, fast-transient response and provides a combined power-good signal. Out-of-Audio mode light-load operation enables low acoustic noise at much higher efficiency than conventional forced PWM operation. Adaptive on-time D-CAP™ control provides convenient and efficient operation. The part operates with supply input voltages ranging from 5.5 V to 28 V and supports output voltages from 2 V to 5.5 V. The TPS51125 is available in a 24-pin QFN package and is specified from -40°C to 85°C ambient temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51125	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

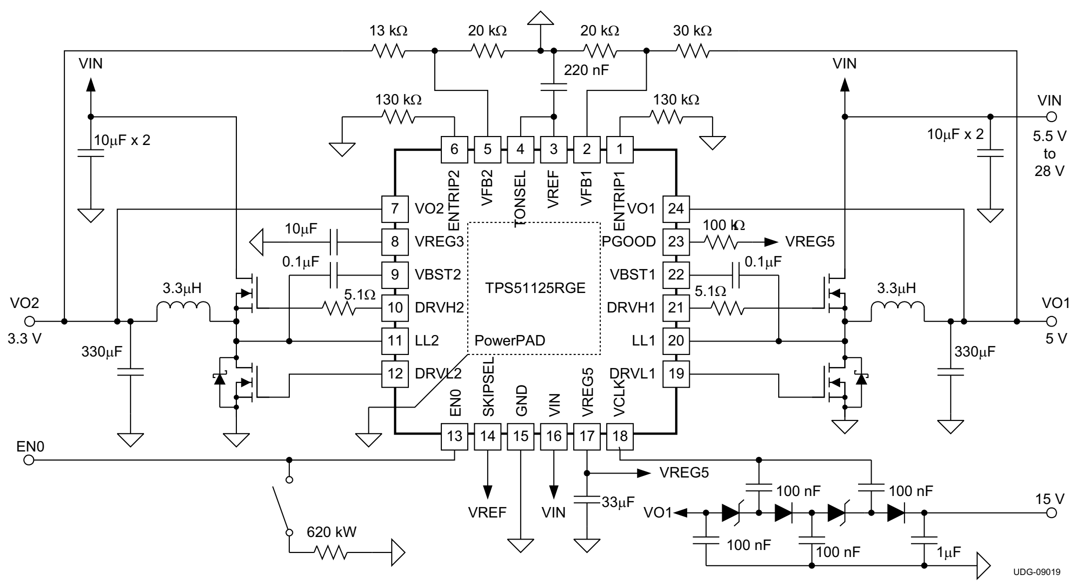


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (June 2012) to Revision H **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

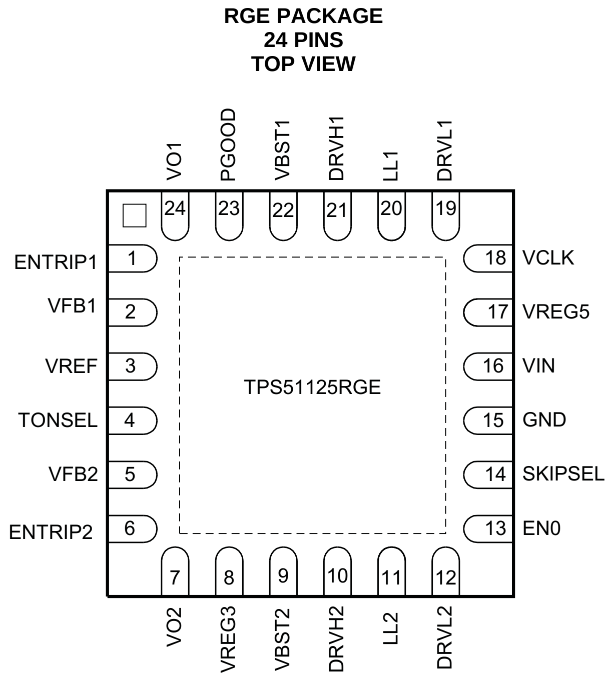
Changes from Revision F (March 2012) to Revision G **Page**

- Added electrostatic discharge ratings in *Absolute Maximum Ratings* table. 5

Changes from Revision E (May 2011) to Revision F **Page**

- Added Input voltage range parameter, LL1, LL2, pulse width < 20 ns with a value of -5 V to 30 V. 5

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DRVH1	21	O	High-side N-channel MOSFET driver outputs. LL referenced drivers.
DRVH2	10		
DRVL1	19	O	Low-side N-channel MOSFET driver outputs. GND referenced drivers.
DRVL2	12		
ENTRIP1	1	I/O	Channel 1 and Channel 2 enable and OCL trip setting pins.Connect resistor from this pin to GND to set threshold for synchronous $R_{DS(on)}$ sense. Short to ground to shutdown a switcher channel.
ENTRIP2	6		
EN0	13	I/O	Master enable input. Open : LDOs on, and ready to turn on VCLK and switcher channels. 620 kΩ to GND : enable both LDOs, VCLK off and ready to turn on switcher channels. Power consumption is almost the same as the case of VCLK = ON. GND : disable all circuit
GND	15	—	Ground.
LL1	20	I	Switch node connections for high-side drivers, current limit and control circuitry.
LL2	11		
PGOOD	23	O	Power Good window comparator output for channel 1 and 2. (Logical AND)
SKIPSEL	14	I	Selection pin for operation mode: OOA auto skip : Connect to VREG3 or VREG5 Auto skip : Connect to VREF Auto skip : Connect to VREF
TONSEL	4	I	On-time adjustment pin 365 kHz/460 kHz setting : connect to VREG5 300 kHz/375 kHz setting : connect to VREG3 245 kHz/305 kHz setting : connect to VREF 200 kHz/250 kHz setting : connect to GND

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VBST1	22	I	Supply input for high-side N-channel MOSFET driver (boost terminal).
VBST2	9		
VCLK	18	O	270-kHz clock output for 15-V charge pump.
VFB1	2	I	SMPS feedback inputs. Connect with feedback resistor divider.
VFB2	5		
VIN	16	I	High voltage power supply input for 5-V/3.3-V LDO.
VO1	24	I/O	Output connection to SMPS. These terminals work as fixed voltage inputs and output discharge inputs. VO1 and VO2 also work as 5 V and 3.3 V switch over return power input respectively.
VO2	7		
VREF	3	O	2-V reference voltage output. Connect 220-nF to 1-μF ceramic capacitor to Signal GND near the device.
VREG3	8	O	3.3-V power supply output. Connect 10-μF ceramic capacitor to Power GND near the device. A 1-μF ceramic capacitor is acceptable when not loaded.
VREG5	17	O	5-V power supply output. Connect 33-μF ceramic capacitor to Power GND near the device.

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage[1]	VBST1, VBST2	–0.3	36	V
	VIN	–0.3	30	
	LL1, LL2	–2.0	30	
	LL1, LL2, pulse width < 20 ns	–5.0	30	
	VBST1, VBST2 [2]	–0.3	6	
	EN0, ENTRIP1, ENTRIP2, VFB1, VFB2, VO1, VO2, TONSEL, SKIPSEL	–0.3	6	
Output voltage[1]	DRVH1, DRVH2	–1.0	36	
	DRVH1, DRVH2 [2]	–0.3	6	
	PGOOD, VCLK, VREG3, VREG5, VREF, DRVL1, DRVL2	–0.3	6	
Junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the corresponding LLx terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VIN	5.5	28	V
Input voltage	VBST1, VBST2	–0.1	34	
	VBST1, VBST2 (with respect to LLx)	–0.1	5.5	
	EN0, ENTRIP1, ENTRIP2, VFB1, VFB2, VO1, VO2, TONSEL, SKIPSEL	–0.1	5.5	
Output voltage	DRVH1, DRVH2	–0.8	34	
	DRVH1, DRVH2 (with respect to LLx)	–0.1	5.5	
	LL1, LL2	–1.8	28	
	VREF, VREG3, VREG5	–0.1	5.5	
	PGOOD, VCLK, DRVL1, DRVL2	–0.1	5.5	
Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS51125 VQFN 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	12.4	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	12.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN1}	VIN supply current1	VIN current, T_A = 25°C, no load, VO1 = 0 V, VO2 = 0 V, EN0=open, ENTRIPx = 5 V, VFB1 = VFB2 = 2.05 V		0.55	1	mA
I_{VIN2}	VIN supply current2	VIN current, T_A = 25°C, no load, VO1 = 5 V, VO2 = 3.3 V, EN0=open, ENTRIPx = 5 V, VFB1 = VFB2 = 2.05 V		4	6.5	µA
I_{VO1}	VO1 current	VO1 current, T_A = 25°C, no load, VO1 = 5 V, VO2 = 3.3 V, EN0=open, ENTRIPx = 5 V, VFB1 = VFB2 = 2.05 V		0.8	1.5	mA
I_{VO2}	VO2 current	VO2 current, T_A = 25°C, no load, VO1 = 5 V, VO2 = 3.3 V, EN0=open, ENTRIPx = 5 V, VFB1 = VFB2 = 2.05 V		12	100	µA
$I_{VINSTBY}$	VIN standby current	VIN current, T_A = 25°C, no load, EN0 = 1.2 V, ENTRIPx = 0 V		95	250	µA
I_{VINSDN}	VIN shutdown current	VIN current, T_A = 25°C, no load, EN0 = ENTRIPx = 0 V		10	25	µA
VREF OUTPUT						
V_{VREF}	VREF output voltage	I_{VREF} = 0 A	1.98	2.00	2.02	V
		-5 µA < I_{VREF} < 100 µA	1.97	2.00	2.03	V
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	VO1 = 0 V, I_{VREG5} < 100 mA, T_A = 25°C	4.8	5	5.2	V
		VO1 = 0 V, I_{VREG5} < 100 mA, 6.5 V < VIN < 28 V	4.75	5	5.25	V
		VO1 = 0 V, I_{VREG5} < 50 mA, 5.5 V < VIN < 28 V	4. 75	5	5.25	V
I_{VREG5}	VREG5 output current	VO1 = 0 V, VREG5 = 4.5 V	100	175	250	mA
V_{TH5VSW}	Switch over threshold	Turns on	4.55	4.7	4.85	V
		Hysteresis	0.15	0.25	0.3	V
R_{5VSW}	5 V SW R_{ON}	VO1 = 5 V, I_{VREG5} = 100 mA		1	3	Ω
VREG3 OUTPUT						
V_{VREG3}	VREG3 output voltage	VO2 = 0 V, I_{VREG3} < 100 mA, T_A= 25°C	3.2	3.33	3.46	V
		VO2 = 0 V, I_{VREG3} < 100 mA, 6.5 V < VIN < 28 V	3.13	3.33	3.5	V
		VO2 = 0 V, I_{VREG3} < 50 mA, 5.5 V < VIN < 28 V	3.13	3.33	3.5	V
I_{VREG3}	VREG3 output current	VO2 = 0 V, VREG3 = 3 V	100	175	250	mA
V_{TH3VSW}	Switch over threshold	Turns on	3.05	3.15	3.25	V
		Hysteresis	0.1	0.2	0.25	V
R_{3VSW}	3 V SW R_{ON}	VO2 = 3.3 V, I_{VREG3} = 100 mA		1.5	4	Ω
INTERNAL REFERENCE VOLTAGE						
V_{IREF}	Internal reference voltage	I_{VREF} = 0 A, beginning of ON state	1.95	1.98	2.01	V
V_{VFB}	VFB regulation voltage	FB voltage, I_{VREF} = 0 A, skip mode	1.98	2.01	2.04	V
		FB voltage, I_{VREF} = 0 A, OOA mode (1)	2.00	2.035	2.07	V
		FB voltage, I_{VREF} = 0 A, continuous conduction (1)		2.00		V
I_{VFB}	VFB input current	VFBx = 2.0 V, T_A= 25°C	–20		20	nA

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT} DISCHARGE						
I_{Dischg}	VOUT discharge current	ENTRIPx = 0 V, VOx = 0.5 V	10	60		mA
OUTPUT DRIVERS						
R_{DRVH}	DRVH resistance	Source, $V_{BSTx\ -\ DRVHx}$ = 100 mV		4	8	Ω
		Sink, $V_{DRVHx\ -\ LLx}$ = 100 mV		1.5	4	
R_{DRVL}	DRVL resistance	Source, $V_{VREG5\ -\ DRVLx}$ = 100 mV		4	8	
		Sink, V_{DRVLx} = 100 mV		1.5	4	
t_D	Dead time	DRVHx-off to DRVLx-on		10		ns
		DRVLx-off to DRVHx-on		30		
CLOCK OUTPUT						
V_{CLKH}	High level voltage	I_{VCLK} = -10 mA, VO1 = 5 V, T_A = 25 °C	4.84	4.92		V
V_{CLKL}	Low level voltage	I_{VCLK} = 10 mA, VO1 = 5 V, T_A = 25 °C		0.06	0.12	
f_{CLK}	Clock frequency	T_A = 25 °C	175	270	325	kHz
INTERNAL BST DIODE						
V_{FBST}	Forward voltage	$V_{VREG5\text{-}VBSTx}$, I_F = 10 mA, T_A = 25 °C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakage current	VBSTx = 34 V, LLx = 28 V, T_A = 25 °C		0.1	1	μA
DUTY AND FREQUENCY CONTROL						
t_{ON11}	CH1 on time 1	V_{IN} = 12 V, VO1 = 5 V, 200 kHz setting		2080		ns
t_{ON12}	CH1 on time 2	V_{IN} = 12 V, VO1 = 5 V, 245 kHz setting		1700		
t_{ON13}	CH1 on time 3	V_{IN} = 12 V, VO1 = 5 V, 300 kHz setting		1390		
t_{ON14}	CH1 on time 4	V_{IN} = 12 V, VO1 = 5 V, 365 kHz setting		1140		
t_{ON21}	CH2 on time 1	V_{IN} = 12 V, VO2 = 3.3 V, 250 kHz setting		1100		
t_{ON22}	CH2 on time 2	V_{IN} = 12 V, VO2 = 3.3 V, 305 kHz setting		900		
t_{ON23}	CH2 on time 3	V_{IN} = 12 V, VO2 = 3.3 V, 375 kHz setting		730		
t_{ON24}	CH2 on time 4	V_{IN} = 12 V, VO2 = 3.3 V, 460 kHz setting		600		
$t_{ON(min)}$	Minimum on time	T_A = 25 °C		80		
$t_{OFF(min)}$	Minimum off time	T_A = 25 °C		300		
SOFT-START						
t_{SS}	Internal SS time	Internal soft start	1.1	1.6	2.1	ms
POWERGOOD						
V_{THPG}	PG threshold	PG in from lower	92.50%	95%	97.50%	
		PG in from higher	102.50%	105%	107.50%	
		PG hysteresis	2.50%	5%	7.50%	
I_{PGMAX}	PG sink current	PGOOD = 0.5 V	5	12		mA
t_{PGDEL}	PG delay	Delay for PG in	350	510	670	μs

Electrical Characteristics (continued)

over operating free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD AND SETTING CONDITIONS						
V_{EN0}	EN0 setting voltage	Shutdown			0.4	V
		Enable, VCLK = off	0.8		1.6	
		Enable, VCLK = on	2.4			
I_{EN0}	EN0 current	V_{EN0} = 0.2 V	2	3.5	5	μA
		V_{EN0} = 1.5 V	1	1.75	2.5	
V_{EN}	ENTRIP1, ENTRIP2 threshold	Shutdown	350	400	450	mV
		Hysteresis	10	30	60	
V_{TONSEL}	TONSEL setting voltage	200 kHz/250 kHz			1.5	V
		245 kHz/305 kHz	1.9		2.1	
		300 kHz/375 kHz	2.7		3.6	
		365 kHz/460 kHz	4.7			
$V_{SKIPSEL}$	SKIPSEL setting voltage	PWM only			1.5	
		Auto skip	1.9		2.1	
		OOA auto skip	2.7			
PROTECTION: CURRENT SENSE						
I_{ENTRIP}	ENTRIPx source current	$V_{ENTRIPx}$ = 920 mV, T_A= 25°C	9.4	10	10.6	μA
$TC_{IENTRIP}$	ENTRIPx current temperature coefficient	On the basis of 25°C[(1)]		4500		ppm/°C
V_{OCLoff}	OCP comparator offset	(($V_{ENTRIPx-GND}$/9)-24 mV -$V_{GND-LLx}$) voltage, $V_{ENTRIPx-GND}$ = 920 mV	–8	0	8	mV
$V_{OCL(max)}$	Maximum OCL setting	$V_{ENTRIPx}$ = 5 V	185	205	225	
V_{ZC}	Zero cross detection comparator offset	$V_{GND-LLx}$ voltage	–5	0	5	
V_{ENTRIP}	Current limit threshold	$V_{ENTRIPx-GND}$ voltage, [(1)]	0.515		2	V
PROTECTION: UNDERVOLTAGE AND OVERVOLTAGE						
V_{OVP}	OVP trip threshold	OVP detect	110%	115%	120%	
t_{OVPDEL}	OVP prop delay			2		μs
V_{UVP}	Output UVP trip threshold	UVP detect	55%	60%	65%	
		Hysteresis		10%		
t_{UVPDEL}	Output UVP prop delay		20	32	40	μs
t_{UVPEN}	Output UVP enable delay		1.4	2	2.6	ms
UVLO						
$V_{UVVREG5}$	VREG5 UVLO threshold	Wake up	4.1	4.2	4.3	V
		Hysteresis	0.38	0.43	0.48	
$V_{UVVREG3}$	VREG3 UVLO threshold	Shutdown [(1)]		VO2-1		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature [(1)]		150		°C
		Hysteresis [(1)]		10		

6.6 Typical Characteristics

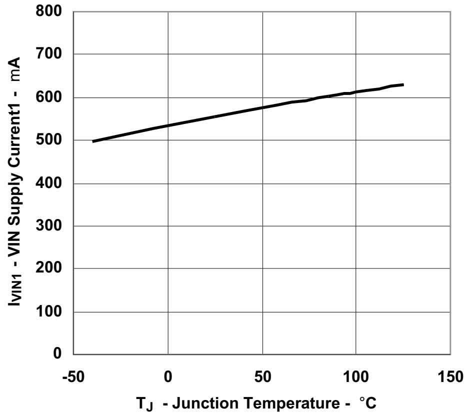


Figure 1. VIN Supply Current1 vs Junction Temperature

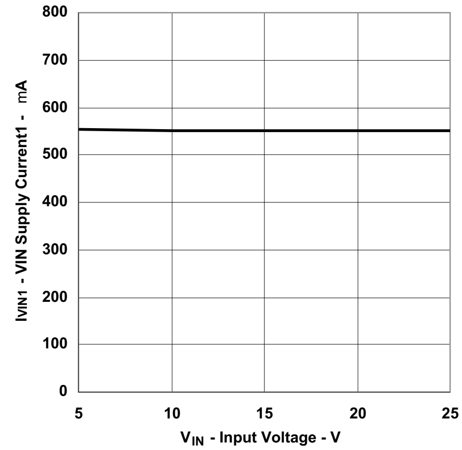


Figure 2. VIN Supply Current1 vs Input Voltage

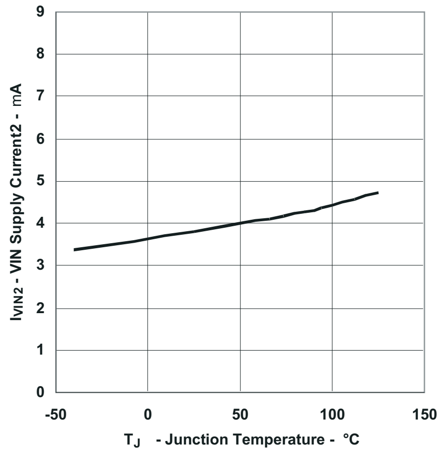


Figure 3. VIN Supply Current2 vs Junction Temperature

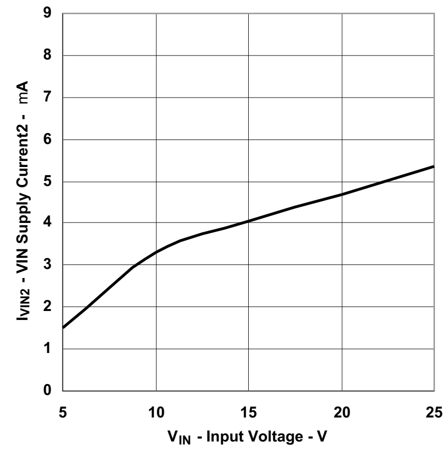


Figure 4. VIN Supply Current1 vs Input Voltage

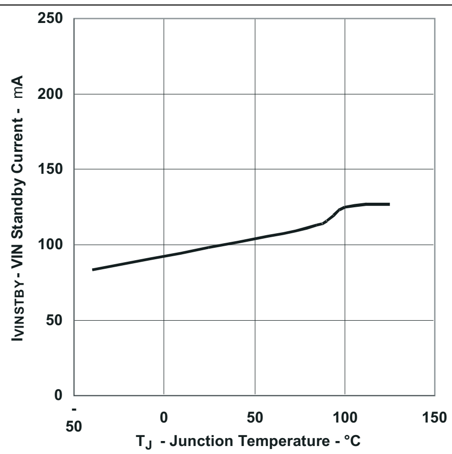


Figure 5. VIN Standby Current vs Junction Temperature

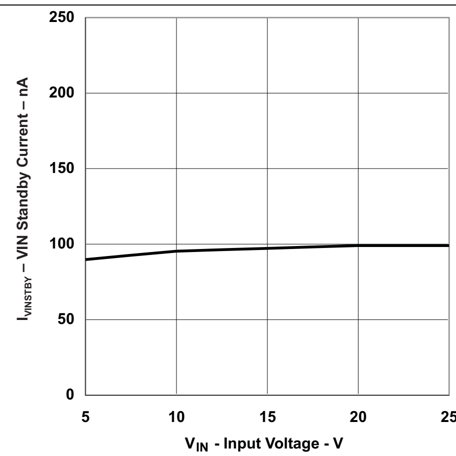


Figure 6. VIN Standby Current vs Input Voltage

Typical Characteristics (continued)

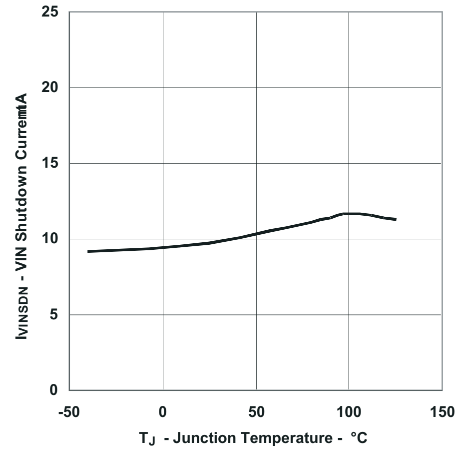


Figure 7. VIN Shutdown Current vs Junction Temperature

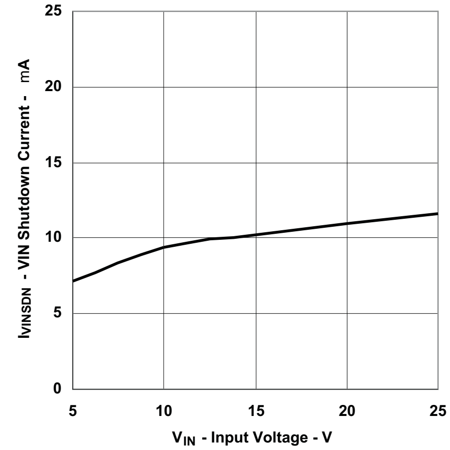


Figure 8. VIN Shutdown Current vs Input Voltage

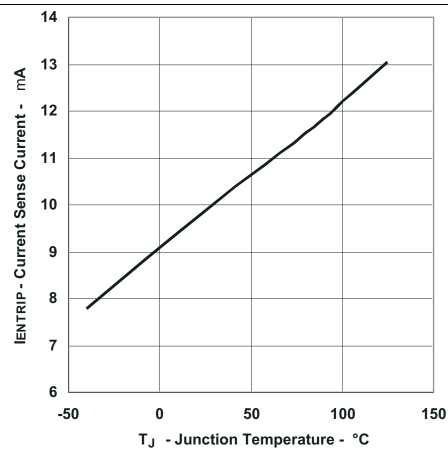


Figure 9. Current Sense Current vs Junction Temperature

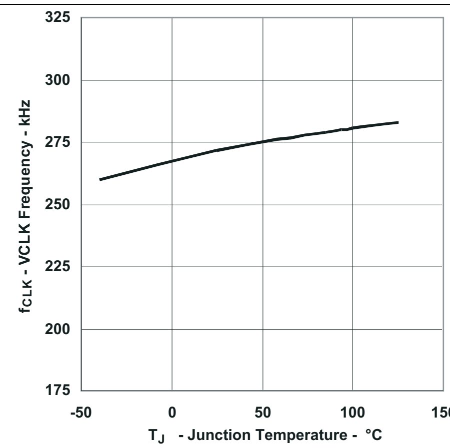


Figure 10. VCLK Frequency vs Junction Temperature

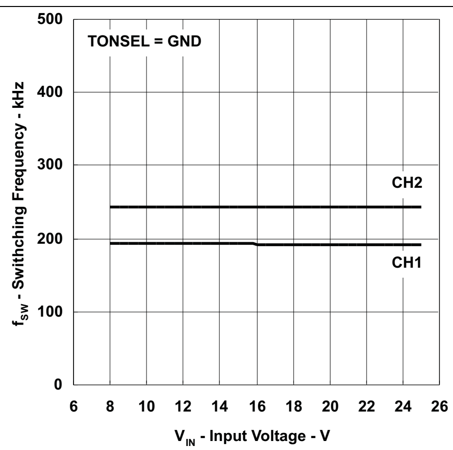


Figure 11. Switching Frequency vs Input Voltage

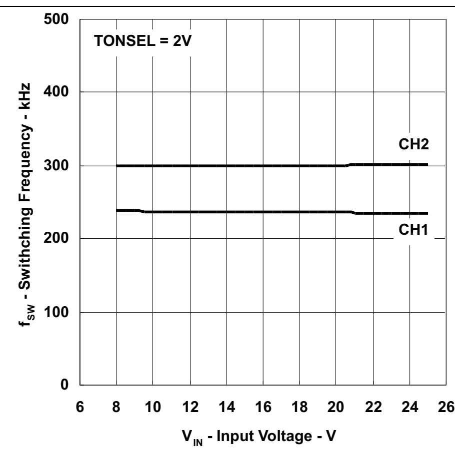


Figure 12. Switching Frequency vs Input Voltage

Typical Characteristics (continued)

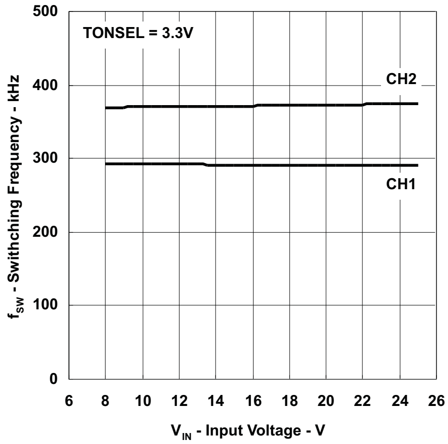


Figure 13. Switching Frequency vs Input Voltage

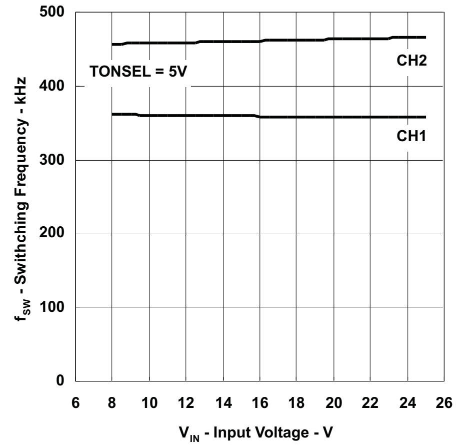


Figure 14. Switching Frequency vs Input Voltage

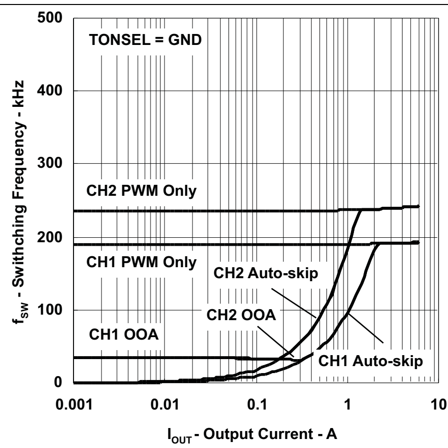


Figure 15. Switching Frequency vs Output Current

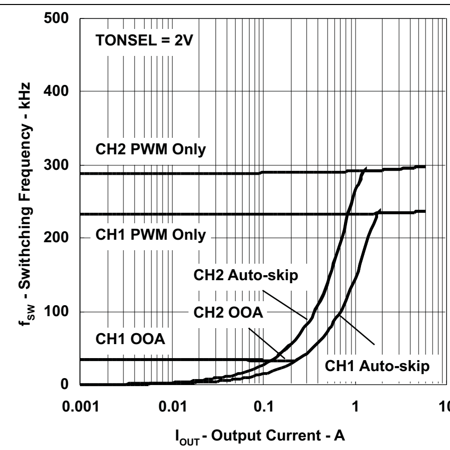


Figure 16. Switching Frequency vs Output Current

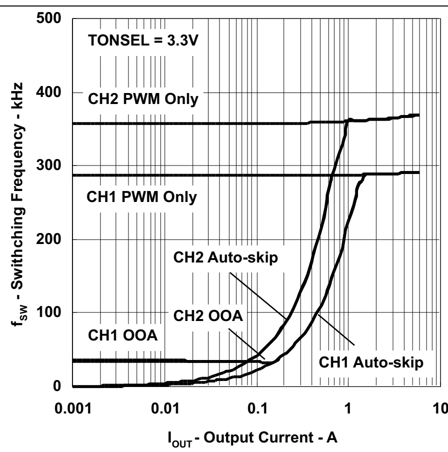


Figure 17. Switching Frequency vs Output Current

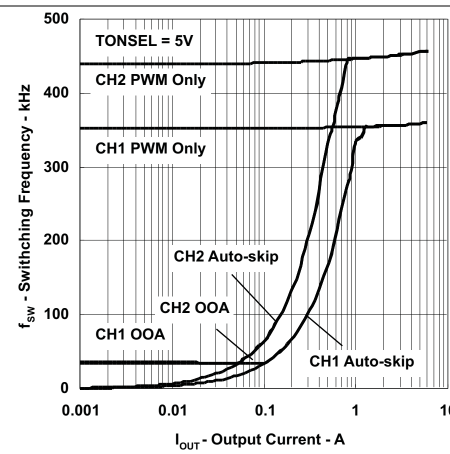


Figure 18. Switching Frequency vs Output Current

Typical Characteristics (continued)

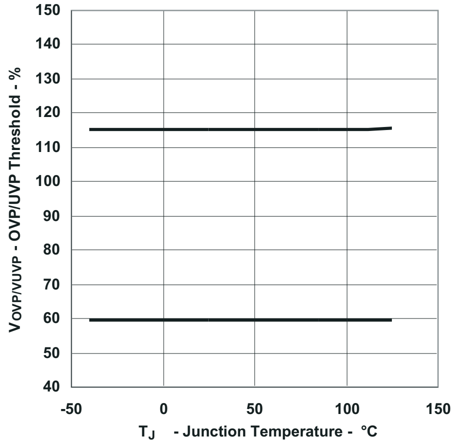


Figure 19. OVP/UVP Threshold Voltage vs Junction Temperature

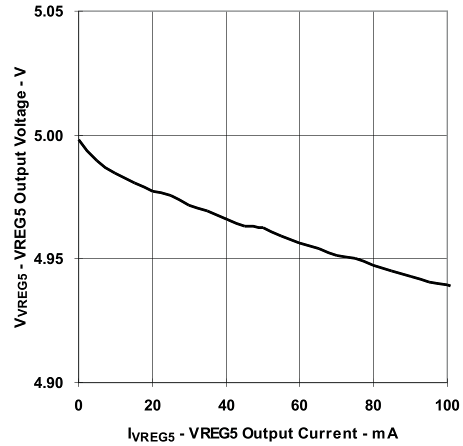


Figure 20. VREG5 Output Voltage vs Output Current

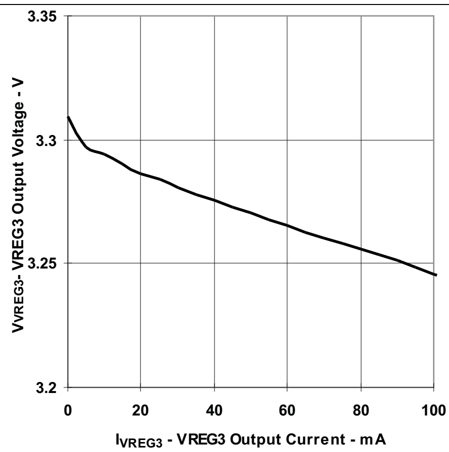


Figure 21. VREG5 Output Voltage vs Output Current

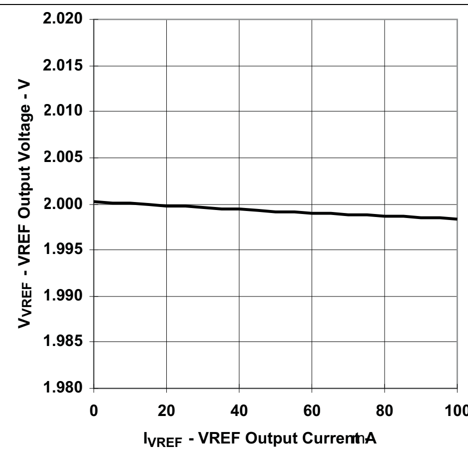


Figure 22. VREG5 Output Voltage vs Output Current

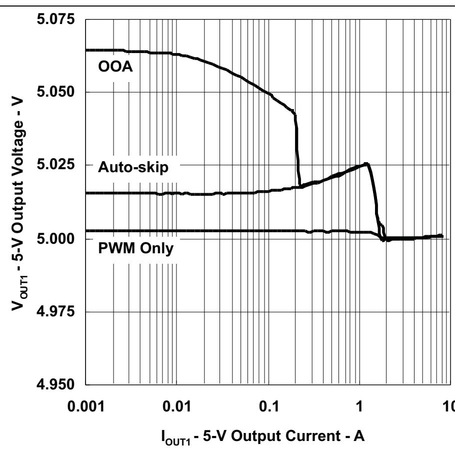


Figure 23. 5-V Output Voltage vs Output Current

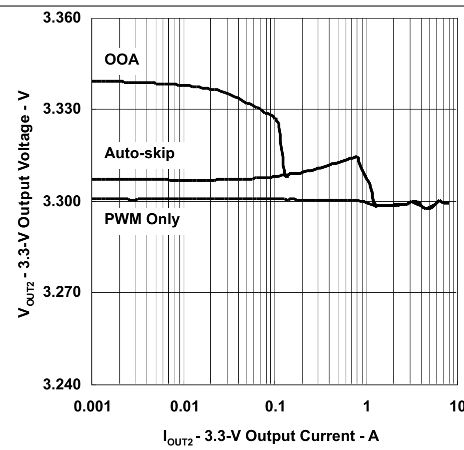


Figure 24. 3.3-V Output Voltage vs Output Current

Typical Characteristics (continued)

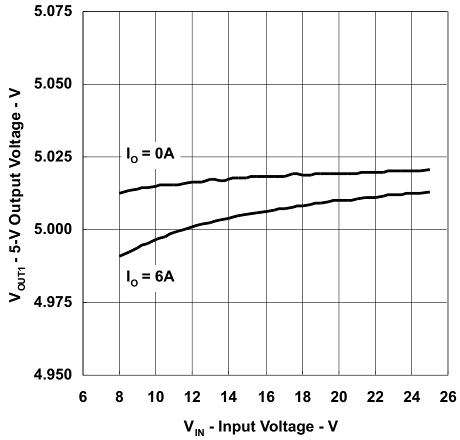


Figure 25. 5-V Output Voltage vs Input Voltage

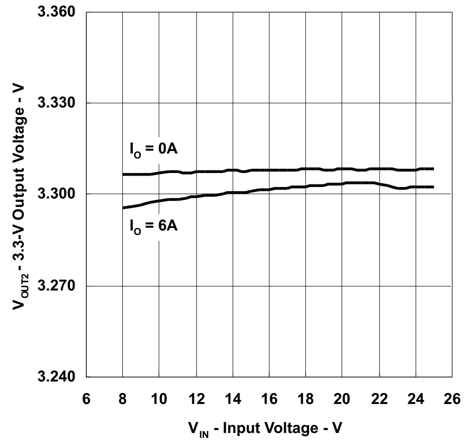


Figure 26. 3.3-V Output Voltage vs Input Voltage

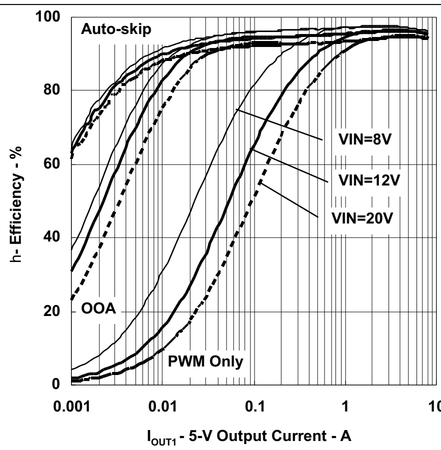


Figure 27. 5-V Efficiency vs Output Current

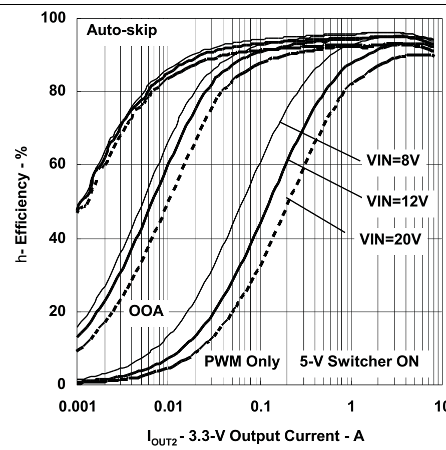


Figure 28. 3.3-V Efficiency vs Output Current

7 Detailed Description

7.1 Overview

The TPS51125 is a cost-effective, dual-synchronous buck controller targeted for notebook system-power supply solutions. It provides 5 V and 3.3 V LDOs and requires few external components. With D-CAP™ control mode implemented, compensation network can be removed. Besides, the fast transient response also reduced the output capacitance.

7.2 Functional Block Diagram

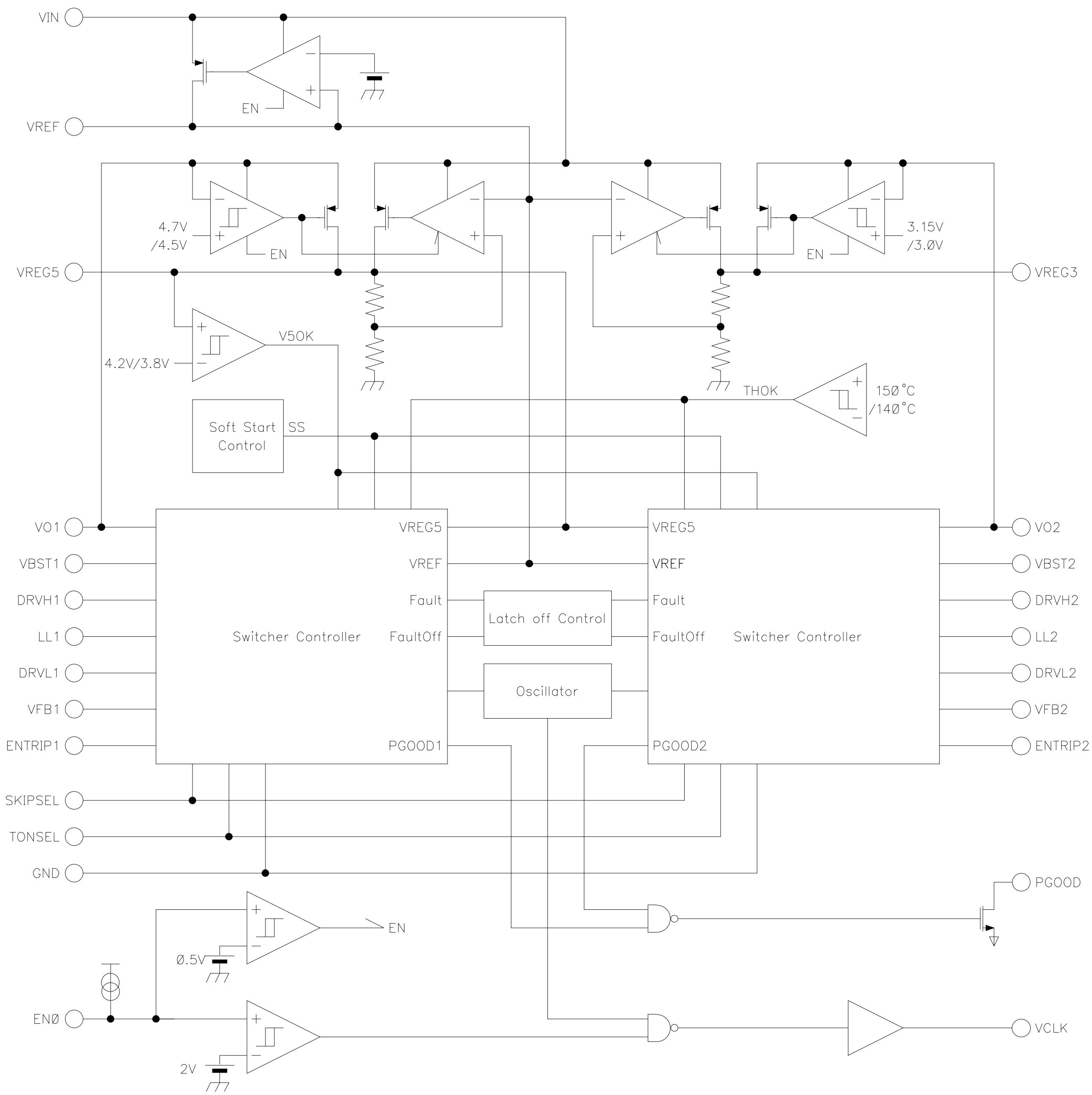


Figure 29. TPS51125 Functional Block Diagram

Functional Block Diagram (continued)

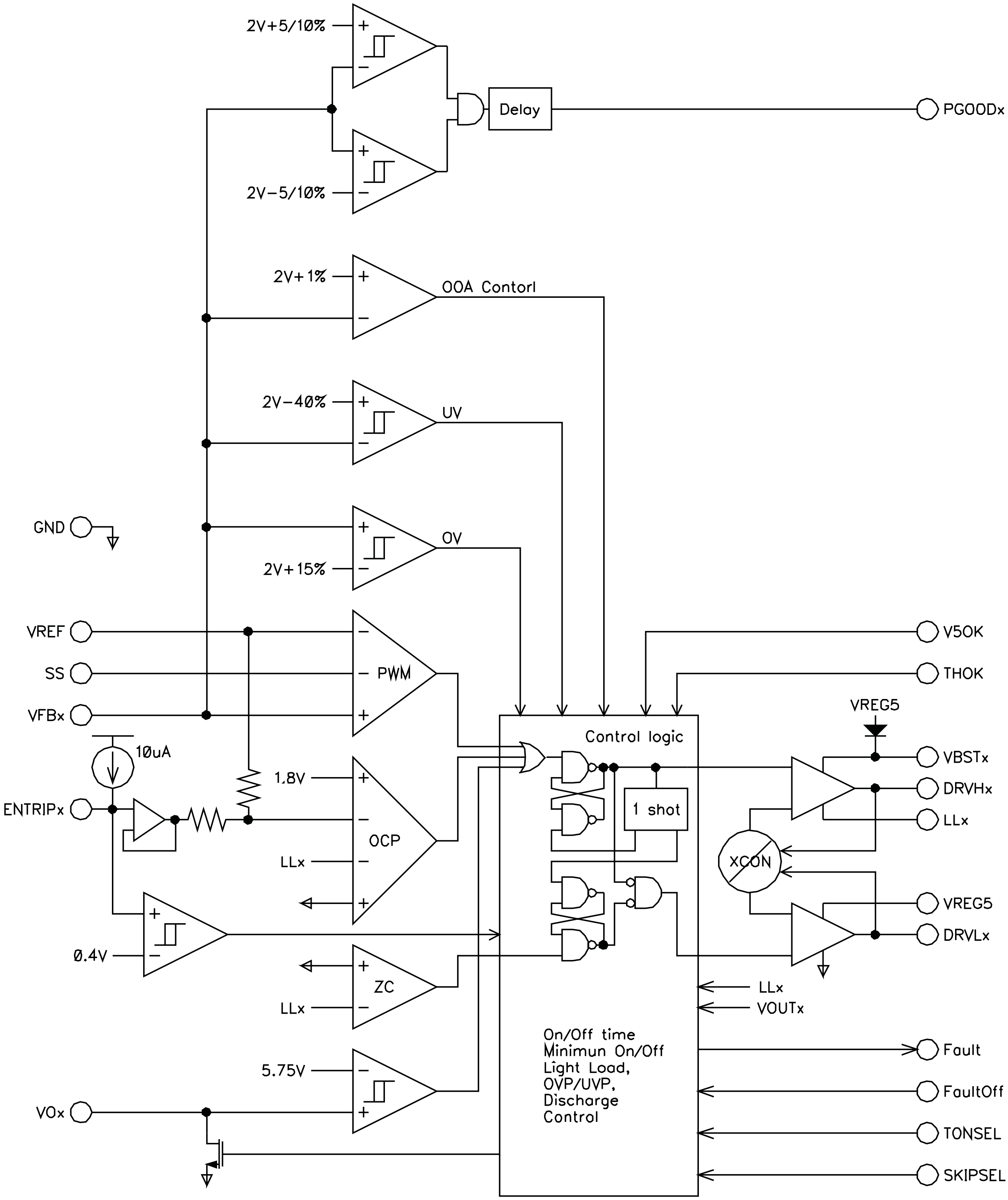


Figure 30. Switcher Controller Block

7.3 Feature Description

7.3.1 PWM Operations

The main control loop of the switch mode power supply (SMPS) is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports a proprietary D-CAP mode. D-CAP mode does not require external compensation circuit and is suitable for low external component count configuration when used with appropriate amount of ESR at the output capacitor(s).

At the beginning of each cycle, the synchronous top MOSFET is turned on, or becomes ON state. This MOSFET is turned off, or becomes OFF state, after internal one-shot timer expires. This one shot is determined by V_{IN} and V_{OUT} to keep frequency fairly constant over input voltage range, hence it is called adaptive on-time control. The MOSFET is turned on again when the feedback point voltage, VFB, decreased to match with internal 2-V reference. The inductor current information is also monitored and should be below the overcurrent threshold to initiate this new cycle. Repeating operation in this manner, the controller regulates the output voltage. The synchronous bottom or the “rectifying” MOSFET is turned on at the beginning of each OFF state to keep the conduction loss minimum.The rectifying MOSFET is turned off before the top MOSFET turns on at next switching cycle or when inductor current information detects zero level. In the auto-skip mode or the OOA skip mode, this enables seamless transition to the reduced frequency operation at light load condition so that high efficiency is kept over broad range of load current.

7.3.2 Adaptive On-Time Control and PWM Frequency

TPS51125 does not have a dedicated oscillator onboard. However, the part runs with pseudo-constant frequency by feed-forwarding the input and output voltage into the on-time, one-shot timer. The on-time is controlled inverse proportional to the input voltage and proportional to the output voltage so that the duty ratio will be kept as VOUT/VIN technically with the same cycle time. The frequencies are set by TONSEL terminal connection as Table 1.

Table 1. Tonsel Connection and Switching Frequency

TONSEL CONNECTION	SWITCHING FREQUENCY	
	CH1	CH2
GND	200 kHz	250 kHz
VREF	245 kHz	305 kHz
VREG3	300 kHz	375 kHz
VREG5	365 kHz	460 kHz

7.3.3 Loop Compensation

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 31.

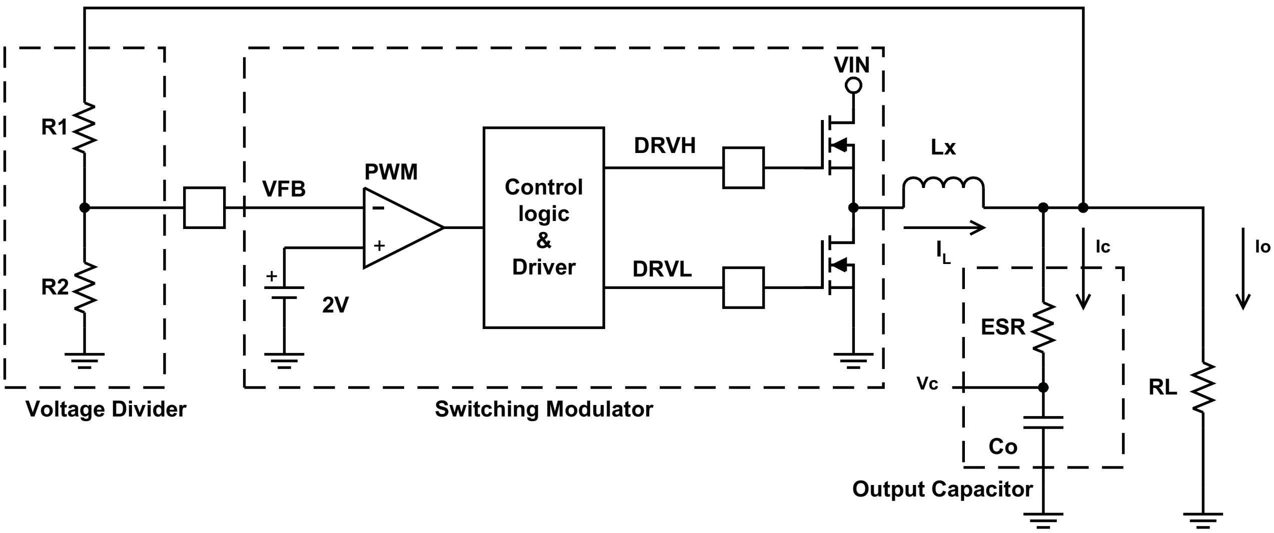


Figure 31. Simplifying the Modulator

The output voltage is compared with internal reference voltage after divider resistors, R1 and R2. The PWM comparator determines the timing to turn on high-side MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle substantially constant. For the loop stability, the 0dB frequency, f_0, defined below need to be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_O} \le \frac{f_{SW}}{4} \tag{1}$$

As f_0 is determined solely by the characteristics of the output capacitor, loop stability of D-CAP mode is determined by the chemistry of the capacitor. For example, specialty polymer capacitors (SP-CAP) have Co in the order of several 100 µF and ESR in range of 10 mΩ. These will make f_0 in the order of 100 kHz or less and the loop will be stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this operational mode.

7.3.4 Ramp Signal

The TPS51125 adds a ramp signal to the 2-V reference in order to improve its jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the S/N ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jitter and stable. The ramp signal is controlled to start with –20 mV at the beginning of ON-cycle and to become 0 mV at the end of OFF-cycle in steady state. By using this scheme, the TPS51125 improve jitter performance without sacrificing the reference accuracy.

7.3.5 Light-Load Condition in Auto-Skip Operation

The TPS51125 automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increase of V_{OUT} ripple. Detail operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its ‘valley’ touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when this zero inductor current is detected. As the load current further decreased, the converter runs in discontinuous conduction mode and it takes longer and longer to discharge the output capacitor to the level that requires next ON cycle. The ON time is kept the same as that in the heavy load condition. In reverse, when the output current increase from light load to heavy load, switching frequency increases to the preset value as the inductor current reaches to the continuous conduction. The transition load point to the light load operation $I_{OUT(LL)}$ (that is, the threshold between continuous and discontinuous conduction mode) can be calculated as follows;

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- f is the PWM switching frequency (2)

Switching frequency versus output current in the light load condition is a function of L, V_{IN} and V_{OUT}, but it decreases almost proportional to the output current from the $I_{OUT(LL)}$ given above. For example, it will be 60 kHz at $I_{OUT(LL)}/5$ if the frequency setting is 300 kHz.

7.3.6 Out-of-Audio Light-Load Operation

Out-of-Audio (OOA) light-load mode is a unique control feature that keeps the switching frequency above acoustic audible frequencies toward virtually no load condition while maintaining best of the art high conversion efficiency. When the Out-of-Audio operation is selected, OOA control circuit monitors the states of both MOSFET and force to change into the ON state if both of MOSFETs are off for more than 32 µs. This means that the top MOSFET is turned on even if the output voltage is higher than the target value so that the output capacitor is tends to be overcharged.

The OOA control circuit detects the over-voltage condition and begins to modulate the on time to keep the output voltage regulated. As a result, the output voltage becomes 0.5% higher than normal light-load operation.

7.3.7 VREG5/VREG3 Linear Regulators

There are two sets of 100-mA standby linear regulators which outputs 5 V and 3.3 V, respectively. The VREG5 serves as the main power supply for the analog circuitry of the device and provides the current for gate drivers. The VREG3 is intended mainly for auxiliary 3.3-V supply for the notebook system during standby mode.

Add a ceramic capacitor with a value of at least 33 µF and place it close to the VREG5 pin, and add at most 10 µF to the VREG3 pin. Total capacitance connected to the VREG3 pin should not exceed 10 µF.

7.3.8 VREG5 Switch Over

When the VO1 voltage becomes higher than 4.7 V AND channel-1 internal powergood flag is generated, internal 5-V LDO regulator is shut off and the VREG5 output is connected to VO1 by internal switch over MOSFET. The 510-µs powergood delay helps a switch over without glitch.

7.3.9 VREG3 Switch Over

When the VO2 voltage becomes higher than 3.15 V AND channel-2 internal powergood flag is generated, internal 3.3-V LDO regulator is shut off and the VREG3 output is connected to VO2 by internal switch over MOSFET. The 510-µs powergood delay helps a switch over without glitch.

7.3.10 Powergood

The TPS51125 has one powergood output that indicates 'high' when both switcher outputs are within the targets (AND gated). The powergood function is activated with 2-ms internal delay after ENTRIPx goes high. If the output voltage becomes within +/-5% of the target value, internal comparators detect power good state and the powergood signal becomes high after 510-µs internal delay. Therefore PGOOD goes high around 2.5 ms after ENTRIPx goes high. If the output voltage goes outside of +/-10% of the target value, the powergood signal becomes low after 2-µs internal delay. The powergood output is an open-drain output and is needed to be pulled up outside.

Also note that, in the case of Auto-skip or Out-of-Audio™ mode, if the output voltage goes +10% above the target value and the power-good signal flags low, then the loop attempts to correct the output by turning on the low-side driver (forced PWM mode). After the feedback voltage returns to be within +5% of the target value and the power-good signal goes high, the controller returns back to auto-skip mode or Out-of-Audio mode.

7.3.11 Output Discharge Control

When ENTRIPx is low, the TPS51125 discharges outputs using internal MOSFET which is connected to VOx and GND. The current capability of these MOSFETs is limited to discharge slowly.

7.3.12 Low-Side Driver

The low-side driver is designed to drive high current low $R_{DS(on)}$ N-channel MOSFETs. The drive capability is represented by its internal resistance, which are 4 Ω for VREG5 to DRVLx and 1.5 Ω for DRVLx to GND. A dead time to prevent shoot through is internally generated between top MOSFET off to bottom MOSFET on, and bottom MOSFET off to top MOSFET on. 5-V bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by an input capacitor connected between VREG5 and GND. The average drive current is equal to the gate charge at Vgs = 5 V times switching frequency. This gate drive current as well as the high-side gate drive current times 5 V makes the driving power which need to be dissipated from TPS51125 package.

7.3.13 High-Side Driver

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFETs. When configured as a floating driver, 5-V bias voltage is delivered from VREG5 supply. The average drive current is also calculated by the gate charge at Vgs = 5 V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between VBSTx and LLx pins. The drive capability is represented by its internal resistance, which are 4 Ω for VBSTx to DRVHx and 1.5Ω for DRVHx to LLx.

7.3.14 VCLK for Charge Pump

270-kHz clock signal can be used for charge pump circuit to generate approximately 15-V dc voltage. The clock signal becomes available when EN0 becomes higher than 2.4 V or open state. Example of control circuit is shown in Figure 32. Note that the clock driver uses VO1 as its power supply. Regardless of enable or disable of VCLK, power consumption of the TPS51125 is almost the same. Therefore even if VCLK is not used, one can let EN0 pin open or supply logic 'high', as shown in Figure 32, and let VCLK pin open. This approach further reduces the external part count.

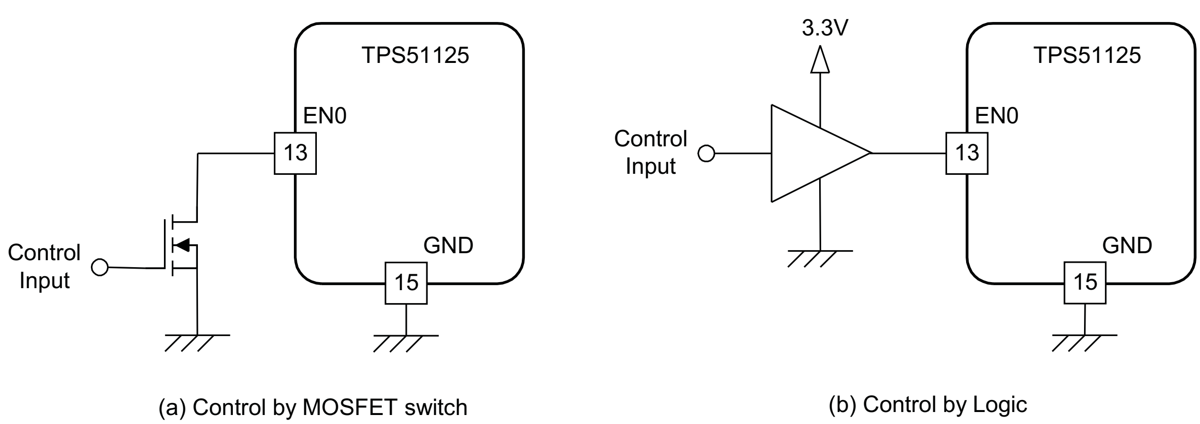


Figure 32. Control Example of EN0 Master Enable

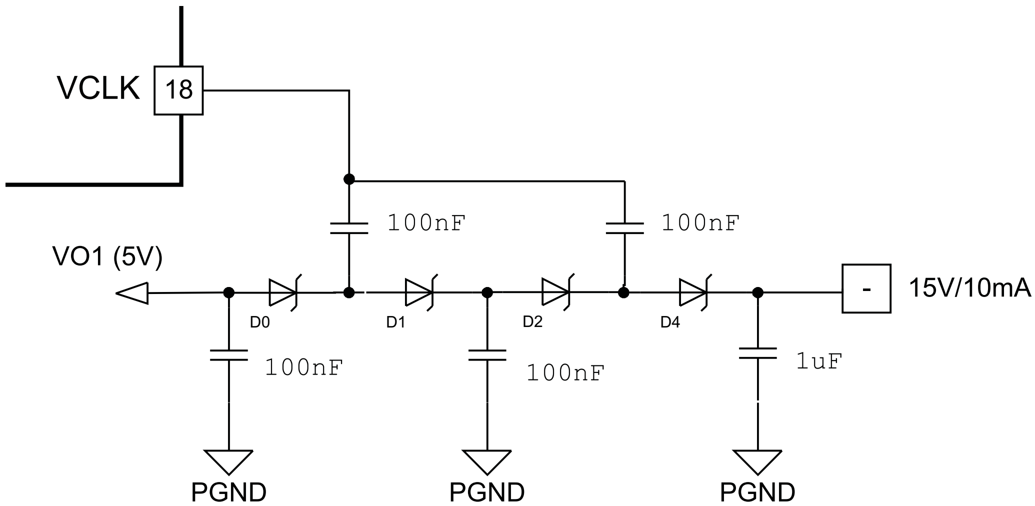


Figure 33. 15-V / 10-mA Charge Pump Configuration

7.3.15 Current Protection

TPS51125 has cycle-by-cycle over current limiting control. The inductor current is monitored during the OFF state and the controller keeps the OFF state during the inductor current is larger than the over current trip level. In order to provide both good accuracy and cost effective solution, TPS51125 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. ENTRIPx pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. ENTRIPx terminal sources I_{TRIP} current, which is 10 µA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as below. Note that the V_{TRIP} is limited up to about 205 mV internally.

$$V_{TRIP}\left(mV\right)=\frac{R_{TRIP}\left(k\Omega\right)\times I_{TRIP}\left(\mu A\right)}{9}-24\left(mV\right) \quad (3)$$

External leakage current to ENTRIPx pin should be minimized to obtain accurate OCL trip voltage.

The inductor current is monitored by the voltage between GND pin and LLx pin so that LLx pin should be connected to the drain terminal of the bottom MOSFET properly. Itrip has 4500 ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the proper current sensing device, i.e. the source terminal of the bottom MOSFET.

As the comparison is done during the OFF state, V_{TRIP} sets valley level of the inductor current. Thus, the load current at over current threshold, I_{OCP}, can be calculated in Equation 4.

$$I_{OCP}=\frac{V_{TRIP}}{R_{DS(on)}}+\frac{I_{RIPPLE}}{2}=\frac{V_{TRIP}}{R_{DS(on)}}+\frac{1}{2\times L\times f}\times\frac{\left(V_{IN}-V_{OUT}\right)\times V_{OUT}}{V_{IN}} \quad (4)$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it ends up with crossing the under voltage protection threshold and shutdown both channels.

7.3.16 Overvoltage and Undervoltage Protection

TPS51125 monitors a resistor divided feedback voltage to detect over and undervoltage. When the feedback voltage becomes higher than 115% of the target voltage, the OVP comparator output goes high and the circuit latches as the top MOSFET driver OFF and the bottom MOSFET driver ON.

Also, TPS51125 monitors VOx voltage directly and if it becomes greater than 5.75 V the TPS51125 turns off the top MOSFET driver.

When the feedback voltage becomes lower than 60% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 32 µs, TPS51125 latches OFF both top and bottom MOSFETs drivers, and shut off both drivers of another channel. This function is enabled after 2 ms following ENTRIPx has become high.

7.3.17 UVLO Protection

TPS51125 has VREG5 undervoltage lockout protection (UVLO). When the VREG5 voltage is lower than UVLO threshold voltage both switch mode power supplies are shut off. This is nonlatch protection. When the VREG3 voltage is lower than (VO2 - 1 V), both switch mode power supplies are also shut off.

7.3.18 Thermal Shutdown

TPS51125 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), TPS51125 is shut off including LDOs. This is nonlatch protection.

7.4 Device Functional Modes

7.4.1 Enable and Soft-Start

EN0 is the control pin of VREG5, VREG3 and VREF regulators. Bring this node down to GND disables those three regulators and minimize the shutdown supply current to 10 µA. Pulling this node up to 3.3 V or 5 V will turn the three regulators on to standby mode. The two switch mode power supplies (channel-1, channel-2) become ready to enable at this standby mode. The TPS51125 has an internal, 1.6 ms, voltage servo softstart for each channel. When the ENTRIPx pin becomes higher than the enable threshold voltage, which is typically 430 mV, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start up. As TPS51125 shares one DAC with both channels, if ENTRIPx pin becomes higher than the enable threshold voltage while another channel is starting up, soft start is postponed until another channel soft start has completed. If both of ENTRIP1 and ENTRIP2 become higher than the enable threshold voltage at a same time (within 60 µs), both channels start up at same time.

Table 2. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don’t Care	Don’t Care	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	On	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	On

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS51125 is typically used as a dual-synchronous buck controller, which convert an input voltage ranging from 5.5 V to 28 V, to output voltage 5 V and 3.3 V respectively, targeted for notebook system-power supply solutions.

8.2 Typical Application

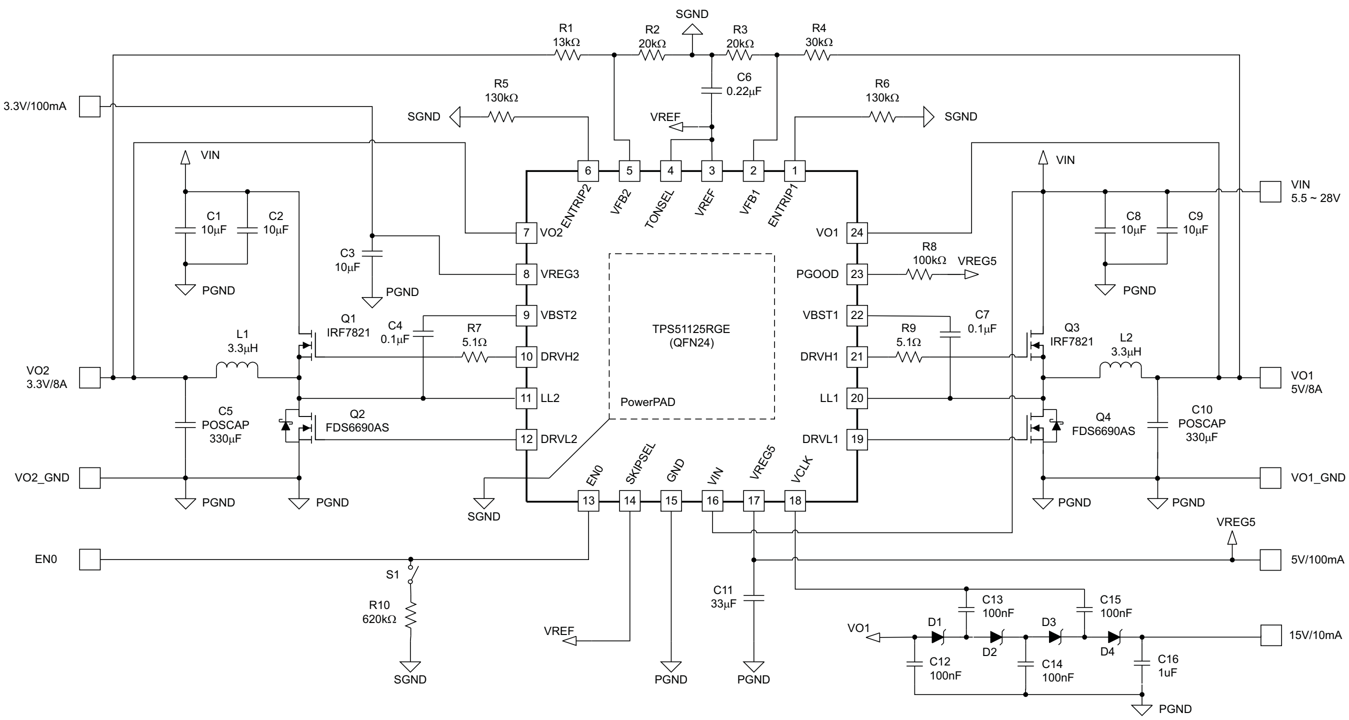


Figure 34. 5-V/8-A, 3.3-V/8-A Application Circuit (245-kHz/305-kHz Setting)

8.2.1 Design Requirements

Table 3. Design Parameters

PARAMETER	VALUE
Input voltage range	5.5 V to 28 V
Channel 1 output voltage	5 V
Channel 1 output current	8 A
Channel 2 output voltage	3.3 V
Channel 2 output current	8 A

8.2.2 Detailed Design Procedure

Table 4. List of Materials for 5-V / 8-A, 3.3-V / 8-A Application Circuit

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C2, C8, C9	10 µ F, 25 V	Taiyo Yuden	TMK325BJ106MM
C3	10 µF, 6.3 V	TDK	C2012X5R0J106K
C11	33 µF, 6.3 V	TDK	C3216X5RBJ336M
C5, C10	330 µF, 6.3 V, 25 mΩ	Sanyo	6TPE330ML
L1, L2	3.3 µH, 15.6 A, 5.92 mΩ	TOKO	FDA1055-3R3M
Q1, Q3	30 V, 9.5 mΩ	IR	IRF7821
Q2, Q4 (1)	30 V, 12 mΩ	Fairchild	FDS6690AS

(1) Please use MOSFET with integrated Schottky barrier diode (SBD) for low side, or add SBD in parallel with normal MOSFET.

8.2.2.1 Determine Output Voltage

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 31. R1 is connected between VFBx pin and the output, and R2 is connected betwen the VFBx pin and GND. Recommended R2 value is from 10 kΩ to 20 kΩ. Determine R1 using equation as below.

$$R1 = \frac{\left(V_{OUT} - 2.0\right)}{2.0} \times R2 \tag{5}$$

8.2.2.2 Choose the Inductor

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves S/N ratio and helps stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{6}$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated as follows.

$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{L \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{7}$$

8.2.2.3 Choose the Output Capacitors

Organic semiconductor capacitors or specialty polymer capacitors are recommended. Determine ESR to meet required ripple voltage. A quick approximation is as shown in Equation 8.

$$ESR = \frac{V_{OUT} \times 20(mV) \times (1 - D)}{2(V) \times I_{RIPPLE}} = \frac{20(mV) \times L \times f}{2(V)}$$

where

- D is the duty cycle
- the required output ripple slope is approximately 20 mV per t_{SW} (switching period) in terms of VFB terminal voltage (8)

8.2.2.4 Choose the Low-Side MOSFET

It is highly recommended that the low-side MOSFET should have an integrated Schottky barrier diode, or an external Schottky barrier diode in parallel to achieve stable operation.

8.2.3 Application Curves

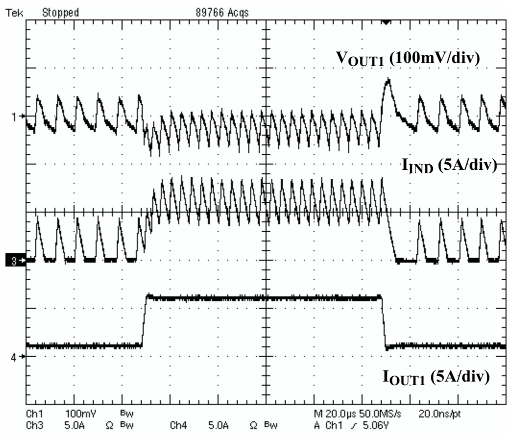


Figure 35. 5-V Load Transient Response

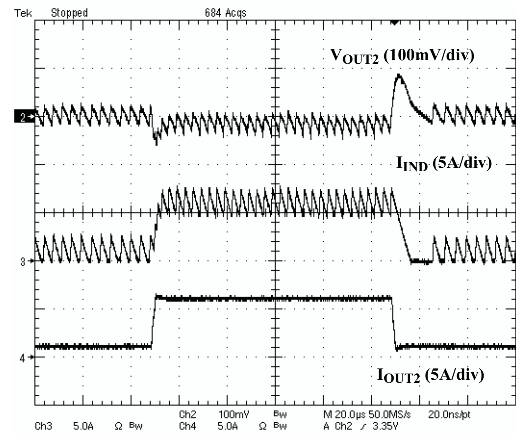


Figure 36. 3.3-V Load Transient Response

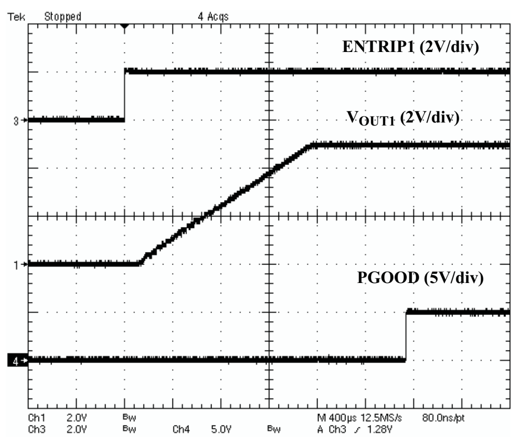


Figure 37. 5-V Start-up Waveforms

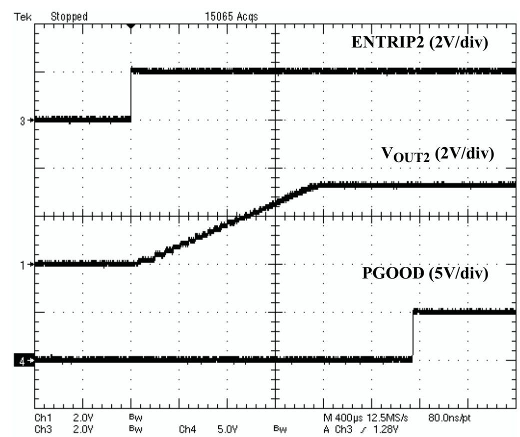


Figure 38. 3.3-V Start-up Waveforms

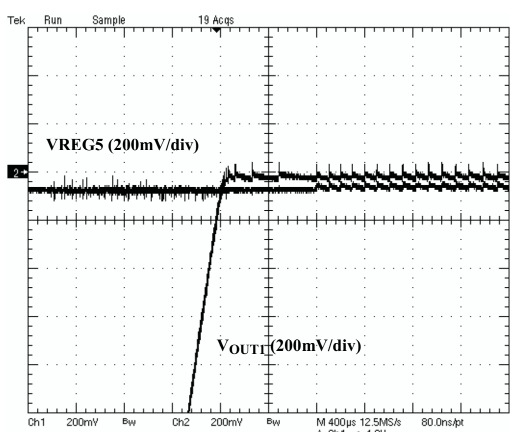


Figure 39. 5-V Switchover Waveforms

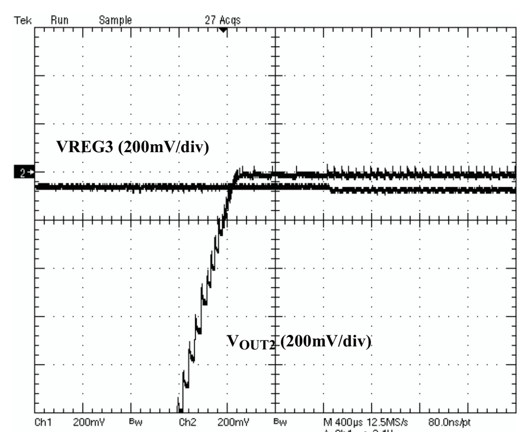


Figure 40. 3.3-V Switchover Waveforms

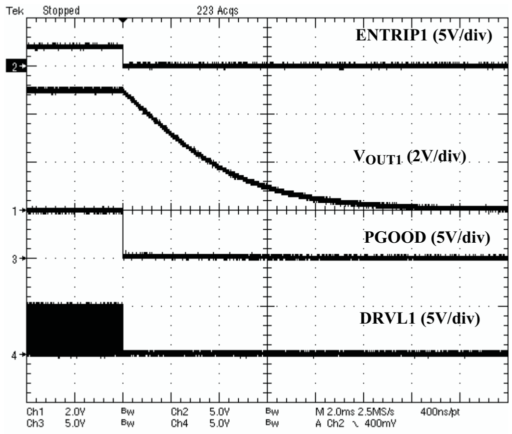


Figure 41. 5-V Soft-Stop Waveforms

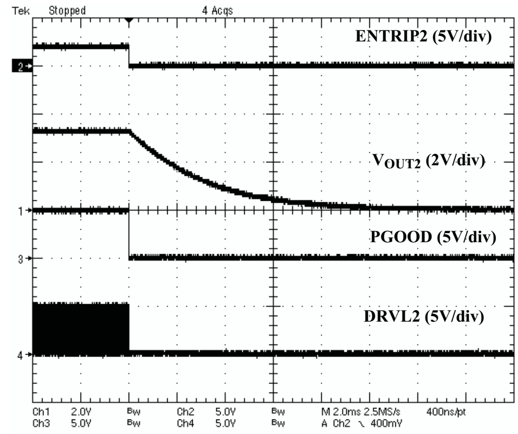


Figure 42. 3.3-V Soft-Stop Waveforms

9 Power Supply Recommendations

The TPS51125 is designed to operate from input supply voltage in the range of 5.5 V to 28 V, make sure power supply voltage in this range.

10 Layout

10.1 Layout Guidelines

Consider these points before starting layout work using the TPS51125.

- TPS51125 has only one GND pin and special care of GND trace design makes operation stable, especially when both channels operate. Group GND terminals of output voltage divider of both channels and the VREF capacitor as close as possible, connect them to an inner GND plane with PowerPad, overcurrent setting resistor, EN0 pull-down resistor and EN0 bypass capacitor as shown in the thin GND line of Figure 43. This trace is named Signal Ground (SGND). Group ground terminals of VIN capacitor(s), VOUT capacitor(s) and source of low-side MOSFETs as close as possible, and connect them to another inner GND plane with GND pin of the device, GND terminal of VREG3 and VREG5 capacitors and 15-V charge-pump circuit as shown in the bold GND line of Figure 43. This trace is named Power Ground (PGND). SGND should be connected to PGND at the middle point between ground terminal of VOUT capacitors.
- Inductor, VOUT capacitor(s), VIN capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Power components of each channel should be at the same distance from the TPS51125. Other small signal parts should be placed on another side (component side). Inner GND planes above should shield and isolate the small signal traces from noisy power lines.
- PCB trace defined as LLx node, which connects to source of high-side MOSFET, drain of low-side MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
- VREG5 requires capacitance of at least 33 μF and VREG3 requires capacitance of at most 10 μF. VREF requires a 220-nF ceramic bypass capacitor which should be placed close to the device and traces should be no longer than 10 mm.
- Connect the overcurrent setting resistors from ENTRIPx to SGND and close to the device, right next to the device if possible.
- The discharge path (VOx) should have a dedicated trace to the output capacitor; separate from the output voltage sensing trace. When LDO5 is switched over Vo1 trace should be 1.5 mm with no loops. When LDO3 is switched over and loaded Vo2 trace should also be 1.5 mm with no loops. There is no restriction for just monitoring Vox. Make the feedback current setting resistor (the resistor between VFBx to SGND) close to the device. Place on the component side and avoid vias between this resistor and the device.
- Connections from the drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65-mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- All sensitive analog traces and components such as VOx, VFBx, VREF, GND, EN0, ENTRIPx, PGOOD, TONSEL and SKIPSEL should be placed away from high-voltage switching nodes such as LLx, DRVLx, DRVHx and VCLK nodes to avoid coupling.
- Traces for VFB1 and VFB2 should be short and laid apart each other to avoid channel to channel interference.
- In order to effectively remove heat from the package, prepare thermal land and solder to the package's thermal pad. Three by three or more vias with a 0.33-mm (13 mils) diameter connected from the thermal land to the internal ground plane should be used to help dissipation. This thermal land underneath the package should be connected to SGND, and should NOT be connected to PGND.

10.2 Layout Example

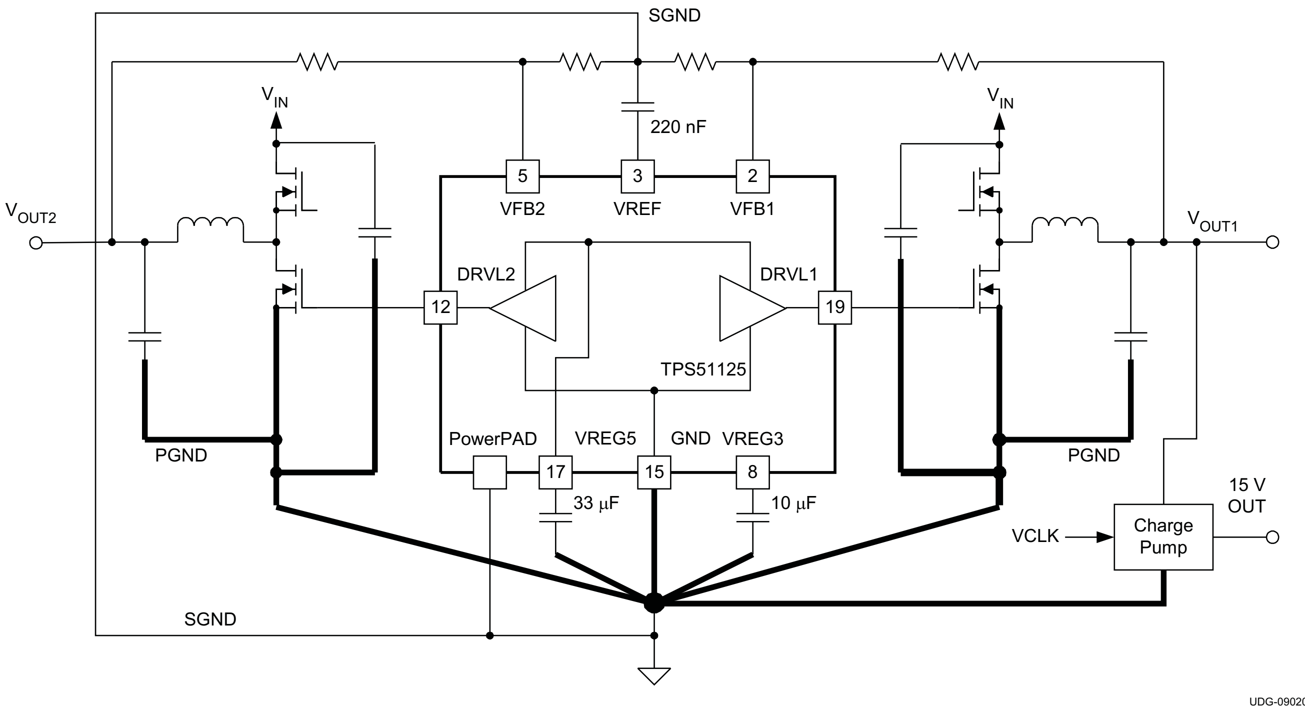


Figure 43. Ground System

Layout Example (continued)

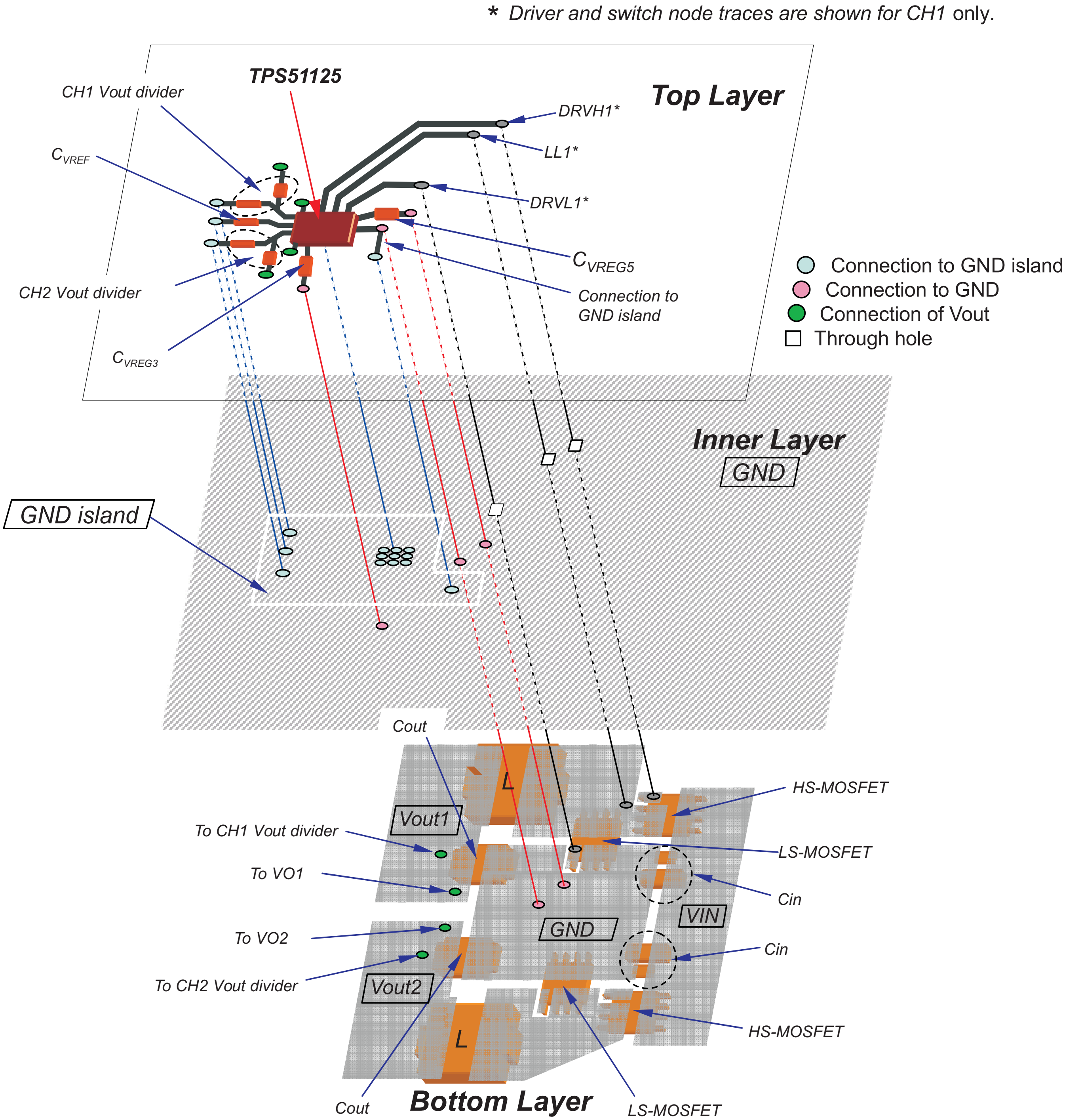


Figure 44. PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Trademarks

D-CAP is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

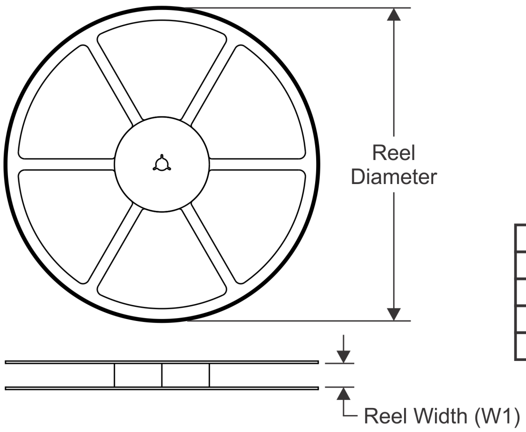
SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

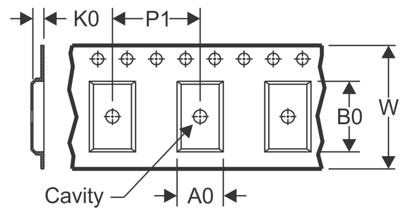
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

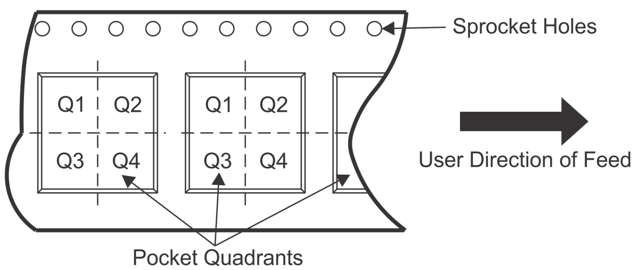


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

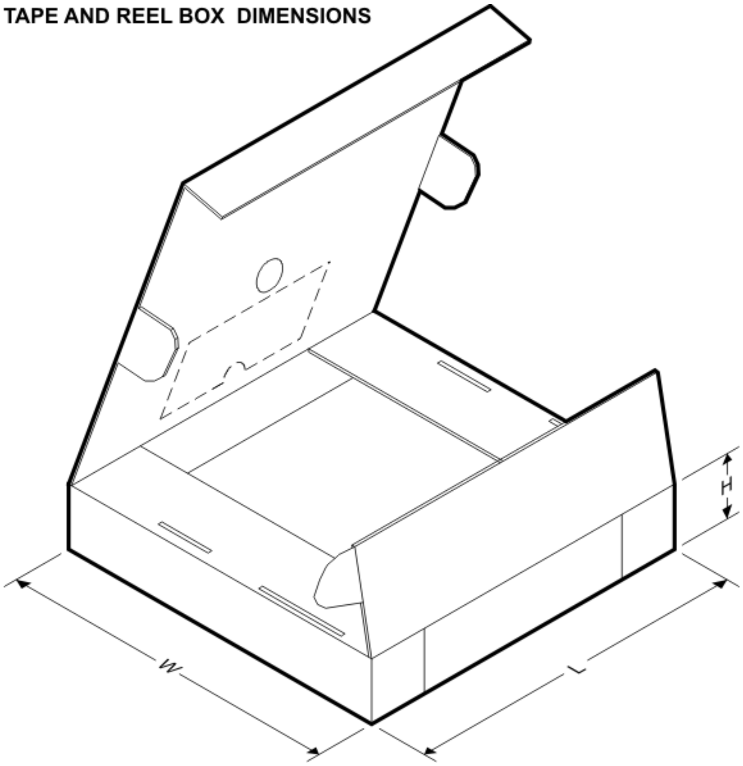
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51125RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS51125RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS51125RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

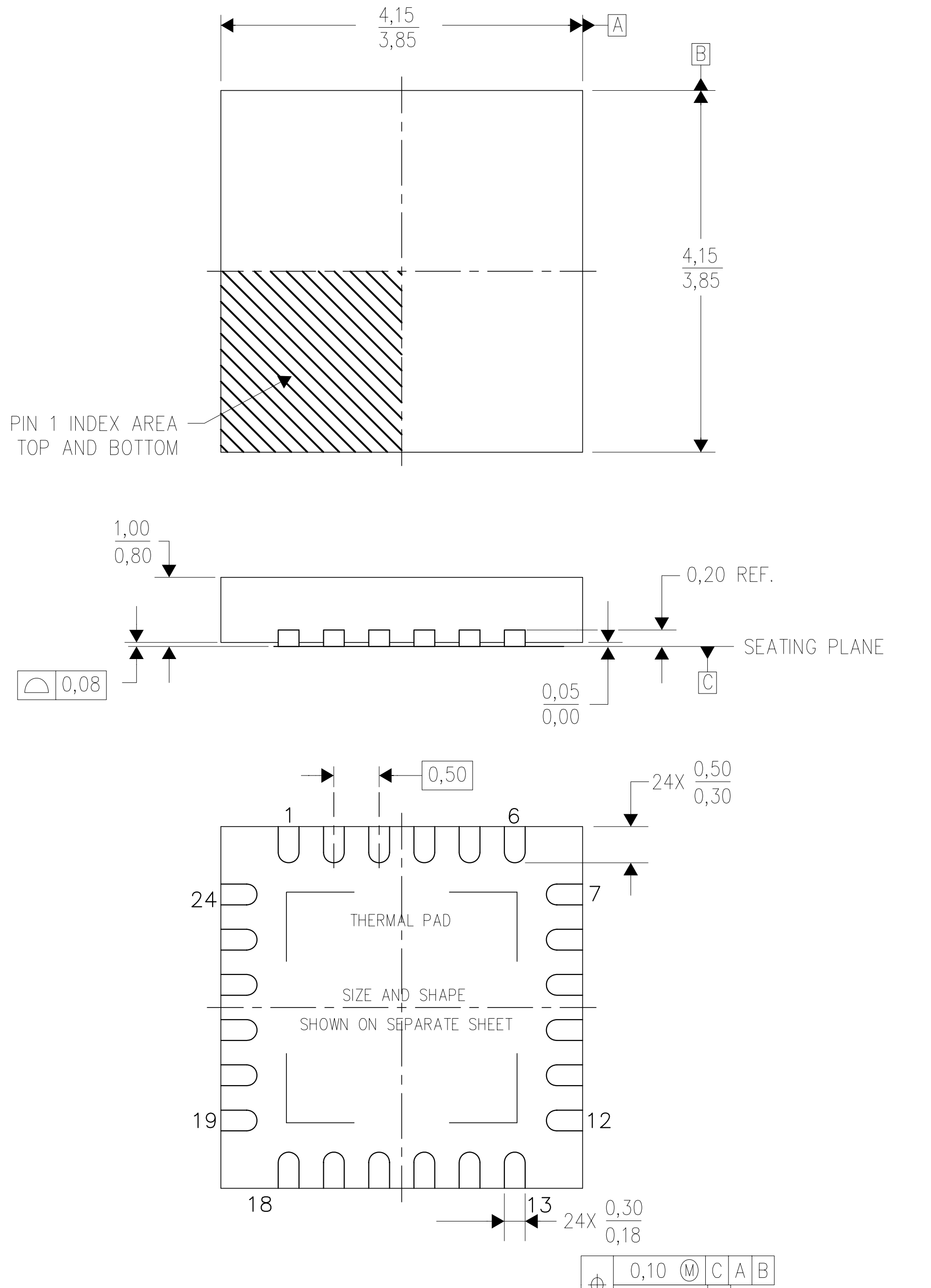
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51125RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS51125RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS51125RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

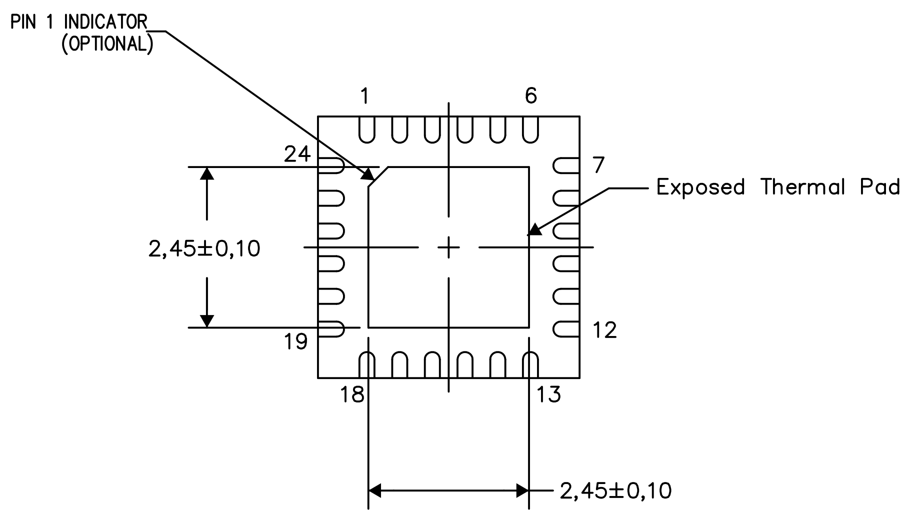
RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



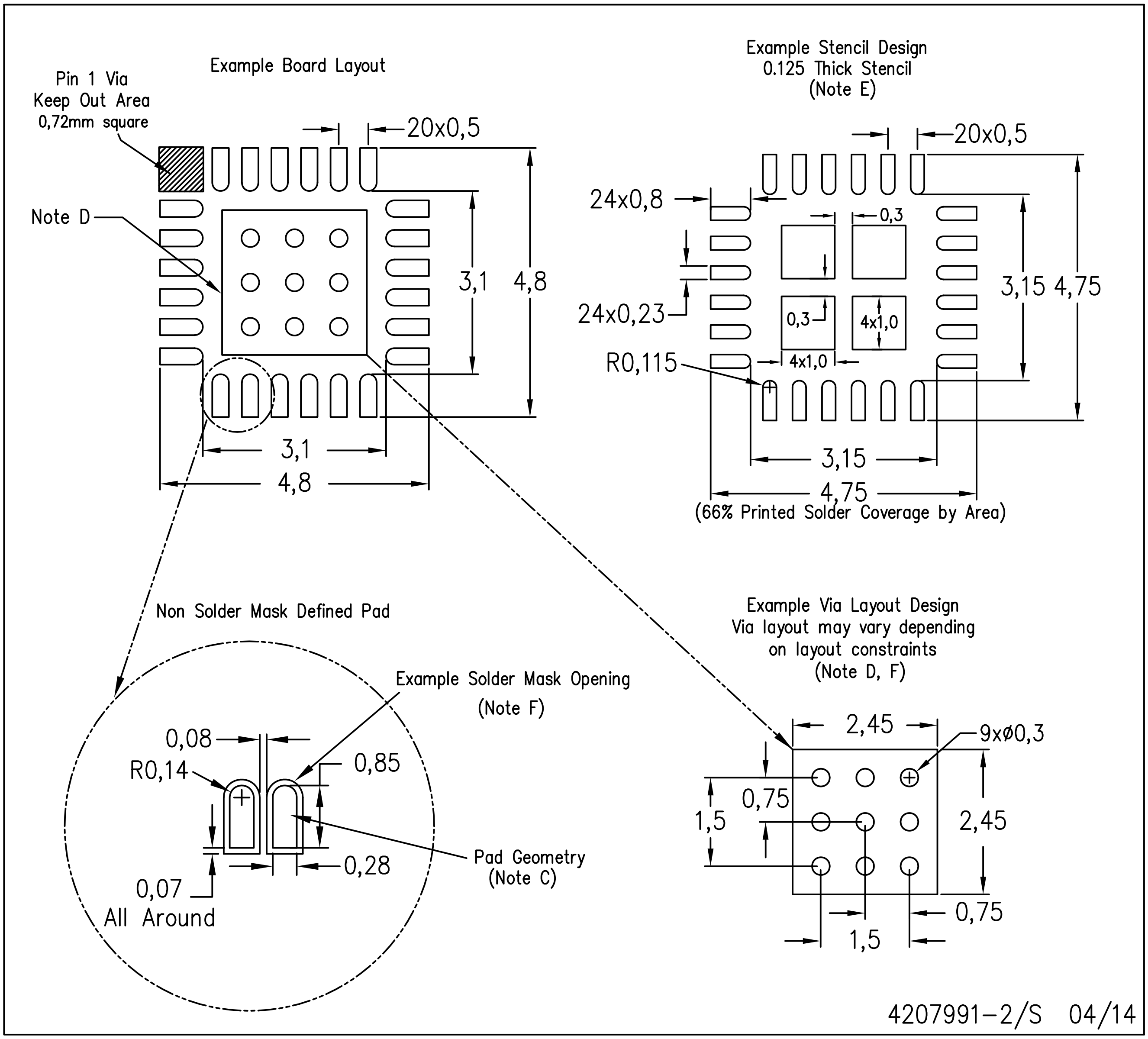
Bottom View

Exposed Thermal Pad Dimensions

4206344-3/AH 08/14

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.