TQP7M9102

½ W High Linearity Amplifier

Applications

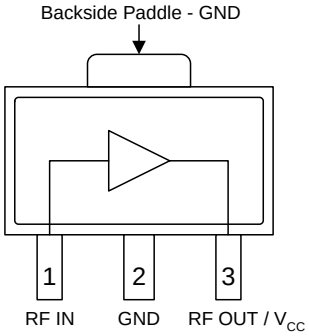
- Repeaters
- Mobile Infrastructure
- CDMA / WCDMA / LTE
- General Purpose Wireless

3 Pin SOT-89 Package

Product Features

- 400-4000 MHz
- +27.5 dBm P1dB
- +44 dBm Output IP3
- 17.8 dB Gain at 2140 MHz
- +5 V Single Supply, 135 mA Current
- Internal RF overdrive protection
- Internal DC overvoltage protection
- On chip ESD protection
- SOT-89 Package

Functional Block Diagram



General Description

The TQP7M9102 is a high linearity driver amplifier in a low-cost, RoHS compliant, surface mount package. This InGaP/GaAs HBT delivers high performance across a broad range of frequencies with +44 dBm OIP3 and +27.5 dBm P1dB while only consuming 135 mA quiescent current. All devices are 100% RF and DC tested.

The TQP7M9102 incorporates on-chip features that differentiate it from other products in the market. The amplifier integrates an on-chip DC over-voltage and RF over-drive protection. This protects the amplifier from electrical DC voltage surges and high input RF input power levels that may occur in a system. On-chip ESD protection allows the amplifier to have a very robust Class 2 HBM ESD rating.

The TQP7M9102 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G / 4G base stations.

Pin Configuration

Pin No.	Label
1	RF IN
2	GND
3	RF OUT / V_{CC}
Backside Paddle	GND

Ordering Information

Part No.	Description
TQP7M9102	0.5 W High Linearity Amplifier
TQP7M9102−PCB900	869−960 MHz Evaluation Board
TQP7M9102−PCB2140	2.11–2.17 GHz Evaluation Board
TQP7M9102−PCB2600	2.5–2.7 GHz Evaluation Board
Standard T/R size = 1000 pieces on a 7” reel	

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to +150°C
RF Input Power, CW, 50Ω, T=25°C	+27 dBm
Device Voltage (V_{CC})	+8 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{CC})	+4.75	+5	+5.25	V
T_{CASE}	-40		+105	°C
Tj for >10^6 hours MTTF			+170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC}=+5V, Temp.=+25 °C, matched 2140 MHz reference circuit

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		400		4000	MHz
Test Frequency			2140		MHz
Gain		15.5	17.8		dB
Input Return Loss			12		dB
Output Return Loss			10		dB
Output P1dB		+26.4	+27.5		dBm
Output IP3	Pout = +9 dBm/tone, Δf = 1 MHz	+41	+43.8		dBm
WCDMA Channel Power(1)	−50 dBc ACLR		+18.5		dBm
Noise Figure			3.9		dB
Quiescent Current, I_{CQ}	See Note 1	115	137	155	mA
Thermal Resistance, θ_{jc}	Junction to case			50	°C/W

Notes:
1. ACLR test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

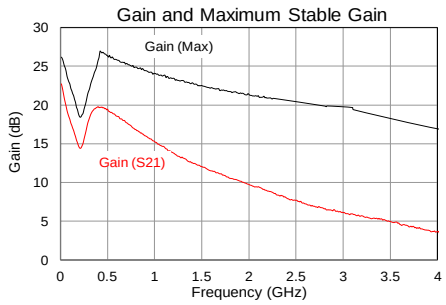
Performance Summary Table

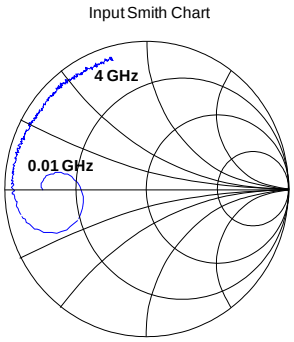
Test conditions unless otherwise noted: V_{CC} =+5V, Temp.= +25 °C, band specific matching networks(1)

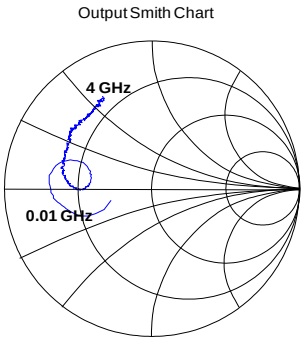
Frequency	768	869	960	1540	1840	1960	2140	2140	2350	2600	3500	MHz
Gain	20.9	21.8	21.7	20.2	20.0	18.4	15.5	17.8	16.0	14.5	14.5	dB
Input Return Loss	9	10	17	15	17	13	8	12	17	14.5	17	dB
Output Return Loss	8	12	9	6	7.5	7	8	11	8	8	11	dB
Output P1dB	+28.4	+27.3	+27.4	+28.2	+27.5	+27.0	+30.7	+27.6	+27.2	+28.0	+26.2	dBm
Output IP3	+44	+43	+44	+51	+42	+46	+38	+44	+44	+44	+45	dBm

Notes:
1. Reference designs for the various frequencies are either included on this datasheet or may be obtained by contacting sjcapplications.engineering@tqs.com.

Device Characterization Data







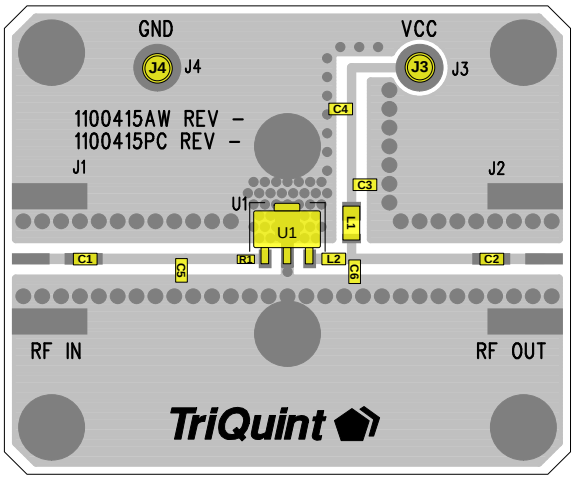
Note: The gain for the unmatched device in a 50 ohm system is shown as the black trace labeled "Gain (S21)". In a circuit tuned for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown as the red trace [Gmax]. The impedance Smith chart plots are shown from 0.01 to 4 GHz.

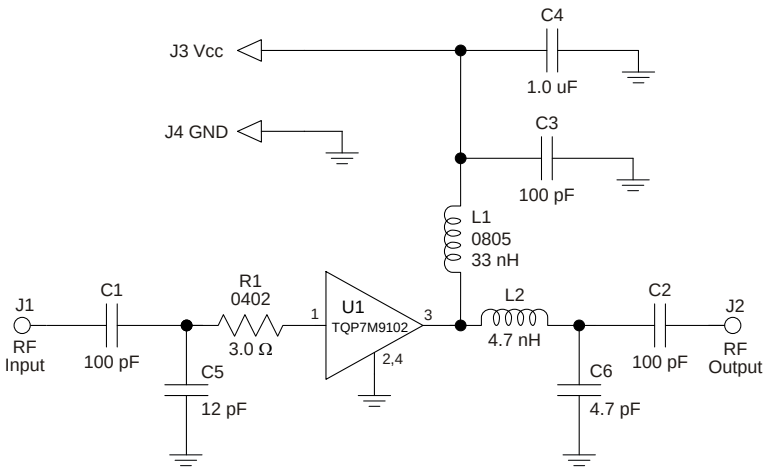
S-Parameters

Test Conditions: V_{CC}=+5 V, I_{CQ}=135 mA (typ.), Temp.=+25 °C, unmatched 50 Ohm system, reference plane at device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-2.55	176.64	20.38	156.15	-35.04	-9.37	-5.88	-159.98
100	-2.91	172.21	18.15	151.53	-35.97	-20.12	-4.45	-167.94
200	-5.79	172.18	14.52	160.74	-41.94	-60.14	-3.20	177.62
400	-1.41	-163.37	19.80	154.97	-34.61	49.55	-7.14	165.58
600	-0.52	179.77	18.56	125.67	-33.11	19.10	-6.55	178.58
800	-0.45	171.80	16.85	108.86	-32.96	8.46	-5.41	178.08
1000	-0.49	165.43	15.28	95.36	-32.92	-1.08	-4.76	174.13
1200	-0.60	160.30	13.79	85.52	-33.15	-4.65	-4.38	171.06
1400	-0.60	157.51	12.55	77.70	-33.23	-9.05	-4.24	167.58
1600	-0.67	152.76	11.49	69.57	-33.03	-15.12	-4.15	163.37
1800	-0.74	148.28	10.53	62.39	-32.96	-19.02	-4.00	159.18
2000	-0.72	143.55	9.75	54.69	-33.03	-20.90	-3.89	155.31
2200	-0.78	139.03	8.88	48.56	-32.96	-25.51	-3.77	150.66
2400	-0.71	135.24	7.99	42.25	-32.88	-27.98	-3.40	146.69
2600	-0.74	131.98	7.23	36.47	-33.43	-30.45	-3.38	144.96
2800	-0.75	128.79	6.58	31.19	-33.15	-33.43	-3.44	142.02
3000	-0.80	126.32	6.09	26.41	-33.23	-36.48	-3.50	139.73
3200	-0.75	122.75	5.69	20.73	-33.43	-37.86	-3.39	137.14
3400	-0.81	118.06	5.30	14.38	-33.39	-44.57	-3.48	130.99
3600	-0.82	113.62	4.59	7.77	-33.03	-43.44	-3.34	124.40
3800	-0.71	108.88	4.07	1.73	-32.92	-50.92	-3.04	120.16
4000	-0.68	105.86	3.64	-2.85	-33.15	-54.00	-2.92	118.44

746 – 768 MHz Reference Design





Notes:

1. See Evaluation Board PCB Information for material and stack up.
2. The recommended component values are dependent upon the frequency of operation.
3. All components are of 0603 size unless stated on the schematic.
4. Critical component placement locations:
   - Distance from U1 Pin Pad 1 (left edge) to R1 (right edge): 0 mils
   - Distance from U1 Pin Pad 1 (left edge) to C6 (right edge): 60 mils
   - Distance from U1 Pin Pad 1 (left edge) to C5 (right edge): 230 mils
   - Distance from U1 Pin Pad 3 (right edge) to L2 (left edge): 0 mils

Bill of Material 746 – 768 MHz Reference Design

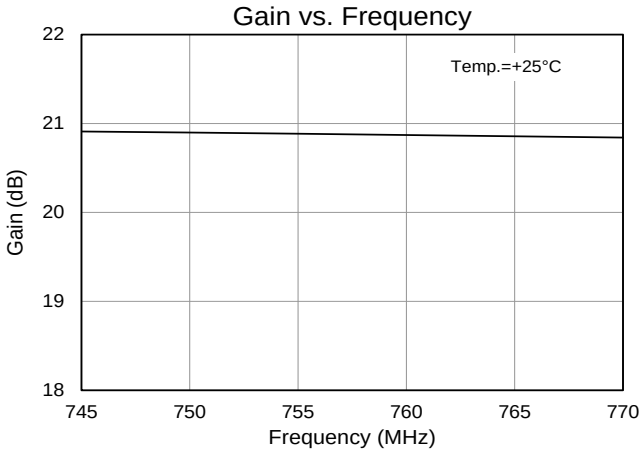
Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	½ W High Linearity Amplifier	Qorvo	TQP7M9102
C1 , C2 , C3	100 pF	CAP, 0603, +/-5%. 100V NPO/COG	various	
C5	12 pF	CAP, 0603, +/-2%. 50V. NPO/COG	various	
C6	4.7 pF	CAP, 0603, +/-0.1PF. 100V. NPO/COG	various	
C4	1.0 uF	CAP, 0603, 10%, X5R , 10V	various	
L1	33 nH	IND, 0805, 5%, Ceramic	Coilcraft	0805CS-331XJL
L2	4.7 nH	IND, 0603, +/-0.3. >5600MHZ	Toko	LL1608-FSL4N7S
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	

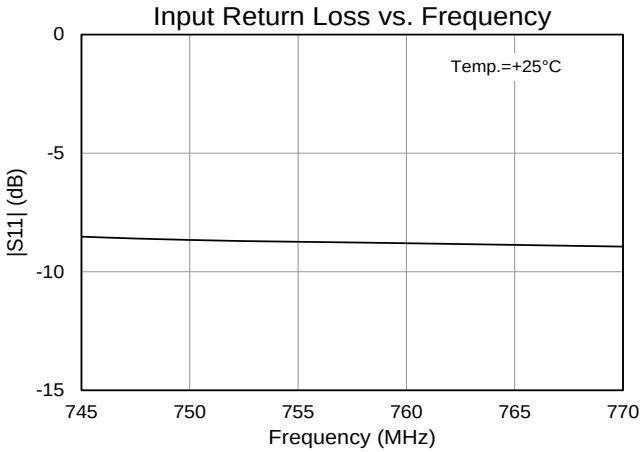
Typical Performance 746 – 768 MHz Reference Design

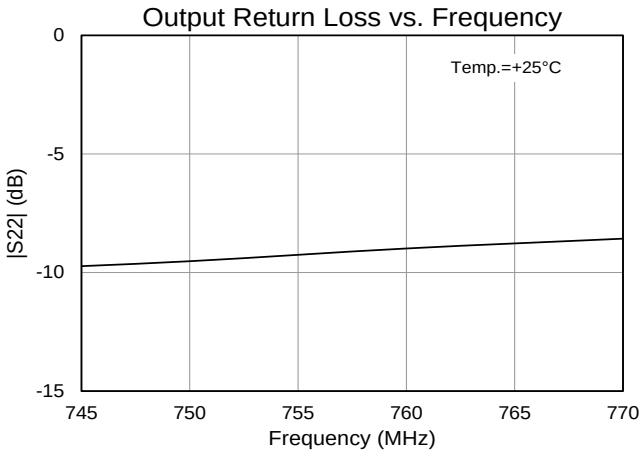
Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

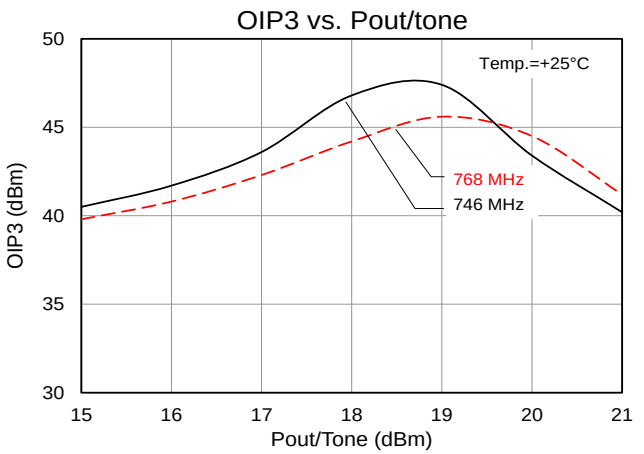
Parameter	Conditions	Typical Value		Units
Frequency		746	768	MHz
Gain		20.9	20.9	dB
Input Return Loss		8	9	dB
Output Return Loss		10	8	dB
Output P1dB		+28.2	+28.4	dBm
Output IP3	Pout= +18 dBm/tone, Δf= 1 MHz	+47	+44	dBm

Performance Plots 746 – 768 MHz Reference Design

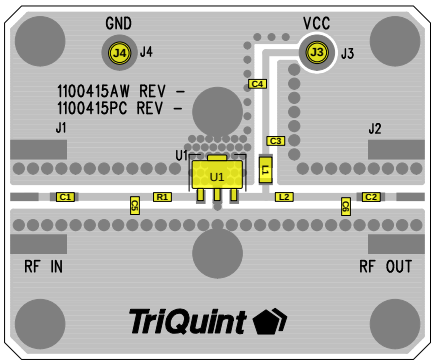


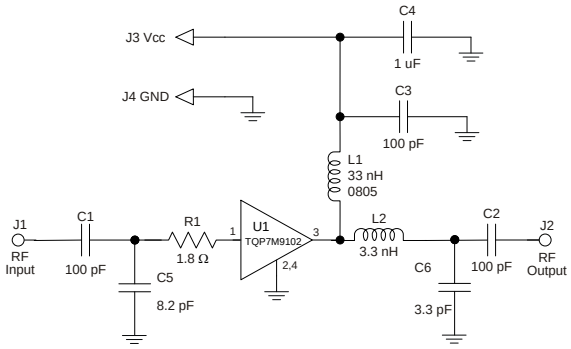






869 – 894 MHz Evaluation Board (TQP7M9102−PCB900)





Notes:

1. See Evaluation Board PCB Information for material and stack up.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The recommended component values are dependent upon the frequency of operation.
4. All components are of 0603 size unless stated on the schematic.
5. Critical component placement locations:
   - Distance from U1 Pin 1 (left edge) to R1 (right edge): 90 mils (4.3 deg. at 920 MHz)
   - Distance from R1 (left edge) to C5 (right edge): 70 mils (3.3 deg. at 920 MHz)
   - Distance from U1 Pin 3 (right edge) to L2 (left edge): 120 mils (5.7 deg. at 920 MHz)
   - Distance from U1 Pin 3 (right edge) to C6 (left edge): 370 mils (17.6 deg. at 920 MHz)

Bill of Material TQP7M9102−PCB900

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	TQP7M9102 Amplifier, SOT-89 pkg.	Qorvo	TQP7M9102
R1	1.8 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
L2	3.3 nH	Inductor, 0603, +/-0.3 nH	Toko	LL1608-FSL3N3S
L1	33 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-330XJLB
C5	8.2 pF	Cap., Chip, 0603, +/-0.1pF. 200V.	AVX	06032U8R2BAT2A
C6	3.3 pF	Cap., Chip, 0603, +/-0.1pF. 200V.	AVX	06032U3R3BAT2A
C1, C2, C3	100 pF	Cap., Chip, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	

Typical Performance TQP7M9102−PCB900

Test conditions unless otherwise noted: V_{CC}=+5V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

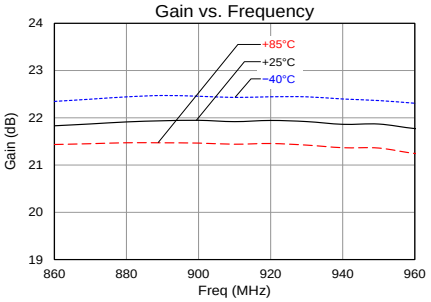
Parameter	Conditions	Typical Value			Units
Frequency		869	920	960	MHz
Gain		21.8	21.9	21.7	dB
Input Return Loss		10	16	17	dB
Output Return Loss		12	10	9	dB
Output P1dB		+27.3	+27.4	+27.4	dBm
OIP3	Pout= +19 dBm/tone, Δf=1 MHz	+42.7	+43.4	+43.9	dBm
WCDMA Channel Power[1]	−50 dBc ACLR	+18.0	+18.2	+18.1	dBm
Noise Figure		5.9	5.9	5.9	dB

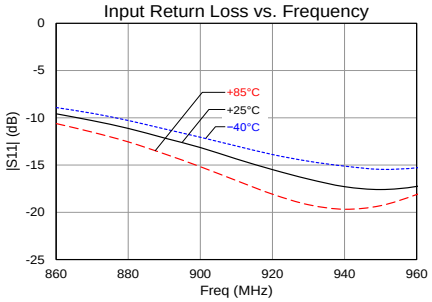
Notes:

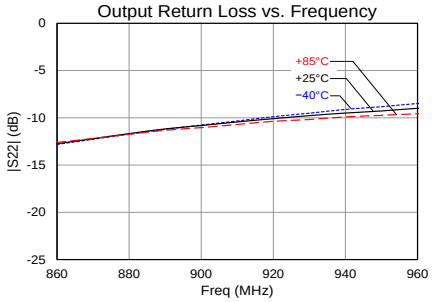
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

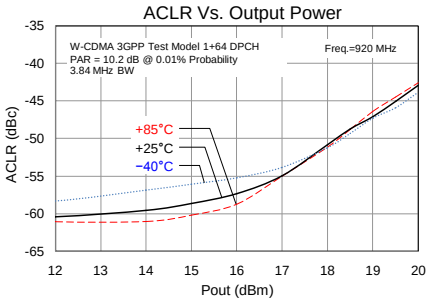
Performance Plots TQP7M9102−PCB900

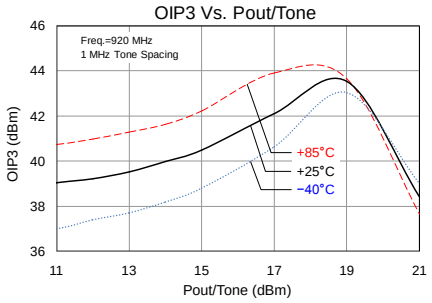
Test conditions unless otherwise noted: V_{CC}=+5V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

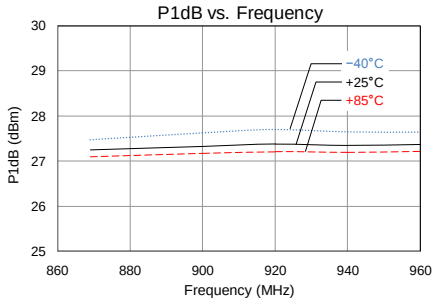


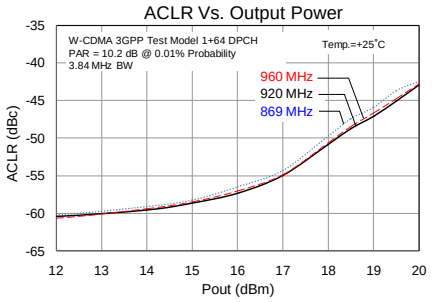


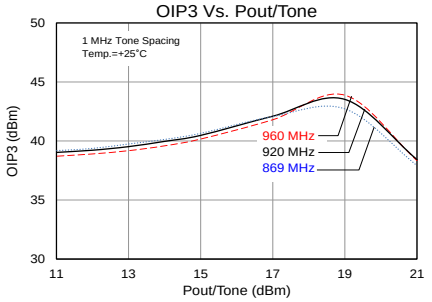


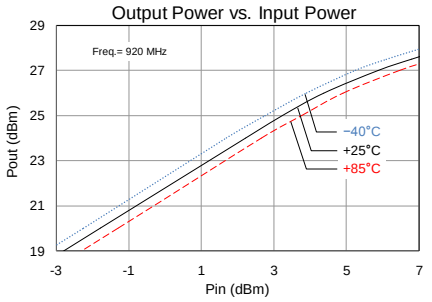


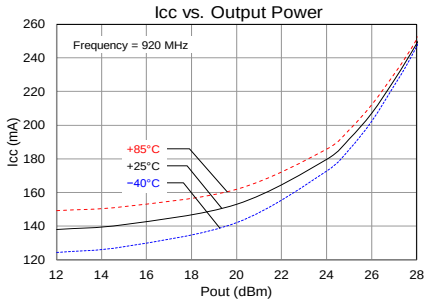




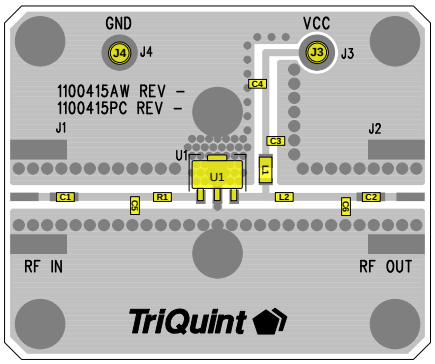


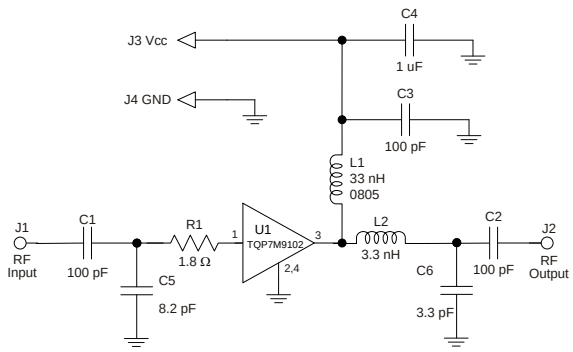






700 – 1000 MHz Evaluation Board (TQP7M9102−PCB900)





Notes:

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2. Components shown on the silkscreen but not on the schematic are not used.
3. The recommended component values are dependent upon the frequency of operation.
4. All components are of 0603 size unless stated on the schematic.
5. Critical component placement locations:
   Distance from U1 Pin 1 (left edge) to R1 (right edge): 90 mils (4.3 deg. at 920 MHz)
   Distance from R1 (left edge) to C5 (right edge): 70 mils (3.3 deg. at 920 MHz)
   Distance from U1 Pin 3 (right edge) to L2 (left edge): 120 mils (5.7 deg. at 920 MHz)
   Distance from U1 Pin 3 (right edge) to C6 (left edge): 370 mils (17.6 deg. at 920 MHz)

Bill of Material TQP7M9102−PCB900

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	TQP7M9102 Amplifier, SOT-89 pkg.	Qorvo	TQP7M9102
R1	1.8 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
L2	3.3 nH	Inductor, 0603, ±0.3 nH	Toko	LL1608-FSL3N3S
L1	33 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-330XJLB
C5	8.2 pF	Cap., Chip, 0603, ±0.1pF. 200V. NPO/COG	AVX	06032U8R2BAT2A
C6	3.3 pF	Cap., Chip, 0603, ±0.1pF. 200V. NPO/COG	AVX	06032U3R3BAT2A
C1, C2, C3	100 pF	Cap., Chip, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	

Typical Performance TQP7M9102−PCB900

Test conditions unless otherwise noted: V_{CC}=+5V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

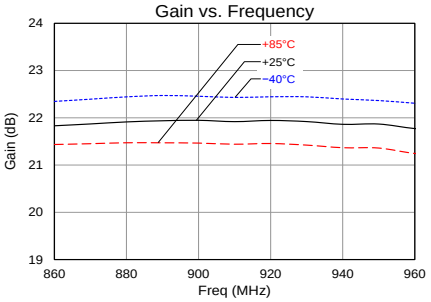
Parameter	Conditions	Typical Value			Units
Frequency		869	920	960	MHz
Gain		21.8	21.9	21.7	dB
Input Return Loss		10	16	17	dB
Output Return Loss		12	10	9	dB
Output P1dB		+27.3	+27.4	+27.4	dBm
OIP3	Pout= +19 dBm/tone, Δf=1 MHz	+42.7	+43.4	+43.9	dBm
WCDMA Channel Power[1]	−50 dBc ACLR	+18.0	+18.2	+18.1	dBm
Noise Figure		5.9	5.9	5.9	dB

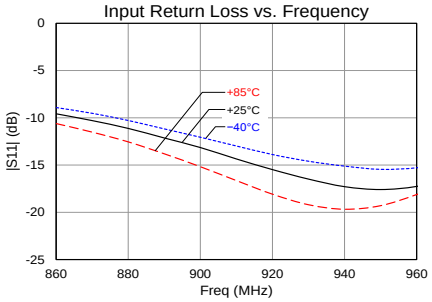
Notes:

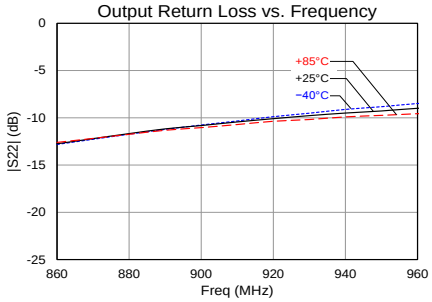
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

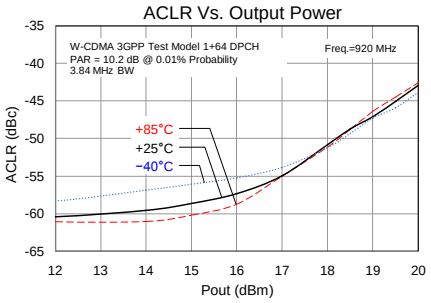
Performance Plots TQP7M9102−PCB900

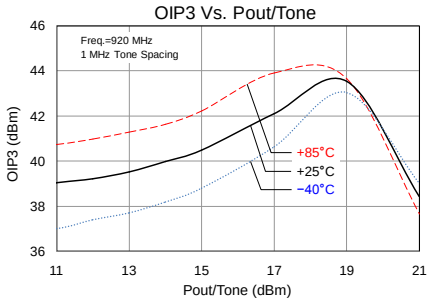
Test conditions unless otherwise noted: V_{CC}=+5V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

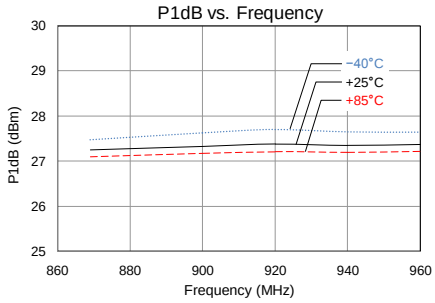


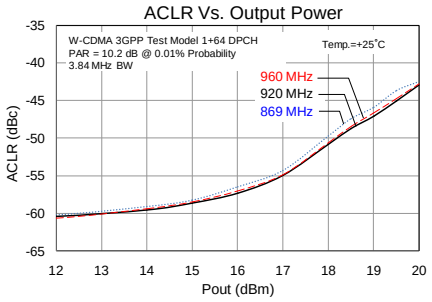


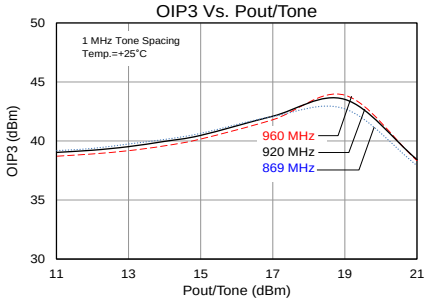


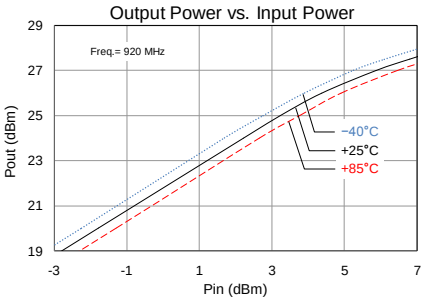


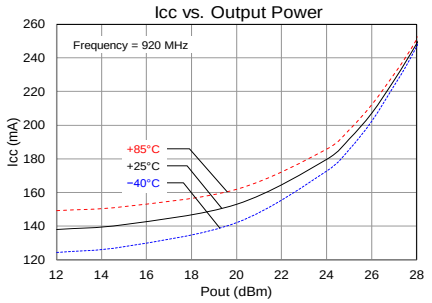




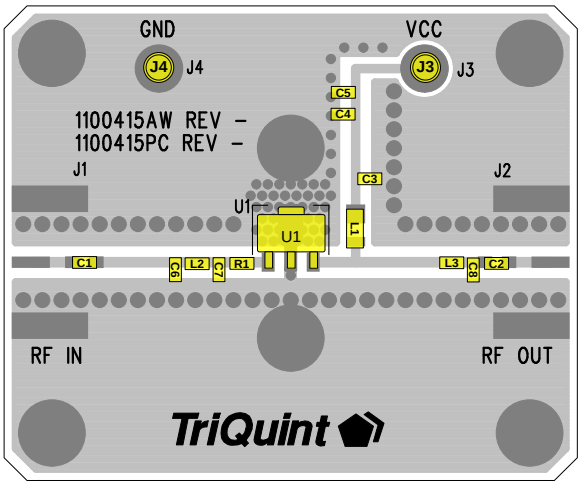


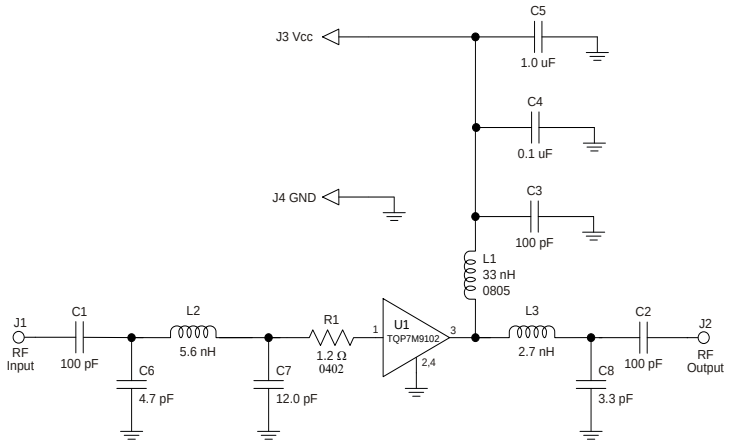






700 – 1000 MHz Reference Design





Notes:

1. The recommended component values are dependent upon the frequency of operation.
2. All components are of 0603 size unless stated on the schematic.
3. Entire Bias network values are critical of linearity performance.
4. Critical component placement locations:
   - Distance from U1 Pin 1 (left edge) to R1 (right edge): 10 mils (0.5 deg at 920 MHz)
   - Distance from R1 (left edge) to C7 (right edge): 10 mils (0.5 deg at 920 MHz)
   - Distance from C7 (left edge) to L2 (right edge): 10 mils (0.5 deg at 920 MHz)
   - Distance from L2 (left edge) to C6 (right edge): 20 mils (1.0 deg at 920 MHz)
   - Distance from U1 Pin 3 (right edge) to L3 (left edge): 290 mils (13.8 deg at 920 MHz)
   - Distance from L3 (right edge) to C8 (left edge): 20 mils (1.0 deg at 920 MHz)

Bill of Material 700 – 1000 MHz Reference Design

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	½ W High Linearity Amplifier	Qorvo	TQP7M9102
C1,C2,C3	100 pF	0603, 5%, 50 V, NPO/COG	various	
C4	0.1 µF	0603, 10%, 50 V, X7R	various	
C5	1.0 µF	0603. 10%, 10 V, X5R	Various	LL-1608-FSL1N2S
L1	33 nH	0805, 5%, cer core,0805 Coilcraft	Coilcraft	0805CS-33XJL
L2	5.6 nH	0603, ± 0.3 nH, multilayer, Toko	Toko	LL1608-FSL5N6S
L3	2.7 nH	0603, ± 0.3 nH, multilayer, Toko	Toko	LL1608-FSL2N7S
C6	4.7 pF	0603, ± 0.1 pF, 200 V, NPO/COG, AVX U Series	AVX	06032U4R7BAT2A
C7	12 pF	0603, 2%, 50 V, NPO/COG	Various	
C8	3.3 pF	0603, ± 0.1 pF, 200 V, NPO/COG, AVX U Series	AVX	06032U3R3BAT2A

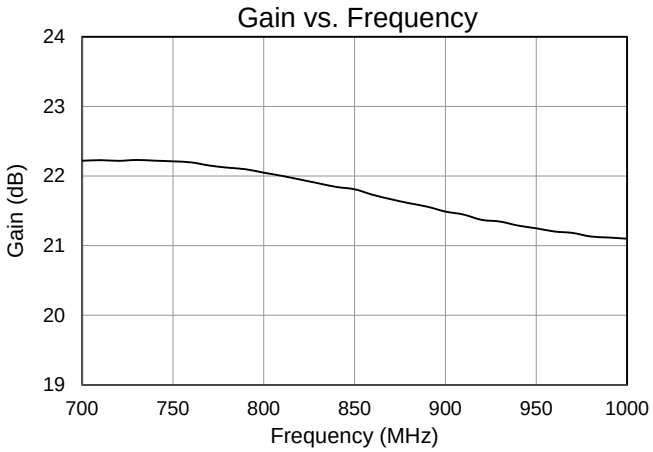
Typical Performance 700 – 1000 MHz Reference Design

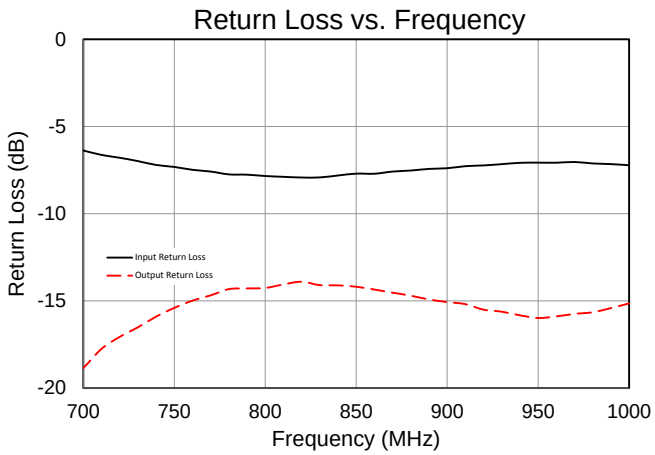
Test conditions unless otherwise noted: V_{CC} = +5 V, I_{CQ}=135 mA , Temp = +25 °C, 50 Ω system

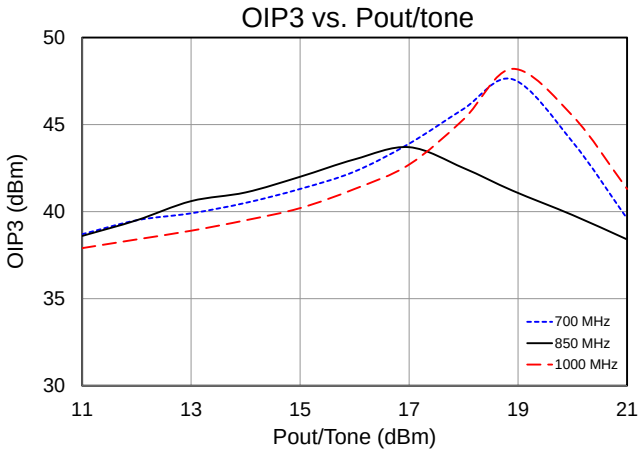
Parameter	Conditions	Typical Value			Units
Frequency		700	850	1000	MHz
Gain		22.2	21.8	21.1	dB
Input Return Loss		6.3	7.7	7.2	dB
Output Return Loss		18.8	14.2	15.2	dB
Output P1dB		+27.4	+28	+28.3	dBm
Output IP3	Pout= +16 dBm / tone, Δf= 1 MHz	+42.3	+43	+41.3	dBm

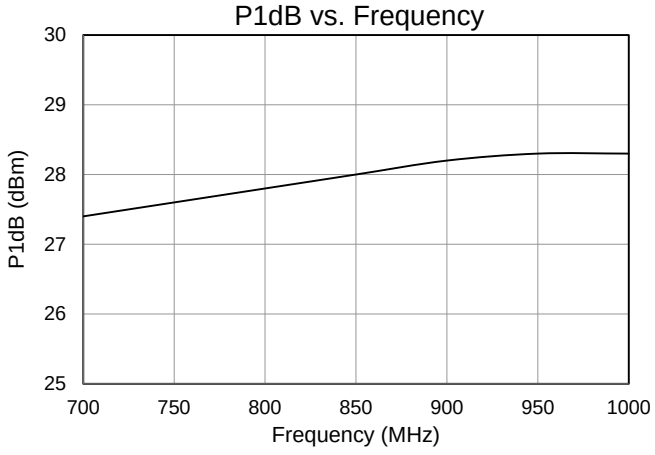
Performance Plots 700 – 1000 MHz Reference Design

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

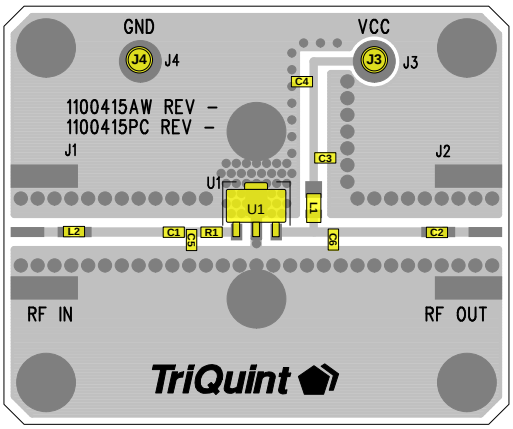


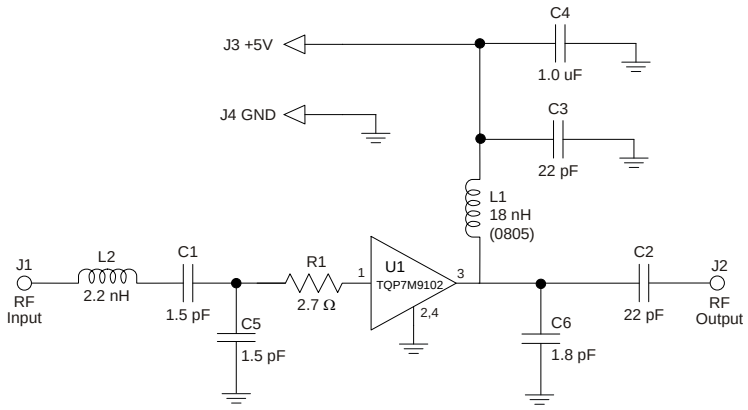






1800 – 2200 MHz 1 Watt Reference Design





Notes:

1. See Evaluation Board PCB Information for material and stack up.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω resistors (R2) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:
   - Distance from U1 Pin 1 (left edge) to R1 (right edge): 25 mils
   - Distance from U1 Pin 1 (left edge) to C1 (right edge): 145 mils
   - Distance from U1 Pin 1 (left edge) to C5 (right edge): 90 mils
   - Distance from U1 Pin 3 (right edge) to C6 (left edge): 145 mils

Bill of Material 1800 – 2200 MHz 1 Watt Reference Design

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	½ W High Linearity Amplifier	Qorvo	TQP7M9102
C2 , C3	22 pF	CAP, 0603, +/-1%. 200V NPO/COG	various	
C1, C5	1.5 pF	CAP, 0603, +/-0.1pF. 200V. NPO/COG	various	
L2	2.2 nH	Ind, chip, 0603, +/-0.3nH >6000MHz	Toko	LL-1608-FSL1N2S
C4	1.0 uF	CAP, 0603, 10%, X5R , 10V	various	
L1	18 nH	IND, 0805, 5%, Ceramic	Coilcraft	0805CS-181XJL
C6	1.8pF	CAP, 0603, +/-0.1pF. 200V. NPO/COG	various	
R1	2.7 Ω	RES, 0603, 5%	various	

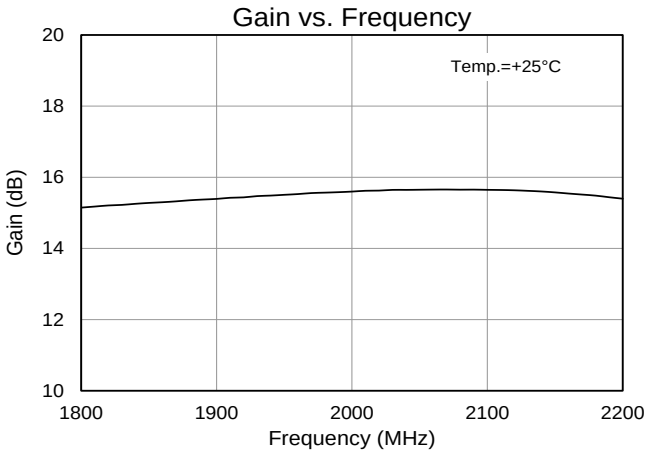
Typical Performance 1800 – 2200 MHz 1 Watt Reference Design

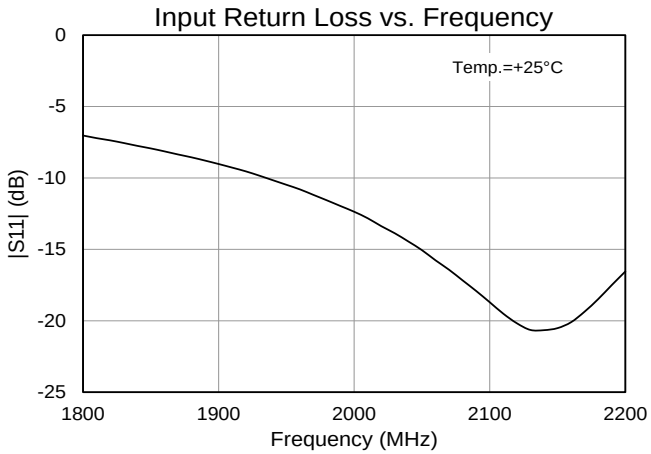
Test conditions unless otherwise noted: V_{CC} =+5V, I_{CQ}=137 mA (typ.), Temp= +25°C

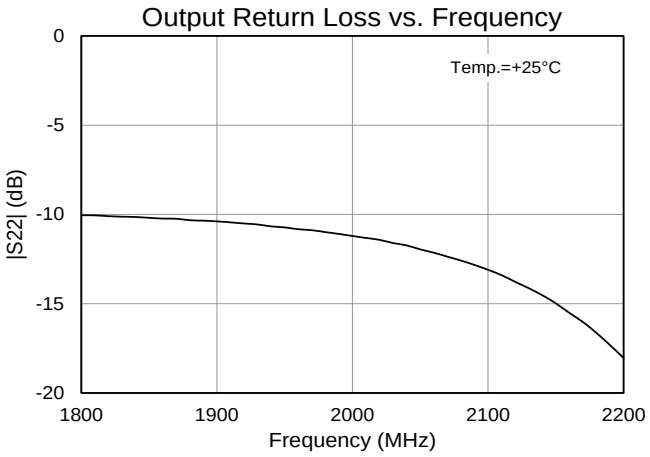
Parameter	Conditions	Typical Value			Units
Frequency		1800	2000	2200	MHz
Gain		15.3	15.5	15.4	dB
Input Return Loss		7.5	8	9	dB
Output Return Loss		7	8	8	dB
Output P1dB		+29.7	+30.7	+29.9	dBm
Output IP3	Pout= +15 dBm/tone, Δf= 1 MHz	+38	+38	+38	dBm

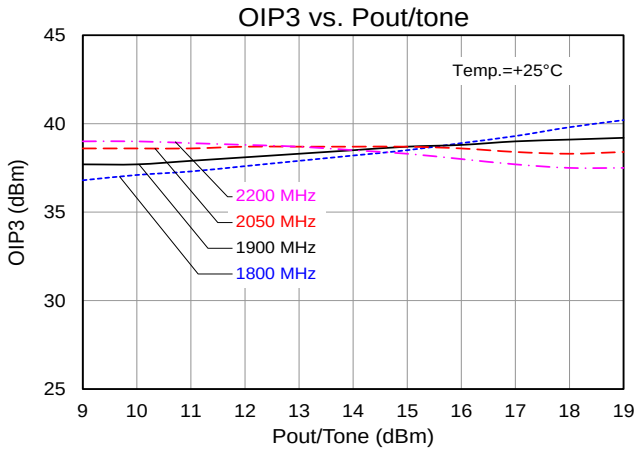
Performance Plots 1800 – 2200 MHz 1 Watt Reference Design

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

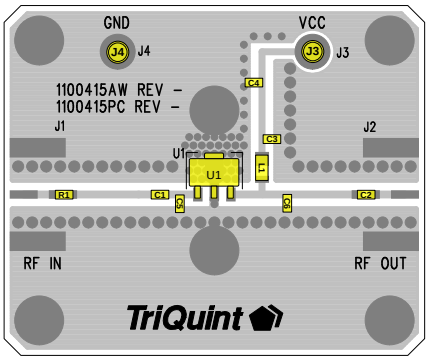


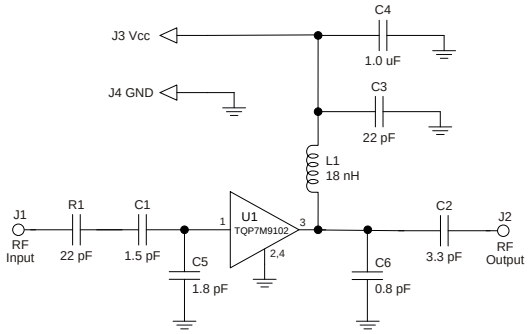






2110 – 2170 MHz Evaluation Board (TQP7M9102−PCB2140)





Notes:
1. See Evaluation Board PCB Information for material and stack up.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The recommended component values are dependent upon the frequency of operation.
4. All components are of 0603 size unless stated on the schematic.
5. Critical component placement locations:
   - Distance from U1 Pin 1 (left edge) to C5 (right edge): 35 mils (3.9 deg. at 2140 MHz)
   - Distance from U1 Pin 1 (left edge) to C1 (right edge): 90 mils (9.9 deg. at 2140 MHz)
   - Distance from U1 Pin 3 (right edge) to C6 (left edge): 210 mils (23.2 deg. at 2140 MHz)

Bill of Material TQP7M9102−PCB2140

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	TQP7M9102 Amplifier, SOT-89 pkg.	Qorvo	TQP7M9102
R1	39 pF	Cap., Chip, 0603, +/-1%. 200V NPO/COG	various	
L1	18 nH	Inductor, 0805, Coilcraft CS Series	Coilcraft	0805CS-180XJLB
C1	1.5 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	various	06032U1R5BAT2A
C2	3.3 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	various	06032U3R3BAT2A
C3	22 pF	Cap., Chip, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	
C5	1.8 pF	Cap., Chip, 0603, +/-0.1pF. 200V. NPO/COG	various	06032U1R8BAT2A
C6	0.8 pF	Cap., Chip, 0603, +/-0.05pF, 50V	various	06032U0R8BAT2A

Typical Performance TQP7M9102−PCB2140

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp=+25 °C

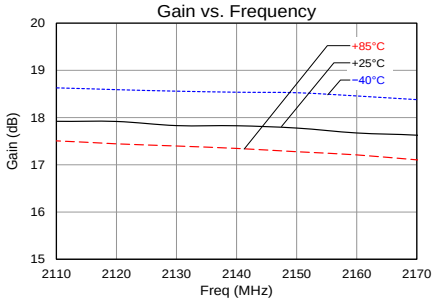
Parameter	Conditions	Typical Value			Units
Frequency		2110	2140	2170	MHz
Gain		17.9	17.8	17.7	dB
Input Return Loss		12	12	11	dB
Output Return Loss		12	11	10	dB
Output P1dB		+27.8	+27.6	+27.4	dBm
OIP3	Pout= +9 dBm/tone, Δf=1 MHz	+43.6	+43.5	+43.6	dBm
WCDMA Channel Power(1)	−50 dBc ACLR	+18.5	+18.4	+18.3	dBm
Noise Figure		3.8	3.9	4.0	dB

Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob

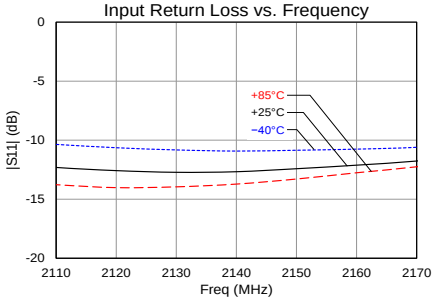
Performance Plots TQP7M9102−PCB2140

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

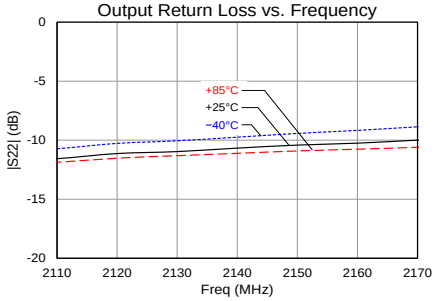
Gain vs. Frequency



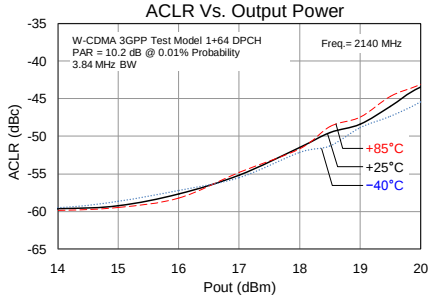
Input Return Loss vs. Frequency



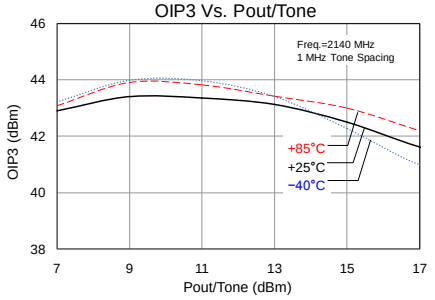
Output Return Loss vs. Frequency



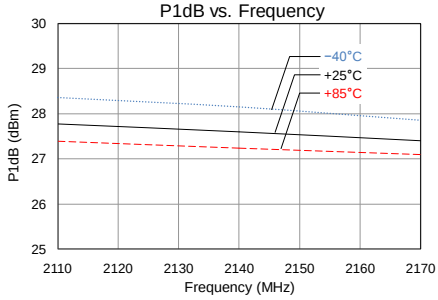
ACLR Vs. Output Power



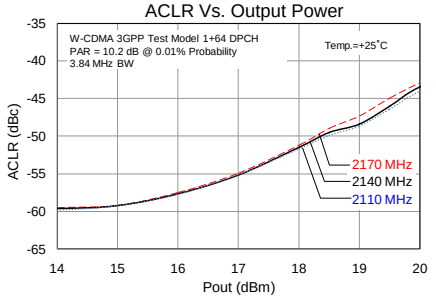
OIP3 Vs. Pout/Tone



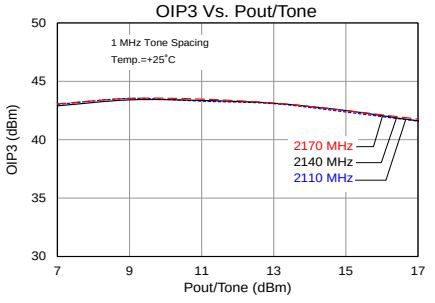
P1dB vs. Frequency



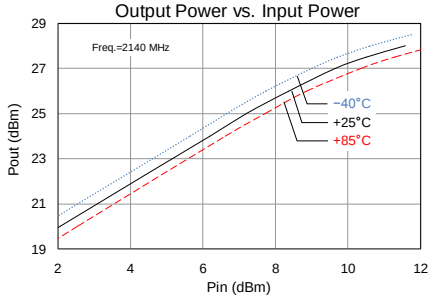
ACLR Vs. Output Power



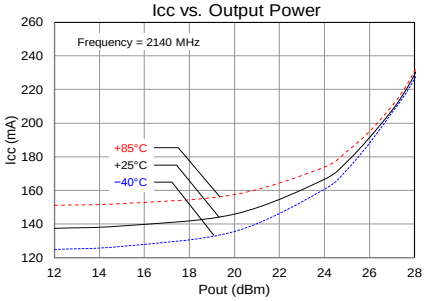
OIP3 Vs. Pout/Tone



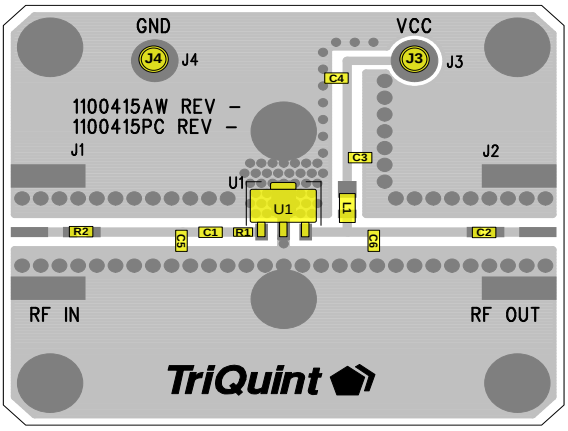
Output Power vs. Input Power

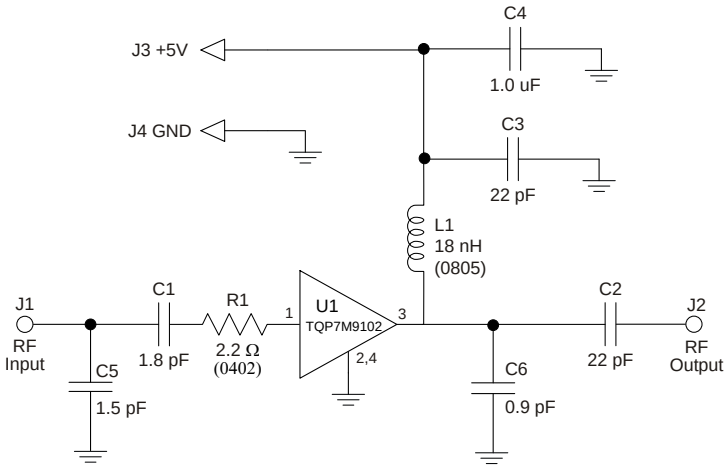


Icc vs. Output Power



2300 – 2700 MHz Reference Design





Notes:

1. See Evaluation Board PCB Information for material and stack up.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω resistors (R2) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:
   - Distance from U1 Pin 1 (left edge) to R1 (right edge): 10 mils
   - Distance from U1 Pin 1 (left edge) to C1 (right edge): 80 mils
   - Distance from U1 Pin 1 (left edge) to C5 (right edge): 235 mils
   - Distance from U1 Pin 3 (right edge) to C6 (left edge): 165 mils

Bill of Material 2300 – 2700 Reference Design

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	½ W High Linearity Amplifier	Qorvo	TQP7M9102
C1	1.8 pF	CAP, 0603, ± 0.05 pF, 50V, ACCU-P	AVX	06035J1R8ABSTR
C5	1.5 pF	CAP, 0603, ± 0.05 pF, 50V, ACCU-P	AVX	06035J1R5ABSTR
C2, C3	22 pF	CAP, 0603, 5%, 50V, NPO/COG	various	
C4	1.0 uF	CAP, 0603, 10%, X5R , 10V	various	
C6	0.9 pF	CAP, 0603	AVX	06035J0R9ABSTR
R1	2.2 Ω	RES, 0402	various	
R2	0 Ω	RES, 0603, 5%, 1/16W, Chip	various	
L1	18 nH	IND, 0805, 5%, Ceramic	Coilcraft	0805CS-180XJL

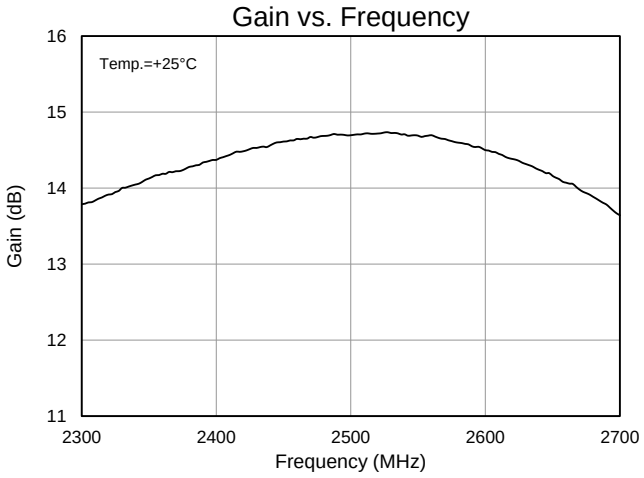
Typical Performance 2300 – 2700 Reference Design

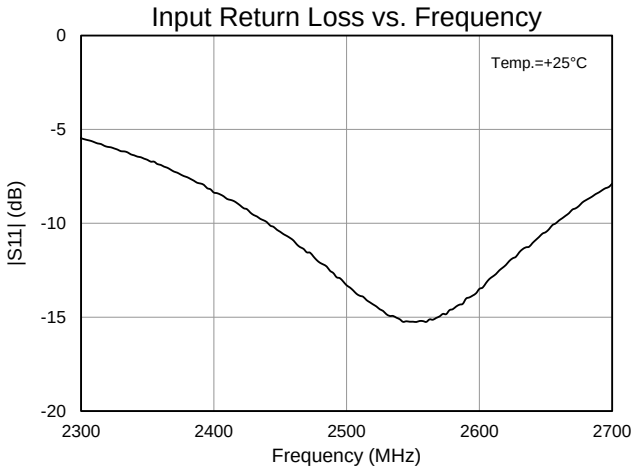
Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp=+25 °C

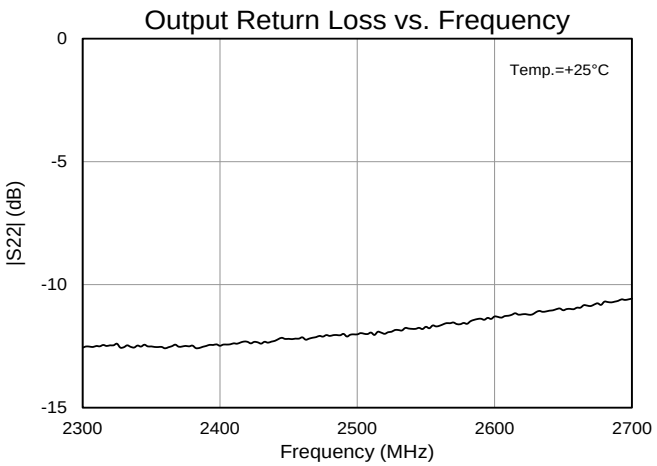
Parameter	Conditions	Typical Value			Units
Frequency		2300	2500	2700	MHz
Gain		13.8	14.7	13.6	dB
Input Return Loss		5.5	13.3	7.9	dB
Output Return Loss		12.6	12	10.6	dB
Output P1dB		+27.7	+27.8	+27.1	dBm
OIP3	Pout= +9 dBm / Tone, Δf = 1 MHz	+43.8	+44.0	+45.9	dBm

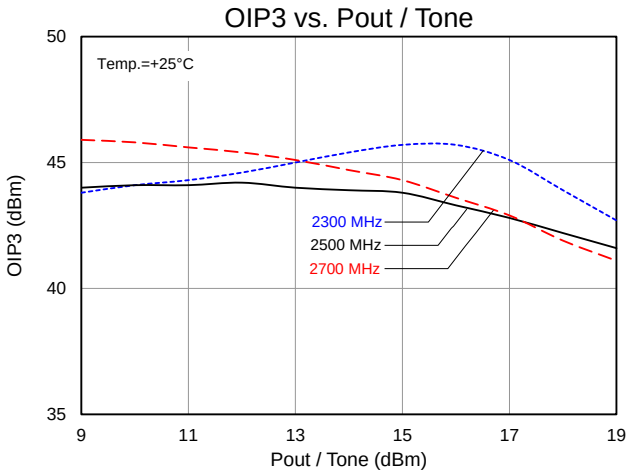
Performance Plots 2300 – 2700 Reference Design

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

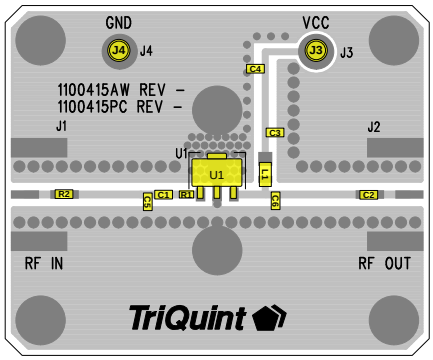


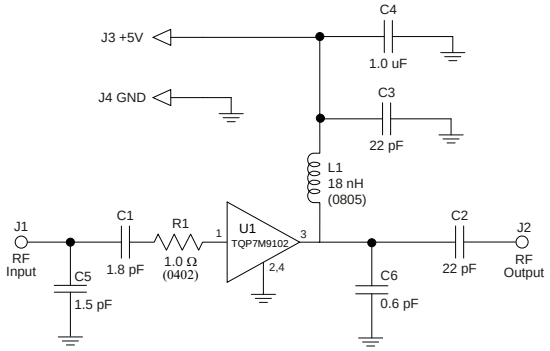






2.5 – 2.7 GHz Evaluation Board (TQP7M9102−PCB2600)





Notes:

1. See Evaluation Board PCB Information for material and stack up.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω resistors (R2) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.
6. Critical component placement locations:
   - Distance from U1 Pin 1 (left edge) to R1 (right edge): 13 mils
   - Distance from U1 Pin 1 (left edge) to C1 (right edge): 70 mils
   - Distance from U1 Pin 1 (left edge) to C5 (right edge): 148 mils
   - Distance from U1 Pin 3 (right edge) to C6 (left edge): 78 mils

Bill of Material TQP7M9102−PCB2600

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	½ W High Linearity Amplifier	Qorvo	TQP7M9102
C1	1.8 pF	CAP, 0603, ± 0.05 pF, 50V, ACCU-P	AVX	06035J1R8ABSTR
C5	1.5 pF	CAP, 0603, ± 0.05 pF, 50V, ACCU-P	AVX	06035J1R5ABSTR
C2, C3	22 pF	CAP, 0603, 5%, 50V, NPO/COG	various	
C4	1.0 uF	CAP, 0603, 10%, X5R , 10V	various	
C6	0.6 pF	CAP, 0603, ± 0.05 pF, 50V, ACCU-P	AVX	06035J0R6ABSTR
R1	1.0 Ω	RES, 0402, 1%, 1/16W. CHIP.	various	
R2	0 Ω	RES, 0603, 5%, 1/16W, Chip	various	
L1	18 nH	IND, 0805, 5%, Ceramic	Coilcraft	0805CS-180XJL

Typical Performance TQP7M9102−PCB2600

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

Parameter	Conditions	Typical Value			Units
Frequency		2500	2600	2700	MHz
Gain		14.3	14.5	14.1	dB
Input Return Loss		8.5	14.5	12	dB
Output Return Loss		8.5	8	7.5	dB
Output P1dB		+28.0	+28.0	+28.0	dBm
OIP3	Pout= +11 dBm/tone, Δf=1 MHz	+44.0	+43.7	+43.0	dBm
WCDMA Channel Power(1)	−50 dBc ACLR	+17.5	+17.5	+17.5	dBm

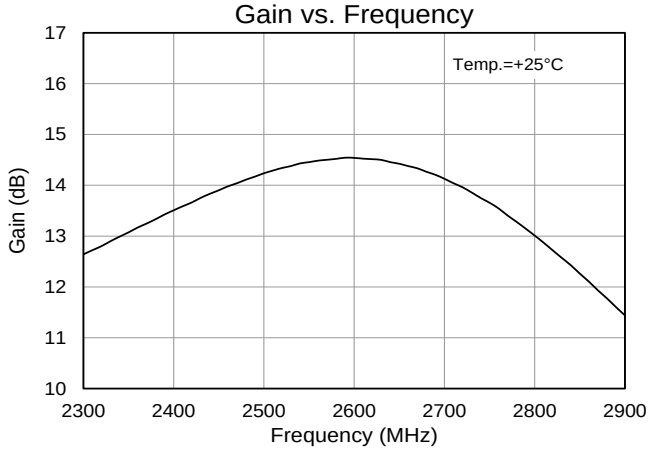
Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob.

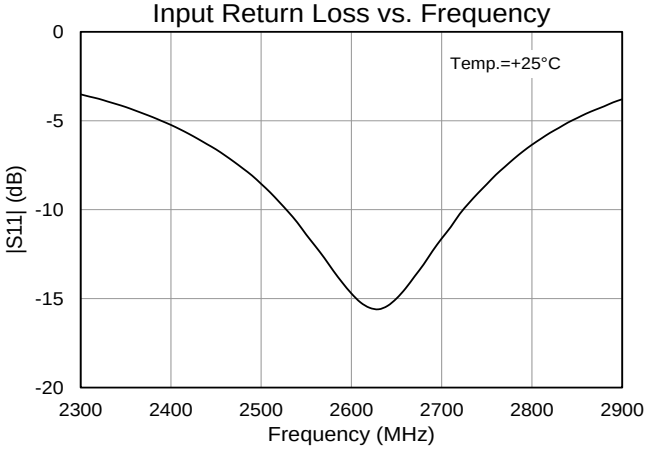
Performance Plots TQP7M9102−PCB2600

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp.=+25 °C

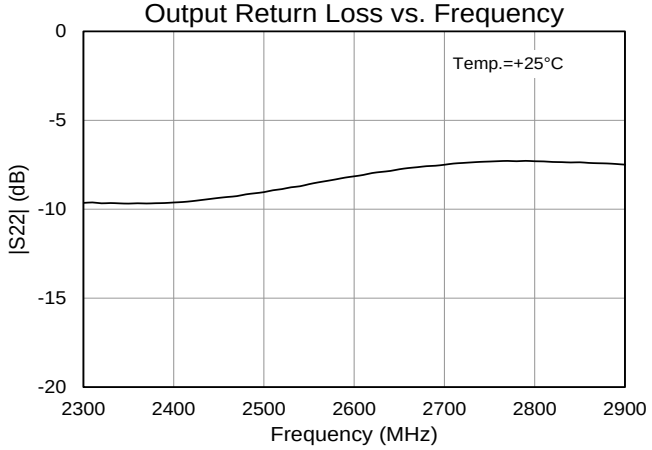
Gain vs. Frequency



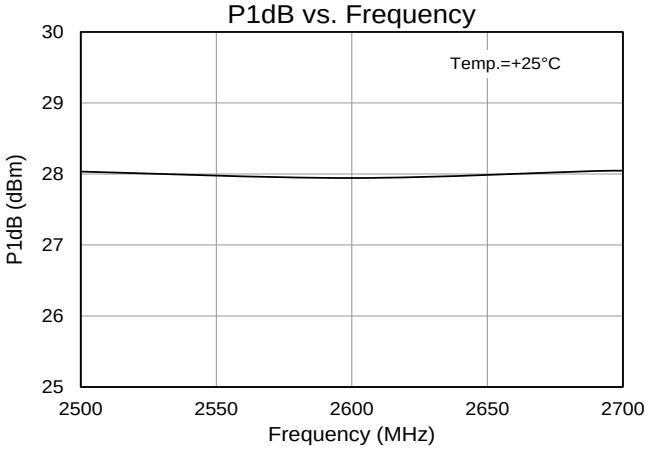
Input Return Loss vs. Frequency



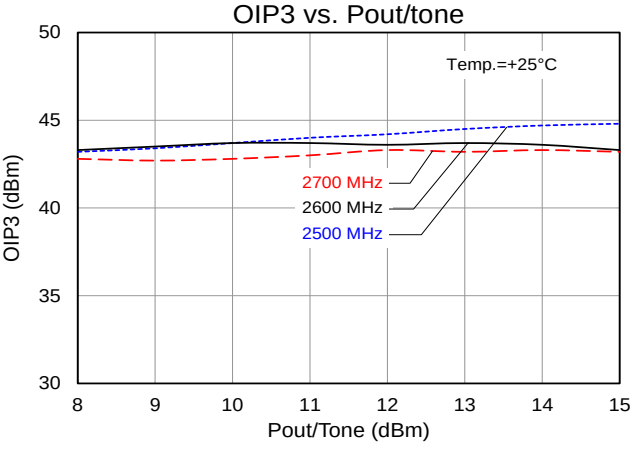
Output Return Loss vs. Frequency



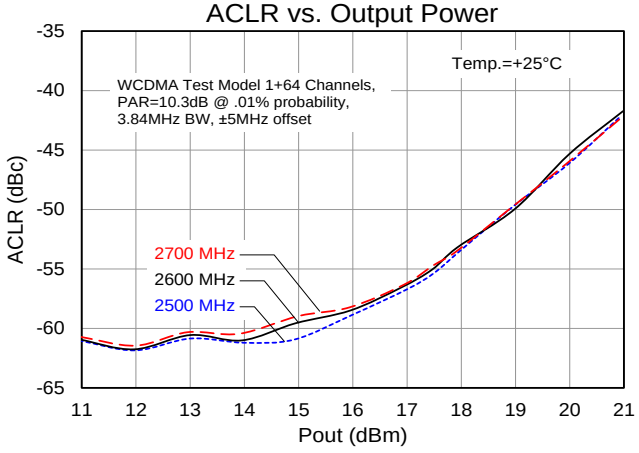
P1dB vs. Frequency



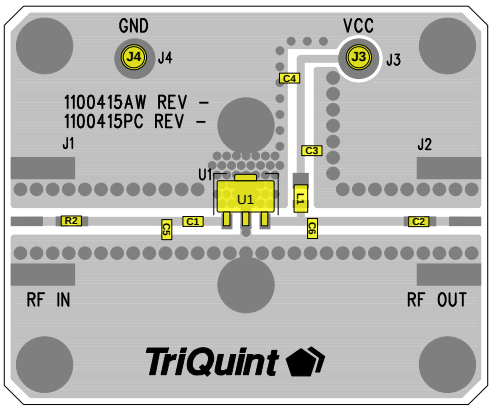
OIP3 vs. Pout/tone

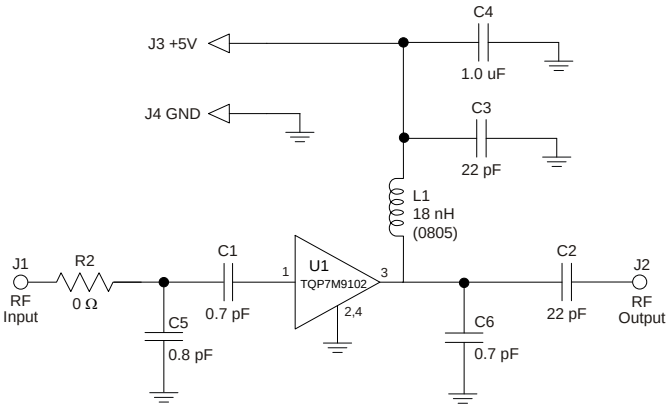


ACLR vs. Output Power



3400 – 3600 MHz Reference Design





Notes:

7. See Evaluation Board PCB Information for material and stack up.
8. Components shown on the silkscreen but not on the schematic are not used.
9. 0 Ω resistors (R2) may be replaced with copper trace in the target application layout.
10. The recommended component values are dependent upon the frequency of operation.
11. All components are of 0603 size unless stated on the schematic.
12. Critical component placement locations:
    - Distance from U1 Pin 1 (left edge) to C1 (right edge): 87 mils
    - Distance from U1 Pin 1 (left edge) to C5 (right edge): 210 mils
    - Distance from U1 Pin 3 (right edge) to C6 (left edge): 105 mils

Bill of Material 3400 – 3600 MHz Reference Design

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	0.25 W High Linearity Amplifier	Qorvo	TQP7M9102
R2	0 Ω	RES , 0603, 5PCT. 1/16W. CHIP	various	
C1 , C6	0.7 pF	CAP, 0603, ± 0.1 pF, 50V	various	
C5	0.8 pF	CAP, 0603, ± 0.1 pF, 50V	various	
C2 , C3	22 pF	CAP, 0603, 5%, 50V, NPO/COG	various	
C4	1.0 uF	CAP, 0603, 10%, X5R , 10V	various	
L1	18 nH	Inductor, 0805, 5%, Coilcraft CS series	Coilcraft	0805CS-180XJLB

Typical Performance 3400 – 3600 MHz Reference Design

Test conditions unless otherwise noted: V_{CC}=+5V, I_{CQ}=137 mA (typ.), Temp.=+25°C

Parameter	Conditions	Typical Value			Units
Frequency		3400	3500	3600	MHz
Gain		14.2	14.5	13.8	dB
Input Return Loss		9	17	9	dB
Output Return Loss		15	11	8	dB
Output P1dB		+27.1	+26.7	+26.2	dBm
OIP3	Pout= +11 dBm/tone, Δf=1 MHz	+43.3	+44.6	+44.6	dBm
WCDMA Channel Power(1)	−50 dBc ACLR	+18.0	+17.5	+17.0	dBm

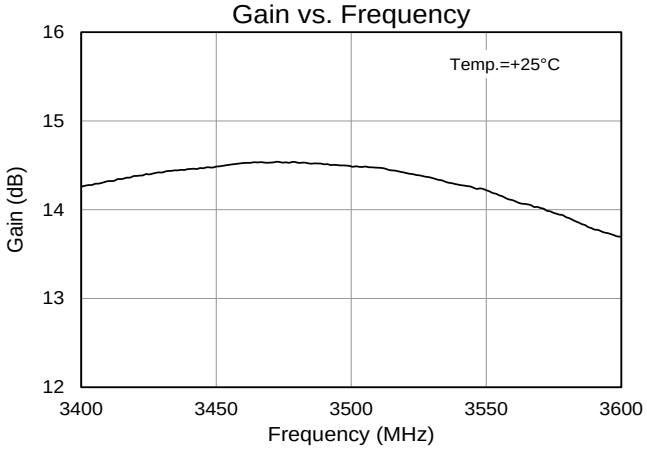
Notes:

1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob

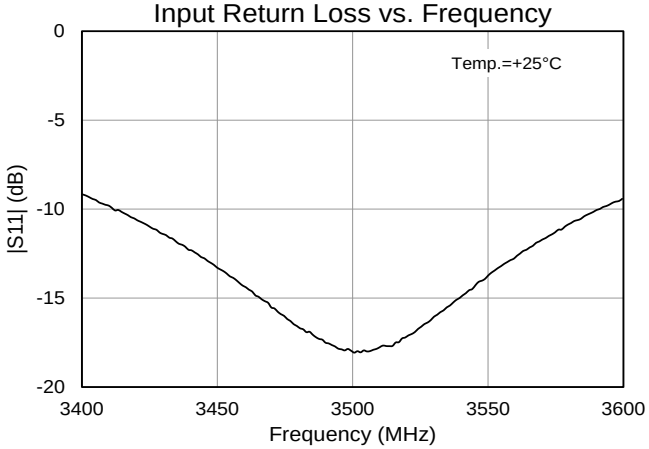
Performance Plots 3400 – 3600 MHz Reference Design

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp=+25°C

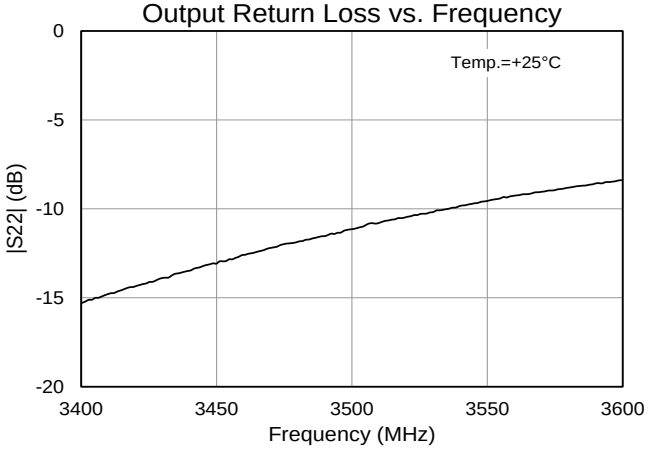
Gain vs. Frequency



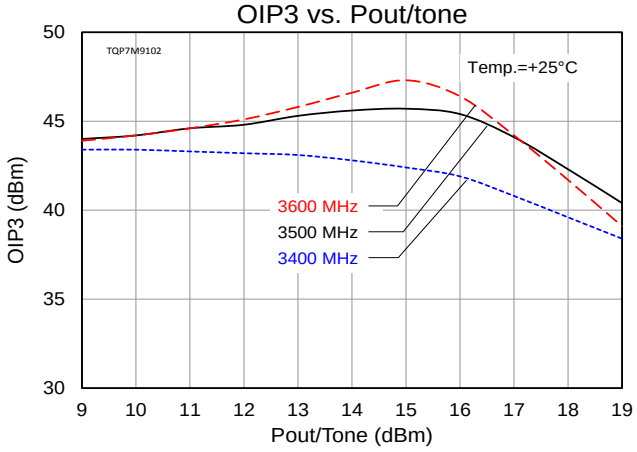
Input Return Loss vs. Frequency



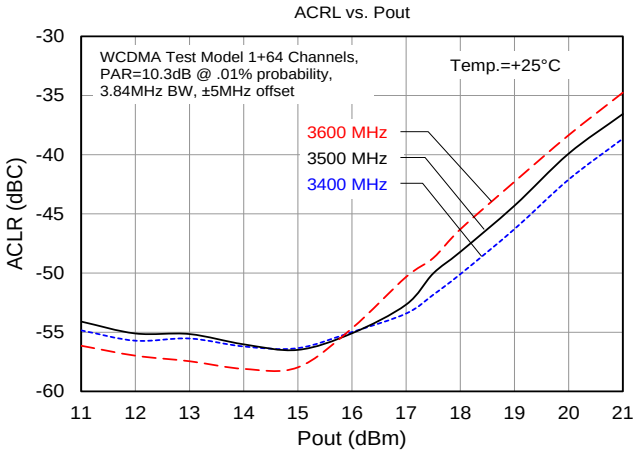
Output Return Loss vs. Frequency



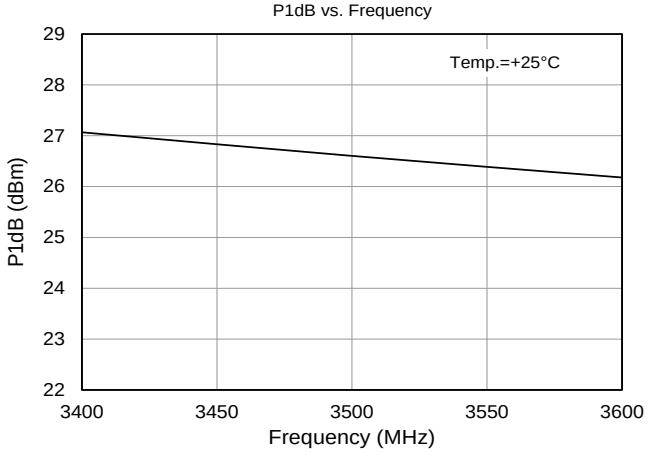
OIP3 vs. Pout/tone



ACRL vs. Pout



P1dB vs. Frequency

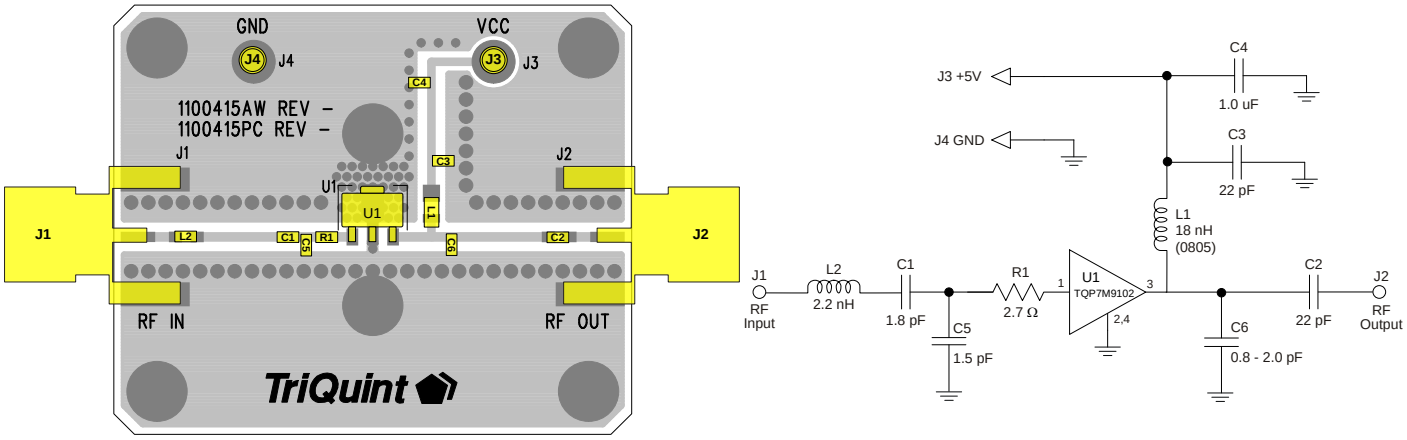


Application Note 1.8-2.2 GHz (1/2 Watt - 1 Watt) Tunable Reference Design

This applications note describes the ability to take the TQP7M9102 1.8-2.2 GHz design and tune it from 1/2 Watt to 1 Watt simply by changing the output match (one component). By use of Load-Pull data we were able to see the capability of this part to be tuned from +27 dBm P1dB to +30 dBm by trading off OIP3 performance. This gives the end user the option to run the TQP7M9102 as a 1 Watt device over a wide frequency band.

Below are the different Reference Design options which show the performance trade-offs between P1dB and OIP3 by changing the value and placement of C6.

Evaluation Board



Notes:

1. All components are of 0603 size unless stated on the schematic.
2. The recommended component values are dependent upon the frequency of operation.
3. Critical component placement locations:
   - Distance between U1 Pin 1 Pad to R1 (right edge): 10 mil
   - Distance between U1 Pin 1 Pad to C1 (right edge): 110 mil
   - Distance between U1 Pin 1 Pad to C5 (right edge): 65 mil
   - Distance between U1 Pin 3 Pad to C6 (left edge): see below:

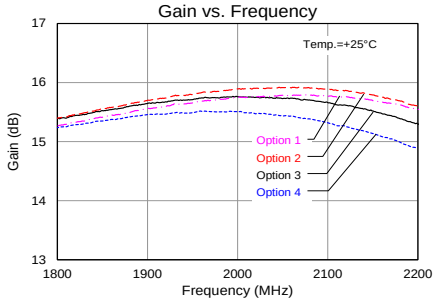
Component Placement

Option	P1dB	C6 Value (pF)	Line Length (mils)	Electrical Length at 2 GHz (degrees)
1	30.0	2.0	145	15.0
2	29.0	1.8	170	17.6
3	28.0	1.2	230	23.8
4	27.0	0.8	290	30.0

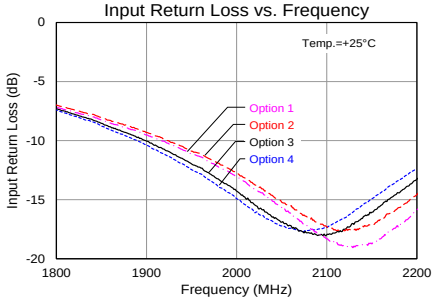
Performance Plots 1.8-2.2 GHz (1/2 Watt - 1 Watt) Tunable Reference Design

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}=137 mA (typ.), Temp=+25°C

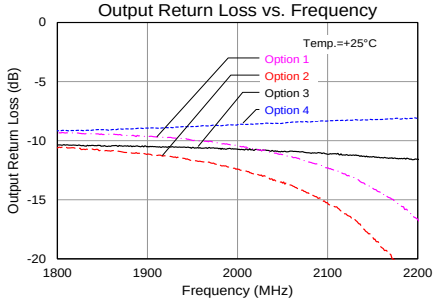
Gain vs. Frequency



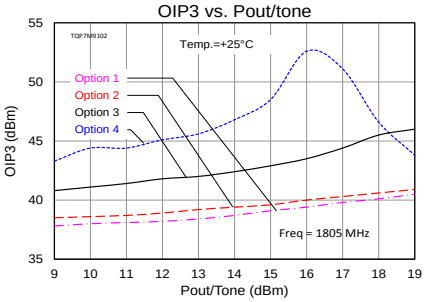
Input Return Loss vs. Frequency



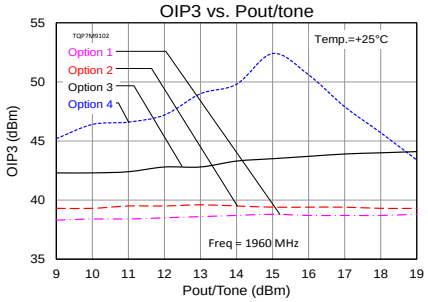
Output Return Loss vs. Frequency



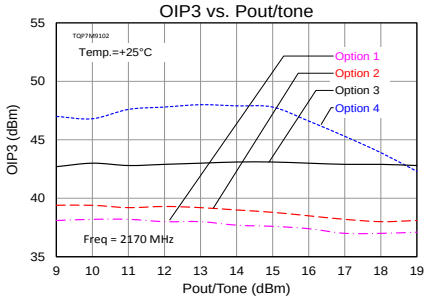
OIP3 vs. Pout/tone



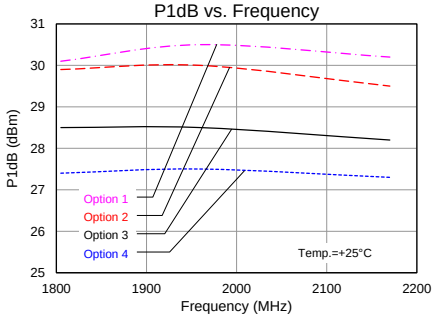
OIP3 vs. Pout/tone



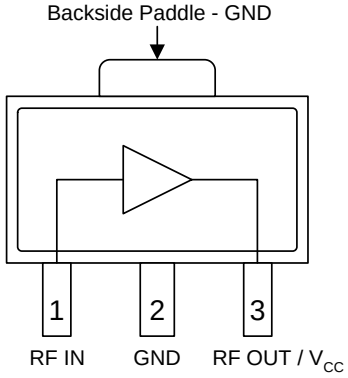
OIP3 vs. Pout/tone



P1dB vs. Frequency



Pin Configuration and Description



Pin No.	Label	Description
1	RF IN	RF input. External DC Block required. Requires conjugate match for optimal performance.
2, Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.
3	RF OUT / V_{CC}	RF output, matched to 50 ohms. External DC Block and bias voltage required.

Evaluation Board PCB Information

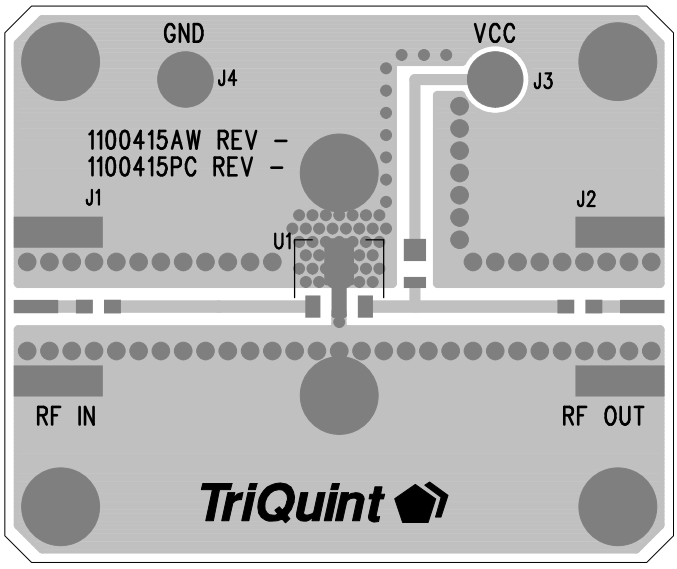
PC Board Layout

PCB Material (stackup):

1 oz. Cu top layer
0.014 inch Nelco N-4000-13, ε_r=3.7
1 oz. Cu MIDDLE layer 1
Core Nelco N-4000-13
1 oz. Cu middle layer 2
0.014 inch Nelco N-4000-13
1 oz. Cu bottom layer
Finished board thickness is 0.062±.006

50 ohm line dimensions: width = .028”, spacing = .028”.

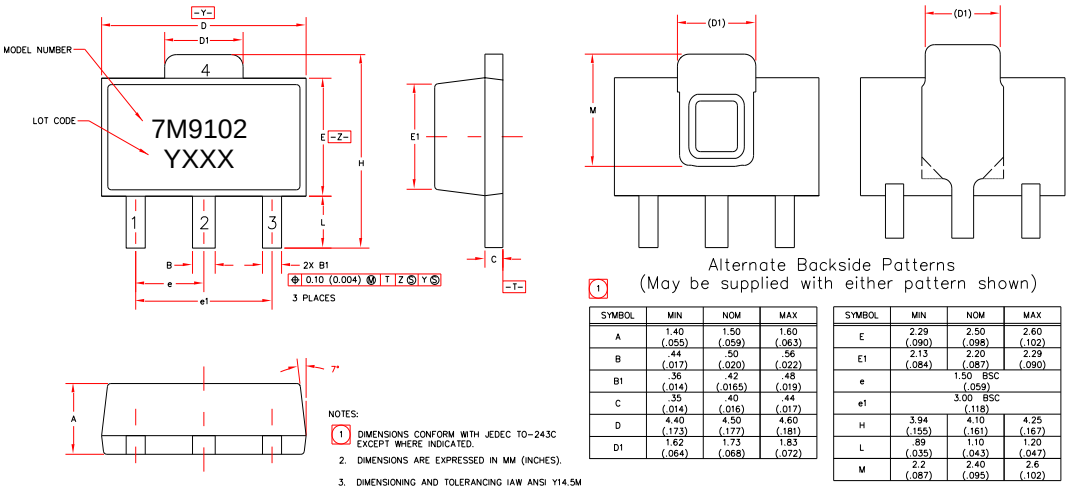
The pad pattern shown has been developed and tested for optimized assembly at Triquint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.



Package Marking and Dimensions

Package Marking

Product ID:
7M9102
Lot code:
YXXX

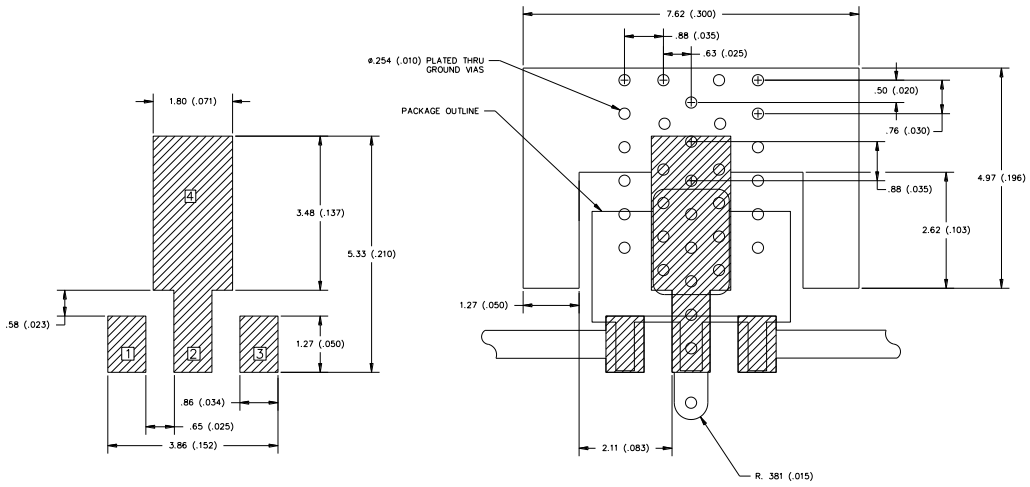


SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e		1.50 BSC (.059)	
e1		3.00 BSC (.118)	
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Contact plating: NiPdAu

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
6. Ensure good package backside paddle solder attach for best electrical and thermal performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 2
Value: ≥2000V to <4000V
Test: Human Body Model (HBM)
Standard: ESAD/JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.triquint.com **Tel: 877-800-8584**
Email: customer.support@qorvo.com

For information about the merger of RFMD and TriQuint as Qorvo:

Web: www.qorvo.com

For technical questions and application information:

Email: sjcapplications.engineering@qorvo.com

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