TS4994

1W Differential Input/Output Audio Power Amplifier with Selectable Standby

- **Differential inputs**
- **Near zero pop & click**
- **100dB PSRR @ 217Hz with grounded inputs**
- **Operating from V_{CC} = 2.5V to 5.5V**
- **1W RAIL to RAIL output power @ Vcc=5V, THD=1%, F=1kHz, with 8Ω load**
- **90dB CMRR @ 217Hz**
- **Ultra-low consumption in standby mode (10nA)**
- **Selectable standby mode (active low or active high**
- **Ultra fast startup time: 15ms typ.**
- **Available in DFN10 3x3, 0.5mm pitch & MiniSO8**
- **All lead-free packages**

Description

The TS4994 is an audio power amplifier capable of delivering 1W of continuous RMS output power into an 8Ω load @ 5V. Thanks to its differential inputs, it exhibits outstanding noise immunity.

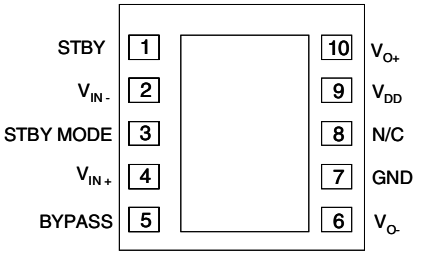
An external standby mode control reduces the supply current to less than 10nA. A STBY MODE pin allows the standby pin to be active HIGH or LOW (except in the MiniSO8 version). An internal thermal shutdown protection is also provided, making the device capable of sustaining short-circuits.

The device is equipped with Common Mode Feedback circuitry allowing outputs to be always biased at Vcc/2 regardless of the input common mode voltage.

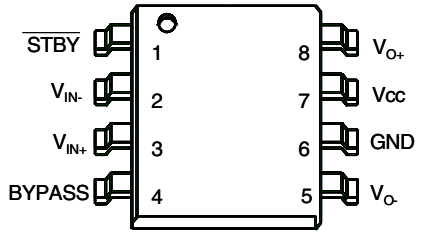
The TS4994 has been designed for high quality audio applications such as mobile phones and requires few external components.

Pin Connections (top view)

TS4994IQT - DFN10



TS4994IST - MiniSO8



Applications

- **Mobile phones (cellular / cordless)**
- **Laptop / notebook computers**
- **PDAs**
- **Portable audio devices**
-
-

Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS4994IQT	-40°C to +85°C	DFN10	Tape & Reel	K994
TS4994IST	-40°C to +85°C	MiniSO8	Tape & Reel	K994

1 Application Component Information

Components	Functional Description
C_S	Supply Bypass capacitor which provides power supply filtering.
C_B	Bypass capacitor which provides half supply filtering.
R_{FEED}	Feedback resistor which sets the closed loop gain in conjunction with R_{IN} A_V= Closed Loop Gain= R_{FEED}/R_{IN}.
R_{IN}	Inverting input resistor which sets the closed loop gain in conjunction with R_{FEED}.
C_{IN}	Optional input capacitor making a high pass filter together with R_{IN}. (fcl = 1 / (2 x Pi x R_{IN} x C_{IN})

Figure 1. Typical Application DFN10 Version

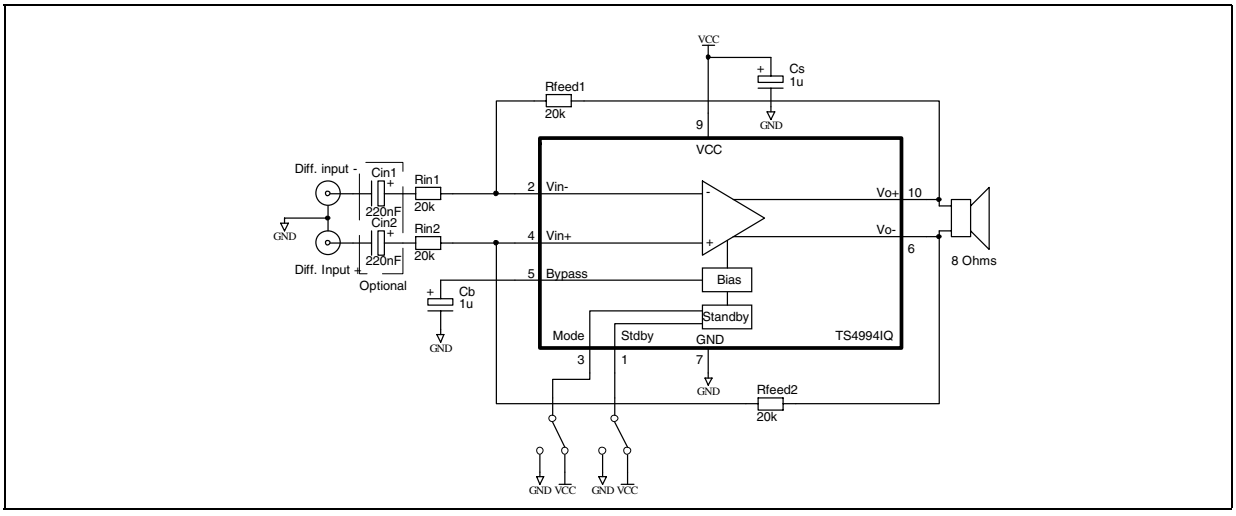
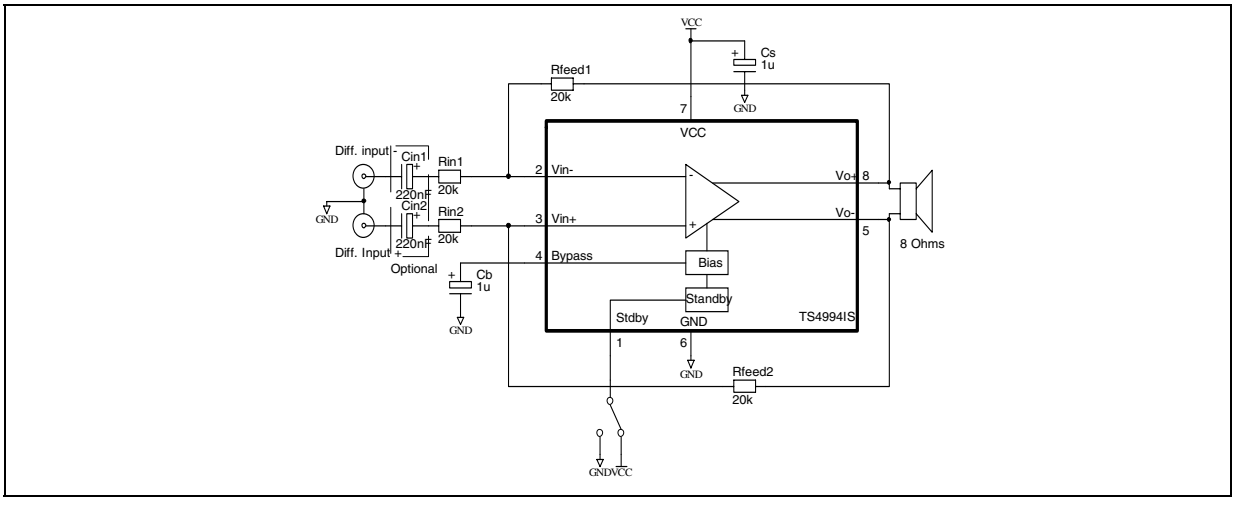


Figure 2. Typical Application Mini-SO8 Version



2 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage [1]	6	V
V_i	Input Voltage [2]	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient [3] DFN10 Mini-SO8	 120 215	°C/W
Pd	Power Dissipation	internally limited	W
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	260	°C

1) All voltages values are measured with respect to the ground pin.

2) The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V

3) The device is protected by a thermal shutdown active at 150°C

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.5 to 5.5	V
V_{SM}	Standby Mode Voltage Input: Standby Active LOW Standby Active HIGH	 V_{SM}=GND V_{SM}=V_{CC}	V
V_{STB}	Standby Voltage Input: Device ON (V_{SM}=GND) or Device OFF (V_{SM}=V_{CC}) Device OFF (V_{SM}=GND) or Device ON (V_{SM}=V_{CC})	 $1.5 \leq V_{STB} \leq V_{CC}$ $G_{ND} \leq V_{STB} \leq 0.4$ [1]	V
T_{SD}	Thermal Shutdown Temperature	150	°C
R_L	Load Resistor	≥ 8	Ω
R_{THJA}	Thermal Resistance Junction to Ambient DFN10 [2] Mini-SO8	 80 190	°C/W

1) The minimum current consumption ($I_{STANDBY}$) is guaranteed when V_{STB}=GND or V_{CC} (i.e. supply rails) for the whole temperature range.

2) When mounted on a 4-layer PCB.

3 Electrical Characteristics

Table 3. Electrical characteristics - V_{CC} = +5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		4	7	mA
$I_{STANDBY}$	Standby Current No input signal, Vstdby = V_{SM} = G_{ND}, RL = 8Ω No input signal, Vstdby = V_{SM} = V_{CC}, RL = 8Ω		10	1000	nA
Voo	Differential Output Offset Voltage No input signal, RL = 8Ω		0.1	10	mV
V_{ICM}	Input Common Mode Voltage CMRR ≤ -60dB	0.6		V_{CC}- 0.9	V
Po	Output Power THD = 1% Max, F= 1kHz, RL = 8Ω	0.8	1		W
THD + N	Total Harmonic Distortion + Noise Po = 850mW rms, Av = 1, 20Hz ≤ F ≤ 20kHz, RL = 8Ω		0.5		%
$PSRR_{IG}$	Power Supply Rejection Ratio with Inputs Grounded[1] F = 217Hz, R = 8Ω, Av = 1, C_{in} = 4.7µF, C_b =1µF Vripple = 200mV_{PP}		100		dB
CMRR	Common Mode Rejection Ratio F = 217Hz, RL = 8Ω, Av = 1, C_{in} = 4.7µF, C_b =1µF Vic = 200mV_{PP}		90		dB
SNR	Signal-to-Noise Ratio (A Weighted Filter, A_v = 2.5) (R_L = 8Ω, THD +N < 0.7%, 20Hz ≤ F ≤ 20kHz)		100		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz
V_N	Output Voltage Noise, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω Unweighted, Av = 1 A weighted, Av = 1 Unweighted, Av = 2.5 A weighted, Av = 2.5 Unweighted, Av = 7.5 A weighted, Av = 7.5 Unweighted, Standby A weighted, Standby		 6 5.5 12 10.5 33 28 1.5 1		μV_{RMS}
T_{WU}	Wake-Up Time[2] C_b =1µF		15		ms

1) Dynamic measurements - 20*log(rms(Vout)/rms (Vripple)). Vripple is the super-imposed sinus signal relative to Vcc.

2) Transition time from standby mode to fully operational amplifier.

Table 4. Electrical Characteristics: V_{CC} = +3.3V (all electrical values are guaranteed with correlation measurements at 2.6V and 5V) GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		3	7	mA
$I_{STANDBY}$	Standby Current No input signal, Vstdby = V_{SM} = G_{ND}, RL = 8Ω No input signal, Vstdby = V_{SM} = V_{CC}, RL = 8Ω		10	1000	nA
Voo	Differential Output Offset Voltage No input signal, RL = 8Ω		0.1	10	mV
V_{ICM}	Input Common Mode Voltage CMRR ≤ -60dB	0.6		V_{CC}- 0.9	V
Po	Output Power THD = 1% Max, F= 1kHz, RL = 8Ω	300	380		mW
THD + N	Total Harmonic Distortion + Noise Po = 300mW rms, Av = 1, 20Hz ≤ F ≤ 20kHz, RL = 8Ω		0.5		%
$PSRR_{IG}$	Power Supply Rejection Ratio with Inputs Grounded[1] F = 217Hz, R = 8Ω, Av = 1, C_{in} = 4.7µF, C_b =1µF Vripple = 200mV_{PP}		100		dB
CMRR	Common Mode Rejection Ratio F = 217Hz, RL = 8Ω, Av = 1, C_{in} = 4.7µF, C_b =1µF Vic = 200mV_{PP}		90		dB
SNR	Signal-to-Noise Ratio (A Weighted Filter, A_v = 2.5) (R_L = 8Ω, THD +N < 0.7%, 20Hz ≤ F ≤ 20kHz)		100		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz
V_N	Output Voltage Noise, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω Unweighted, Av = 1 A weighted, Av = 1 Unweighted, Av = 2.5 A weighted, Av = 2.5 Unweighted, Av = 7.5 A weighted, Av = 7.5 Unweighted, Standby A weighted, Standby		 6 5.5 12 10.5 33 28 1.5 1		µV_{RMS}
T_{WU}	Wake-Up Time[2] C_b =1µF		15		ms

1) Dynamic measurements - 20*log(rms(Vout)/rms (Vripple)). Vripple is the super-imposed sinus signal relative to Vcc.

2) Transition time from standby mode to fully operational amplifier.

Table 5. Electrical Characteristics - V_{CC} = +2.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		3	7	mA
$I_{STANDBY}$	Standby Current No input signal, Vstdby = V_{SM} = G_{ND}, RL = 8Ω No input signal, Vstdby = V_{SM} = V_{CC}, RL = 8Ω		10	1000	nA
Voo	Differential Output Offset Voltage No input signal, RL = 8Ω		0.1	10	mV
V_{ICM}	Input Common Mode Voltage CMRR ≤ -60dB	0.6		V_{CC}- 0.9	V
Po	Output Power THD = 1% Max, F= 1kHz, RL = 8Ω	200	250		mW
THD + N	Total Harmonic Distortion + Noise Po = 225mW rms, Av = 1, 20Hz ≤ F ≤ 20kHz, RL = 8Ω		0.5		%
$PSRR_{IG}$	Power Supply Rejection Ratio with Inputs Grounded[1] F = 217Hz, R = 8Ω, Av = 1, C_{in} = 4.7µF, C_b =1µF Vripple = 200mV_{PP}		100		dB
CMRR	Common Mode Rejection Ratio F = 217Hz, RL = 8Ω, Av = 1, C_{in} = 4.7µF, C_b =1µF Vic = 200mV_{PP}		90		dB
SNR	Signal-to-Noise Ratio (A Weighted Filter, A_v = 2.5) (R_L = 8Ω, THD +N < 0.7%, 20Hz ≤ F ≤ 20kHz)		100		dB
GBP	Gain Bandwidth Product R_L = 8Ω		2		MHz
V_N	Output Voltage Noise, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω Unweighted, Av = 1 A weighted, Av = 1 Unweighted, Av = 2.5 A weighted, Av = 2.5 Unweighted, Av = 7.5 A weighted, Av = 7.5 Unweighted, Standby A weighted, Standby		6 5.5 12 10.5 33 28 1.5 1		µV_{RMS}
T_{WU}	Wake-Up Time[2] C_b =1µF		15		ms

1) Dynamic measurements - 20*log(rms(Vout)/rms (Vripple)). Vripple is the super-imposed sinus signal relative to Vcc.

2) Transition time from standby mode to fully operational amplifier.

Figure 3. Current consumption vs. power supply voltage

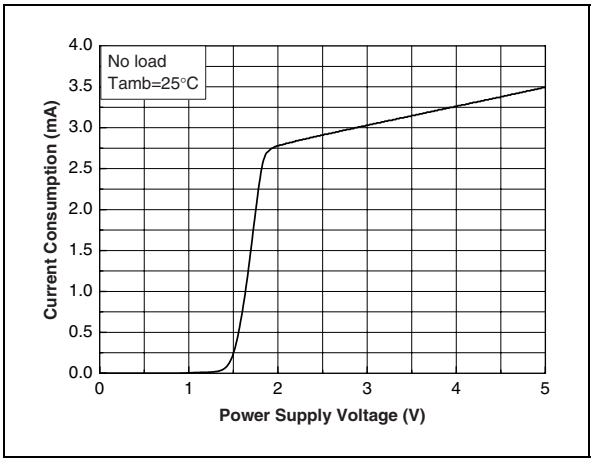


Figure 4. Current consumption vs. standby voltage

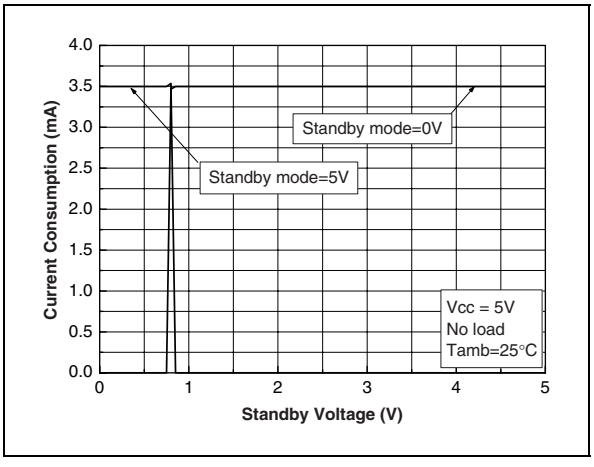


Figure 5. Current consumption vs. standby voltage

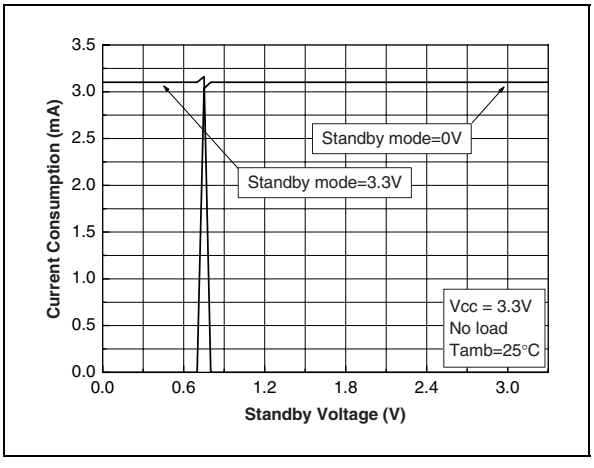


Figure 6. Current consumption vs. standby voltage

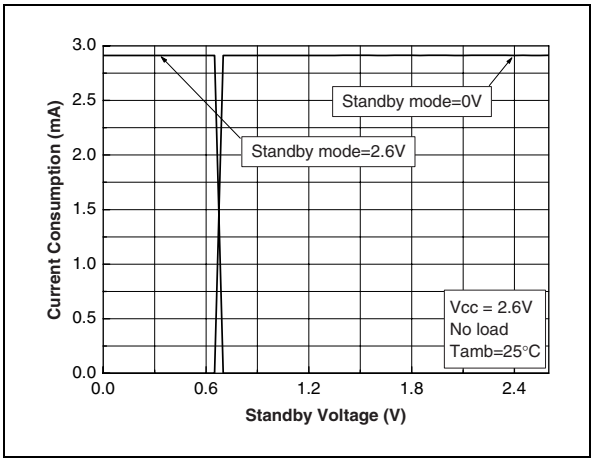


Figure 7. Differential DC output voltage vs. common mode input voltage

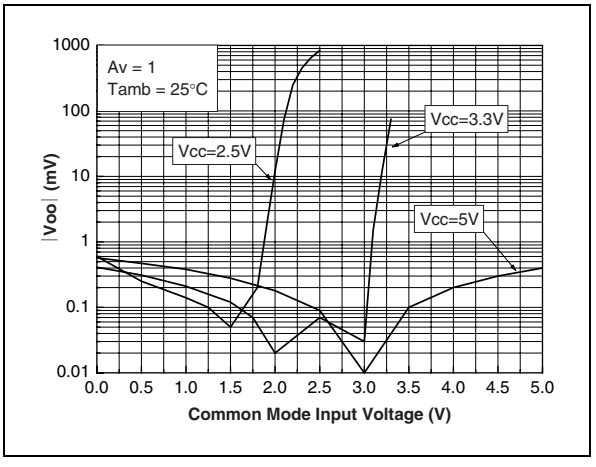


Figure 8. Power dissipation vs. output power

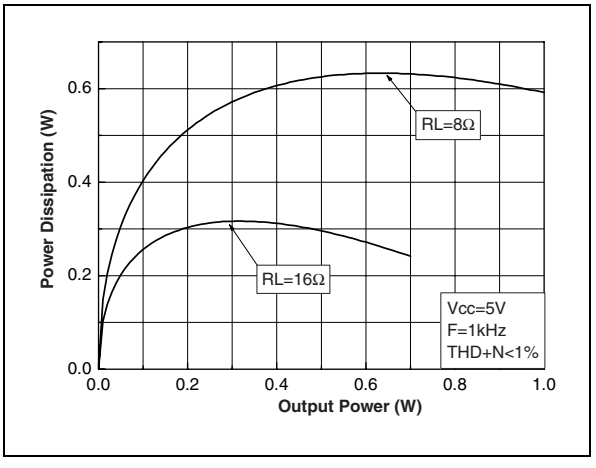


Figure 9. Power dissipation vs. output power

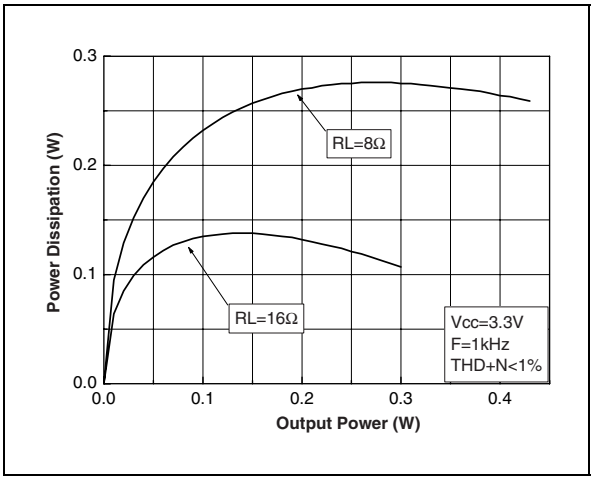


Figure 10. Power dissipation vs. output power

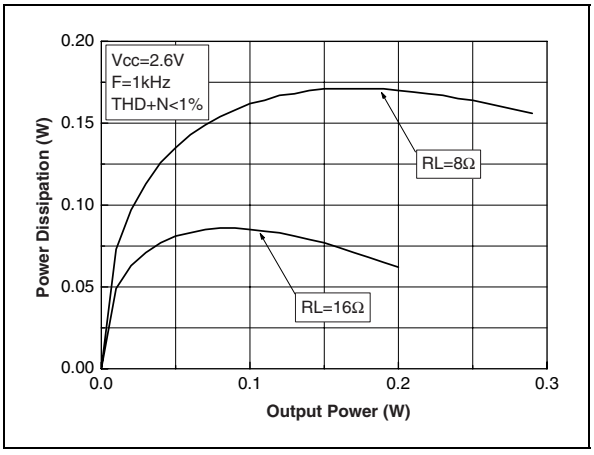


Figure 11. Output power vs. power supply voltage

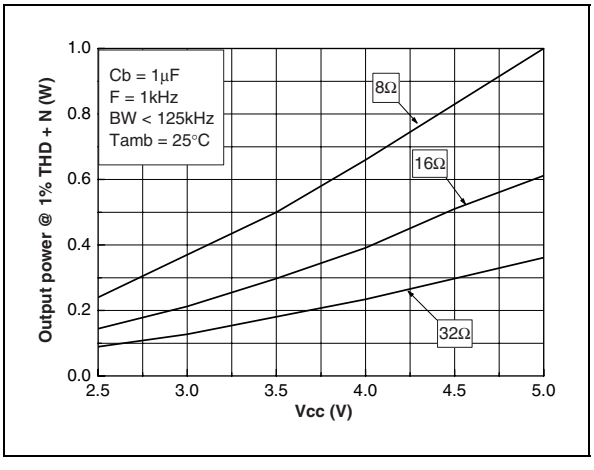


Figure 12. Output power vs. power supply voltage

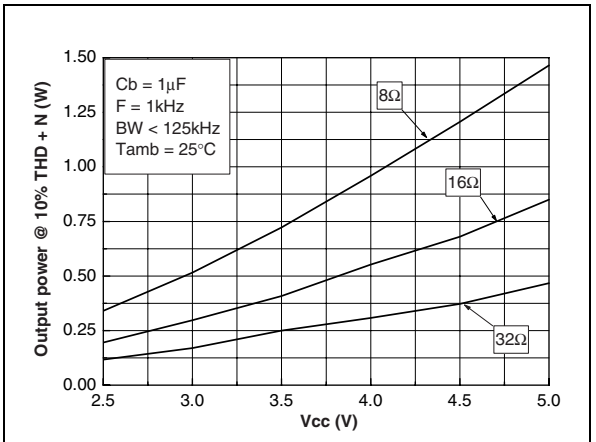


Figure 13. Output power vs. load resistance

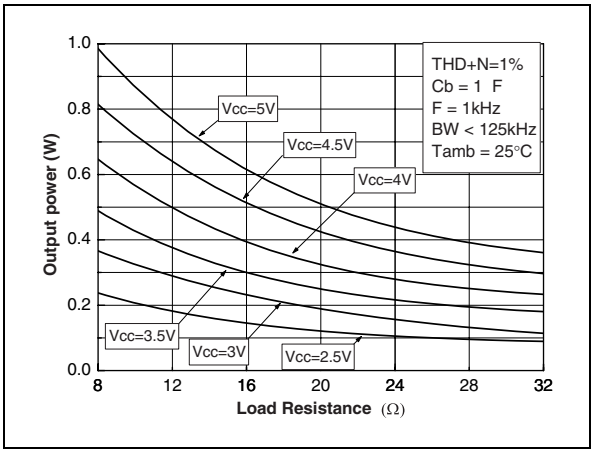


Figure 14. Power derating curves

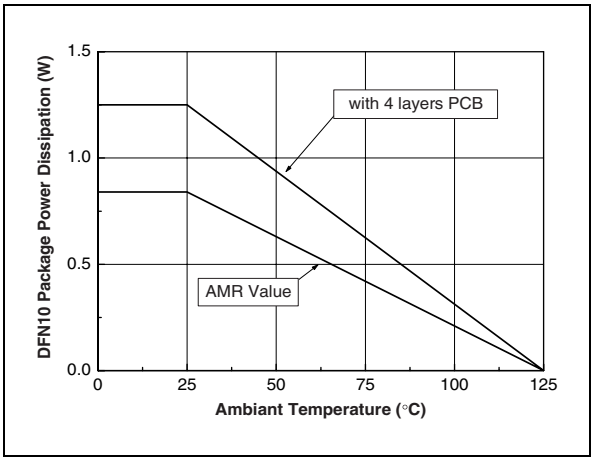


Figure 15. Power derating curves

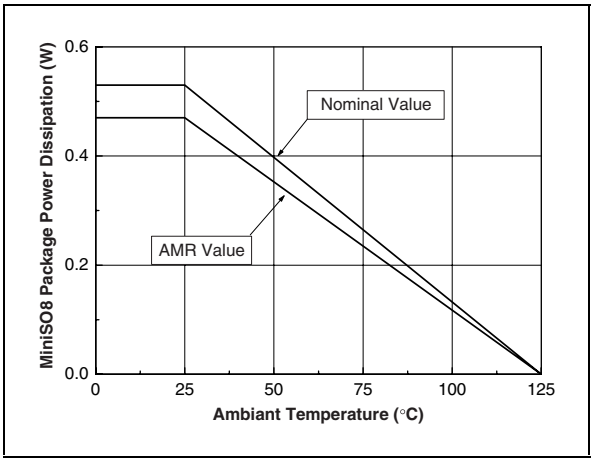


Figure 16. Open loop gain vs. frequency

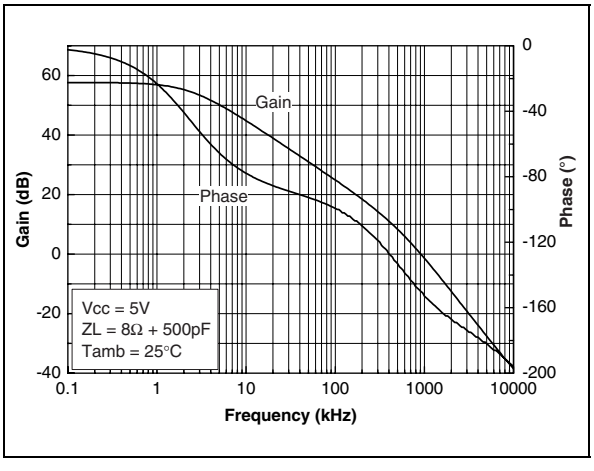


Figure 17. Open loop gain vs. frequency

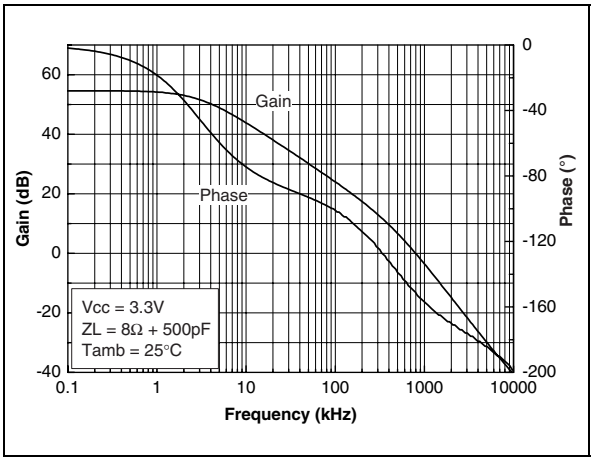


Figure 18. Open Loop gain vs. frequency

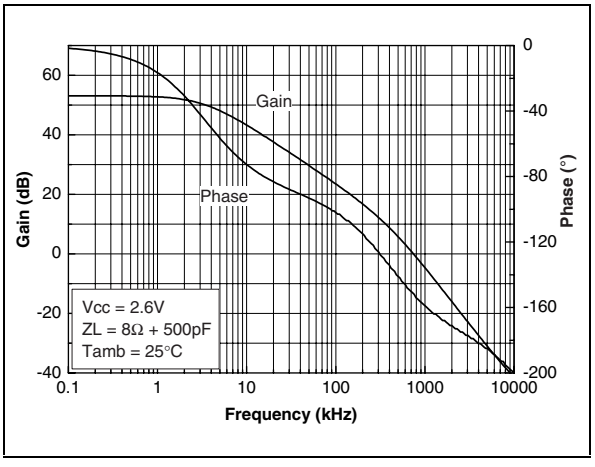


Figure 19. Close loop gain vs. frequency

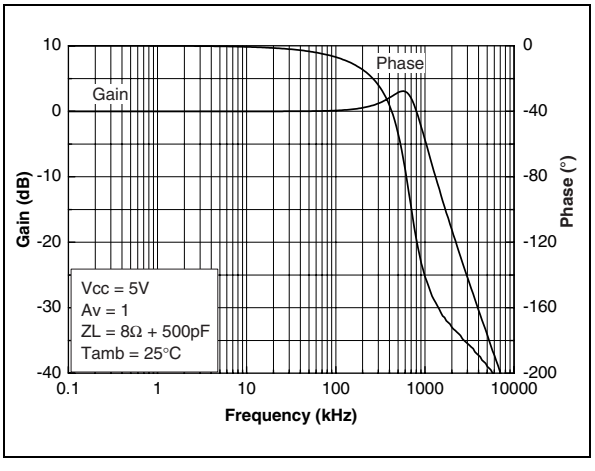


Figure 20. Close loop gain vs. frequency

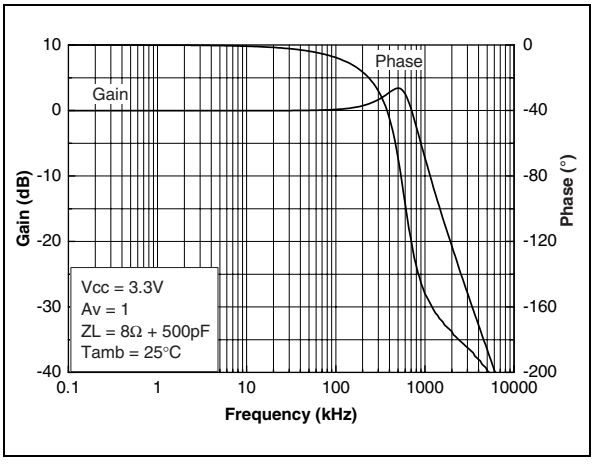


Figure 21. Close loop gain vs. frequency

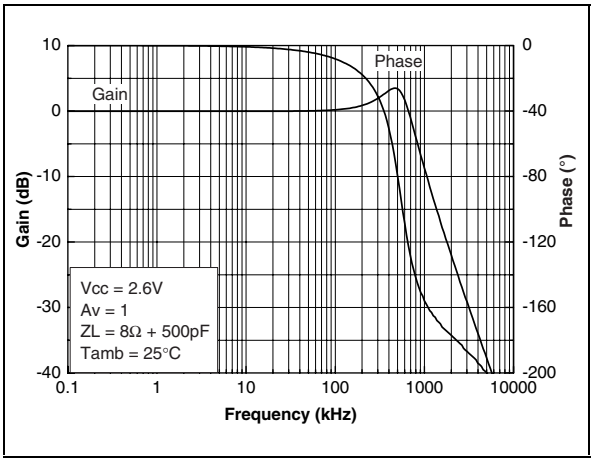


Figure 22. PSRR vs. frequency

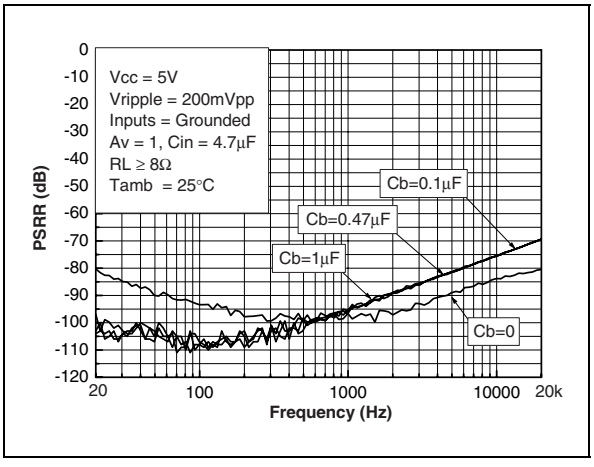


Figure 23. PSRR vs. frequency

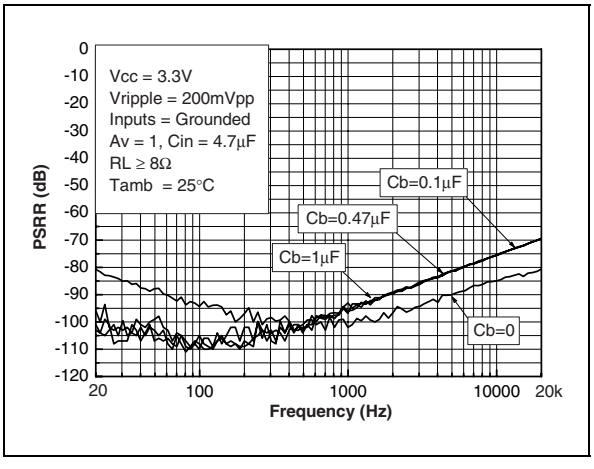


Figure 24. PSRR vs. frequency

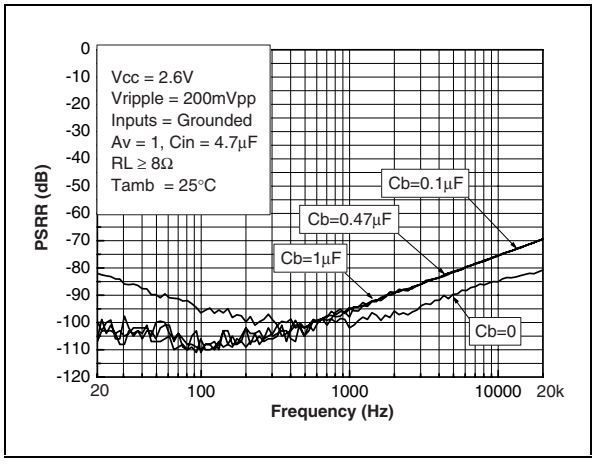


Figure 25. PSRR vs. frequency

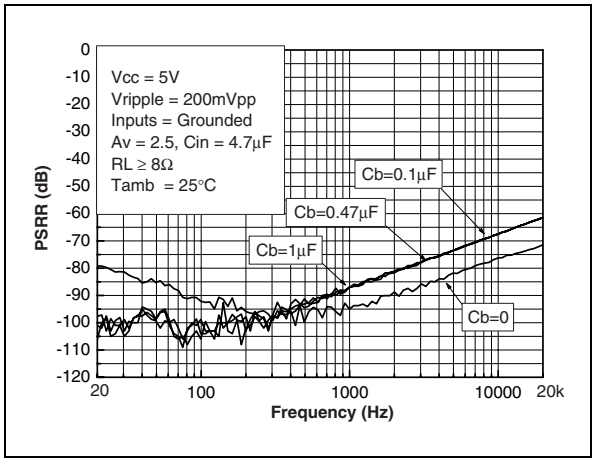


Figure 26. PSRR vs. frequency

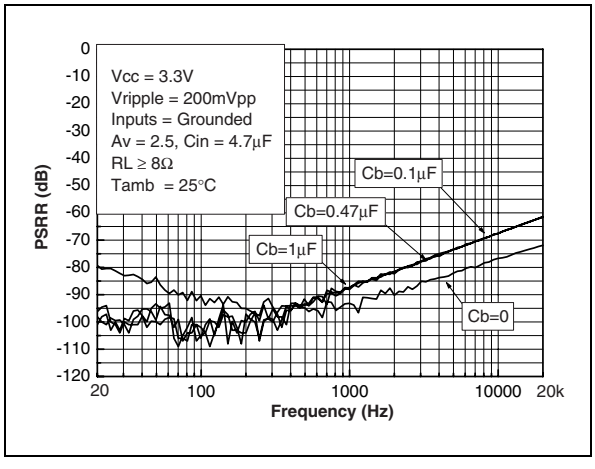


Figure 27. PSRR vs. frequency

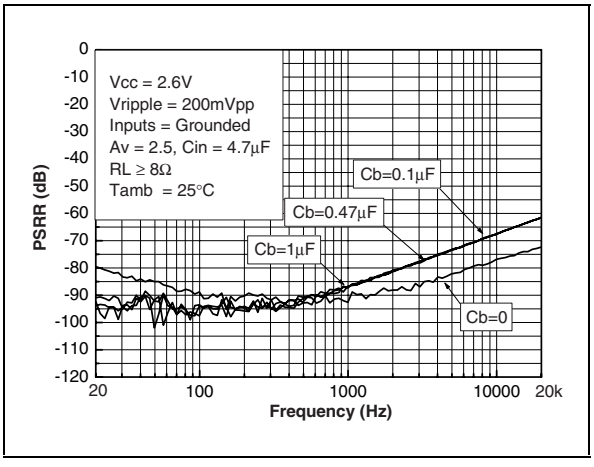


Figure 28. PSRR vs. frequency

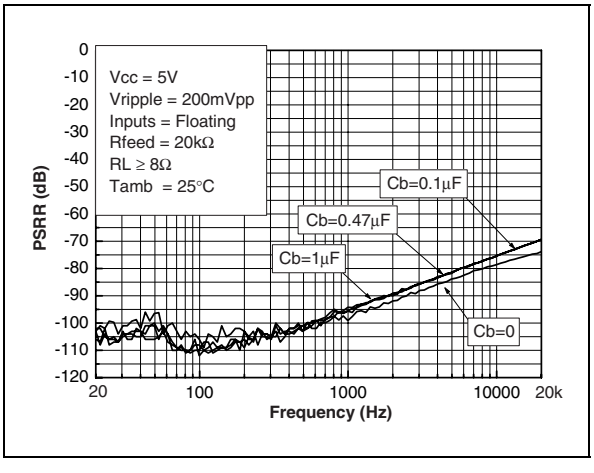


Figure 29. PSRR vs. frequency

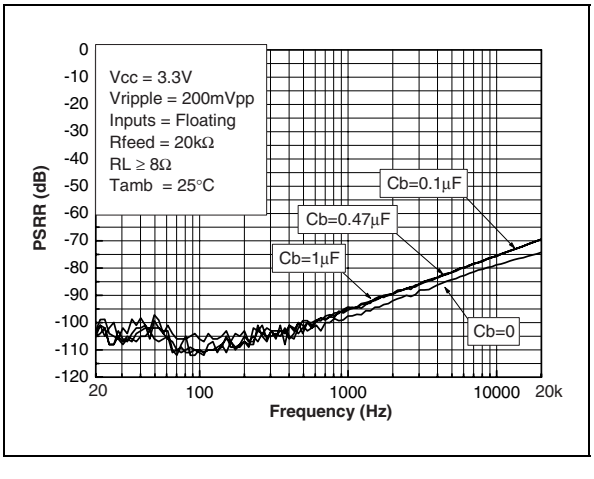


Figure 30. PSRR vs. frequency

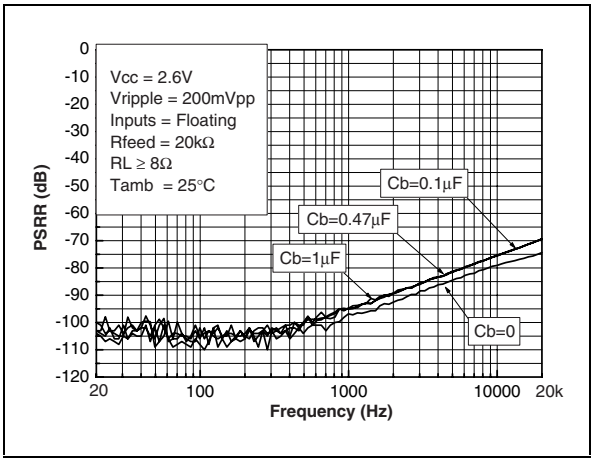


Figure 31. PSRR vs. common mode input voltage

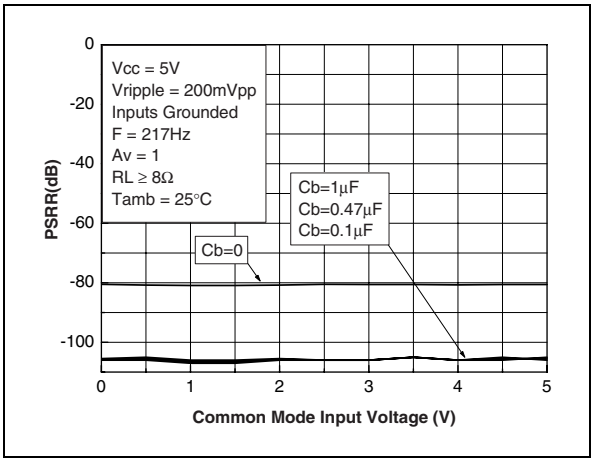


Figure 32. PSRR vs. common mode input voltage

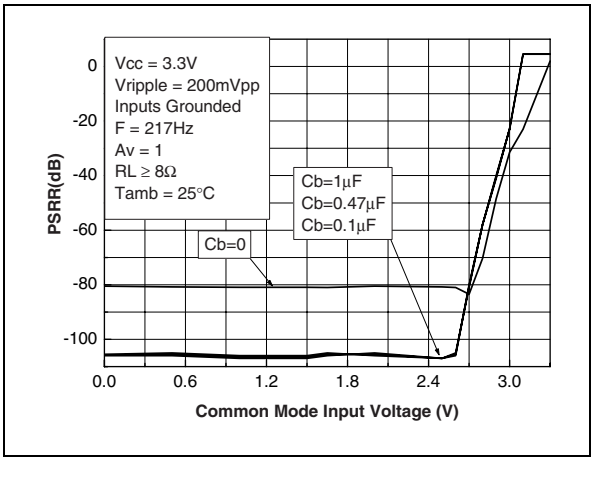


Figure 33. PSRR vs. common mode input voltage

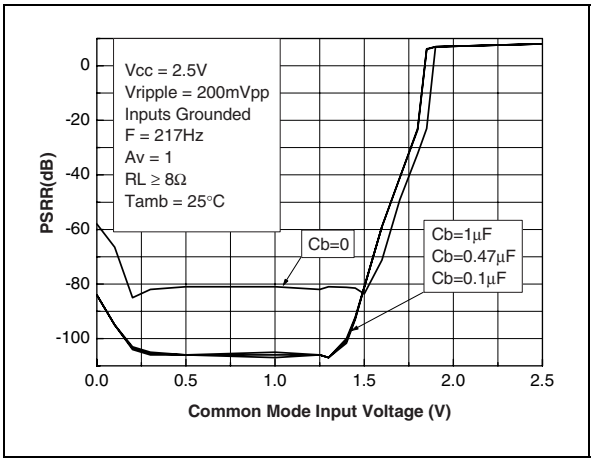


Figure 34. CMRR vs. frequency

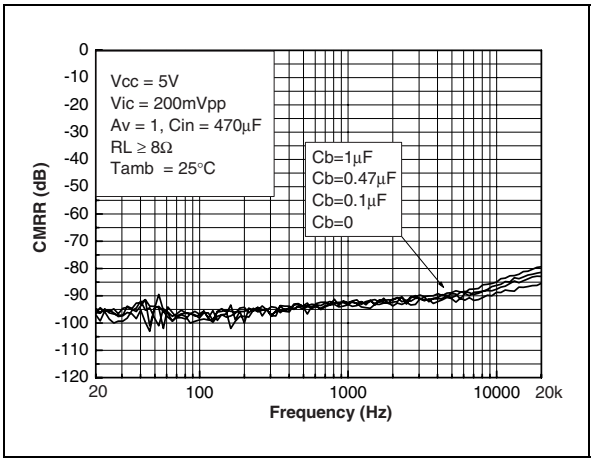


Figure 35. PSRR vs. frequency

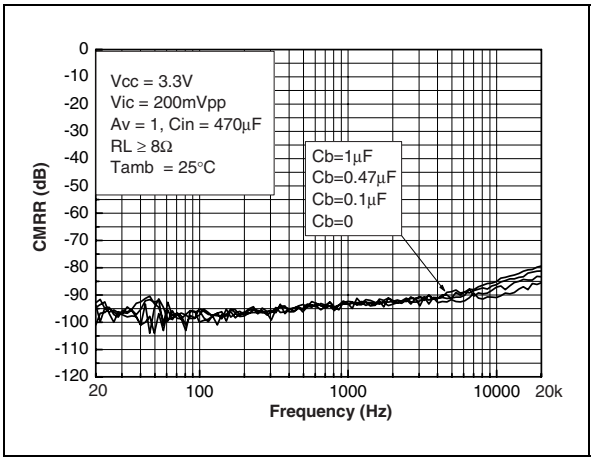


Figure 36. CMRR vs. frequency

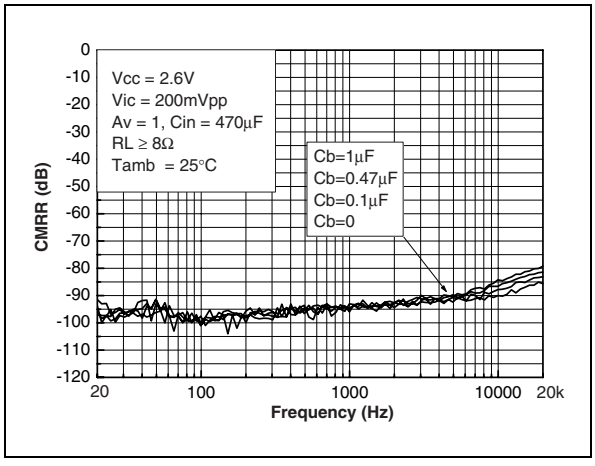


Figure 37. CMRR vs. frequency

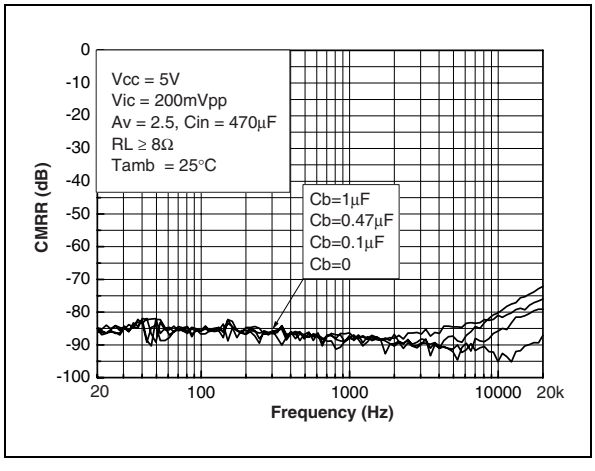


Figure 38. CMRR vs. frequency

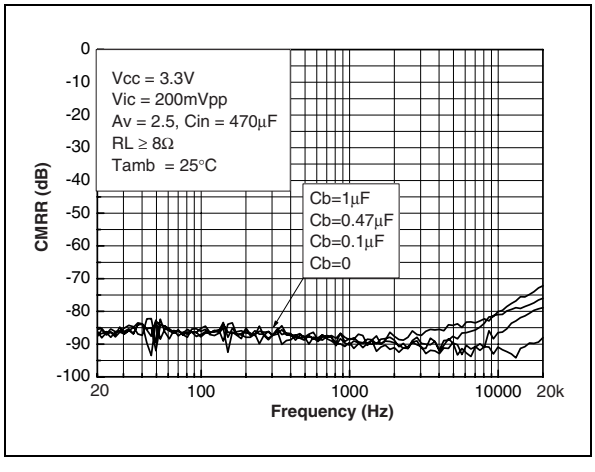


Figure 39. CMRR vs. frequency

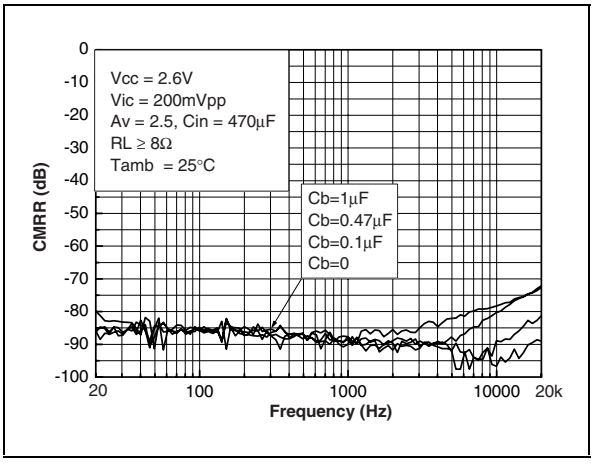


Figure 40. CMRR vs. common mode input voltage

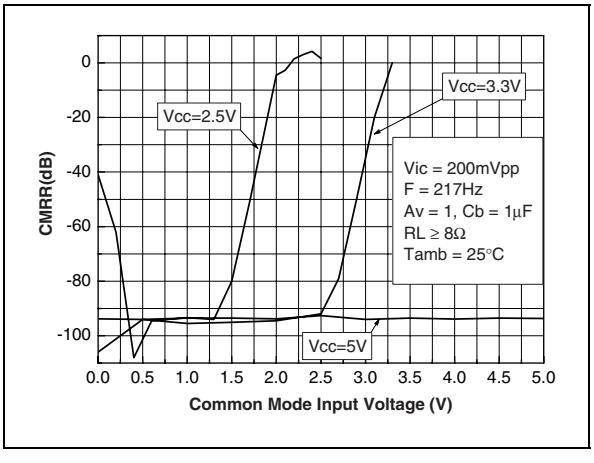


Figure 41. CMRR vs. common mode input voltage

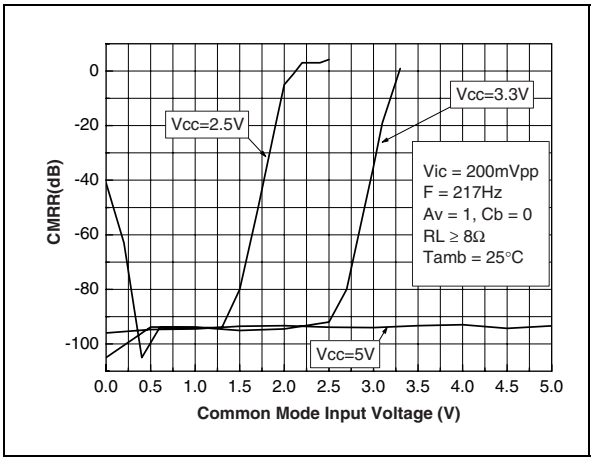


Figure 42. THD+N vs. output power

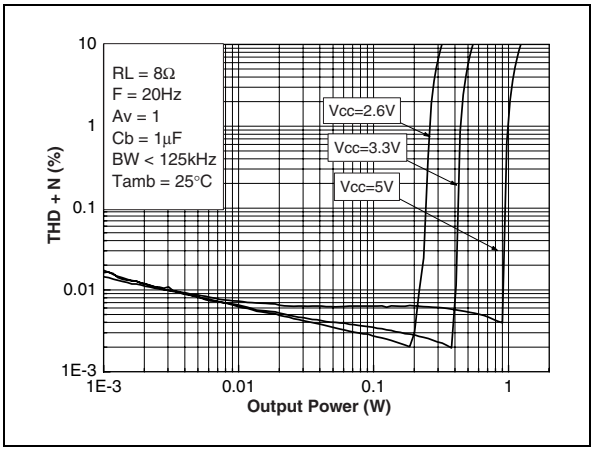


Figure 43. THD+N vs. output power

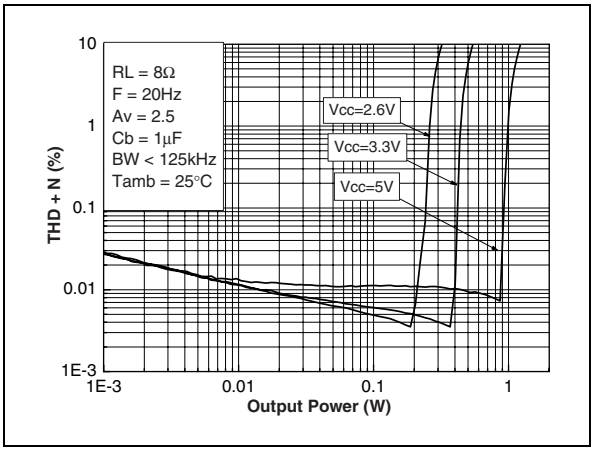


Figure 44. THD+N vs. output power

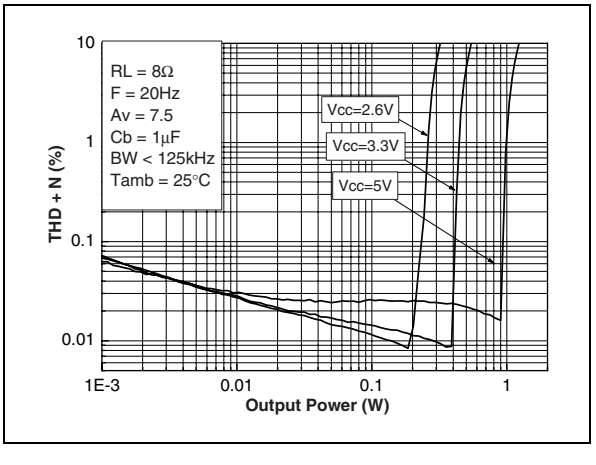


Figure 45. THD+N vs. output power

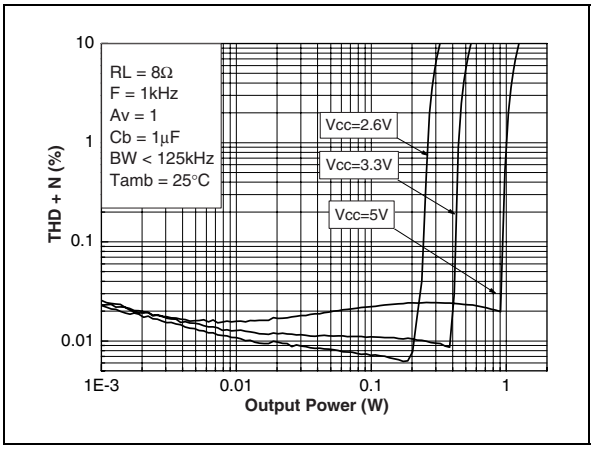


Figure 46. THD+N vs. output power

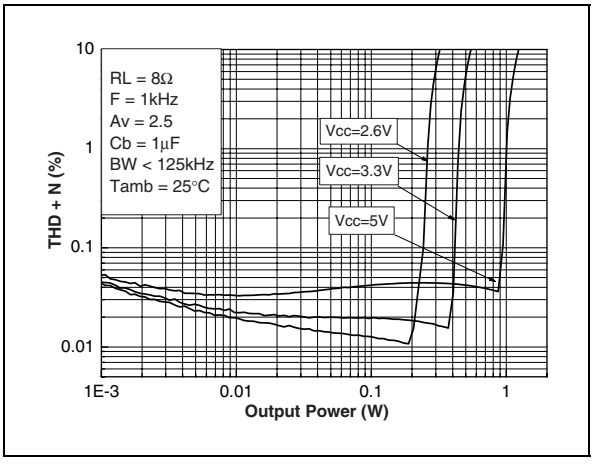


Figure 47. THD+N vs. output power

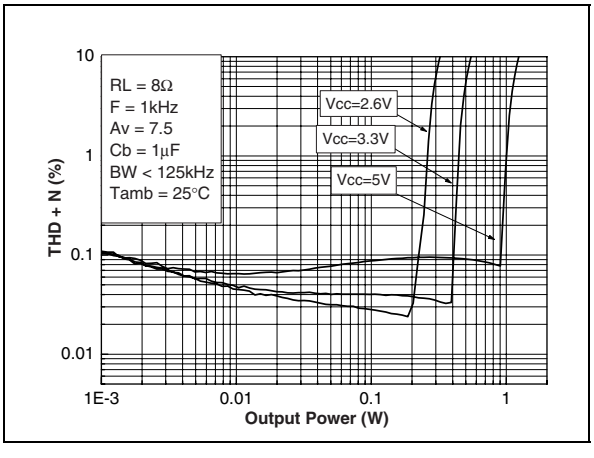


Figure 48. THD+N vs. output power

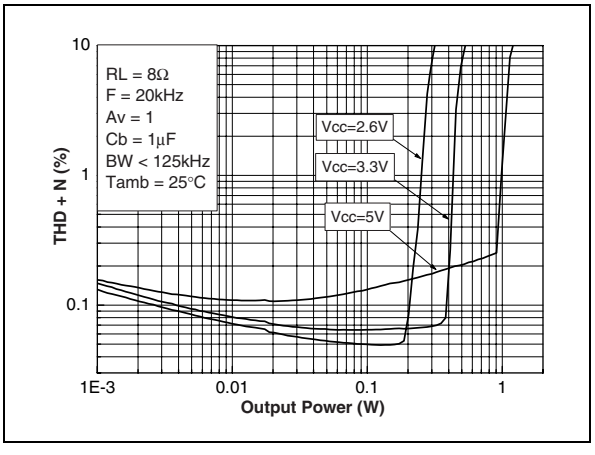


Figure 49. THD+N vs. output power

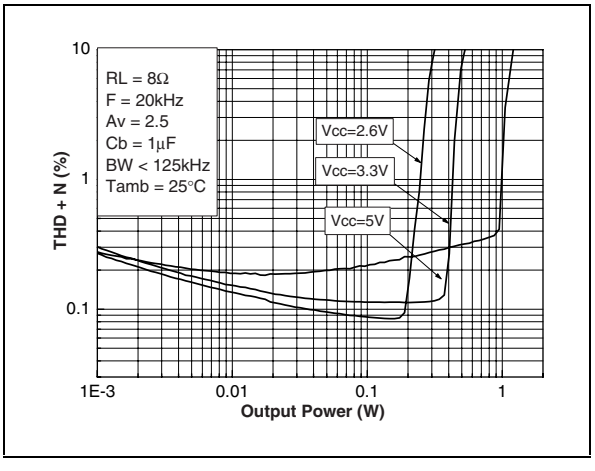


Figure 50. THD+N vs. output power

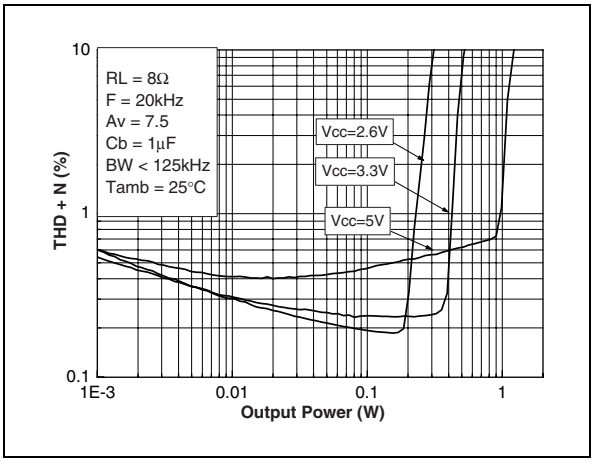


Figure 51. THD+N vs. output power

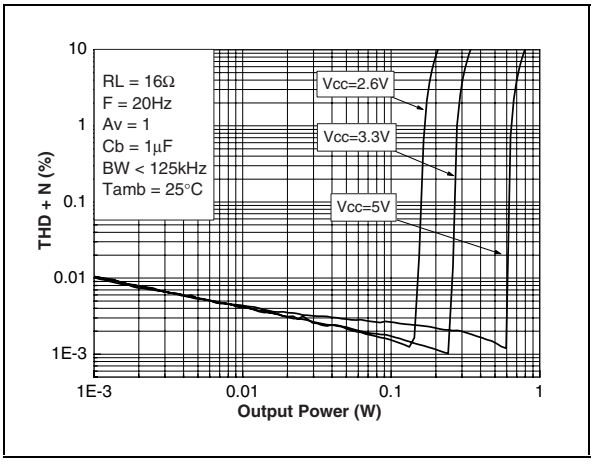


Figure 52. THD+N vs. output power

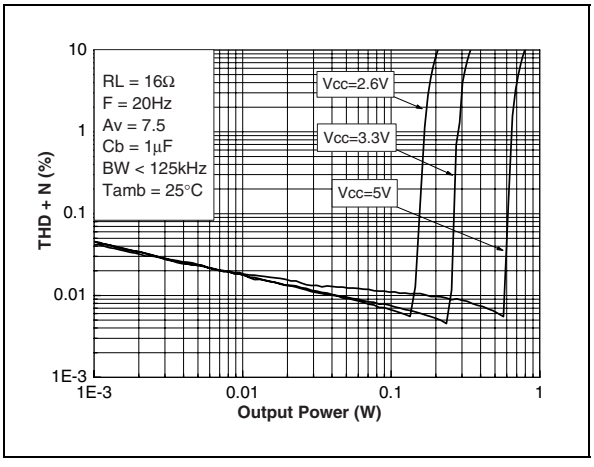


Figure 53. THD+N vs. output power

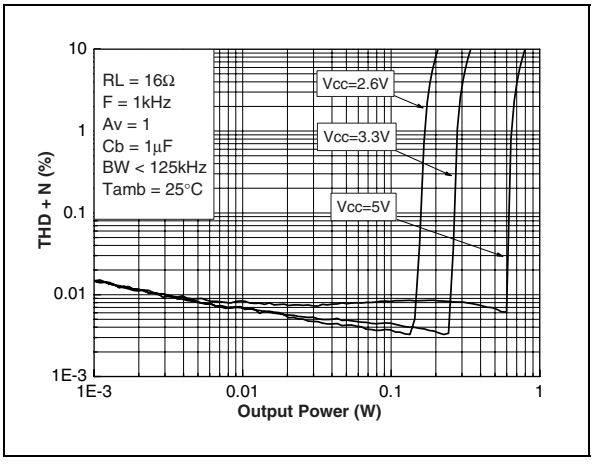


Figure 54. THD+N vs. output power

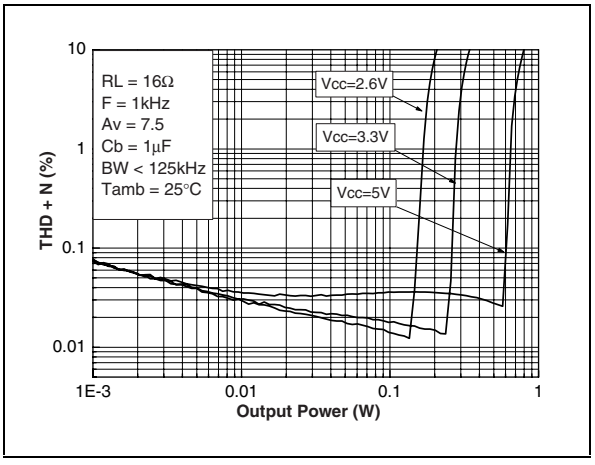


Figure 55. THD+N vs. output power

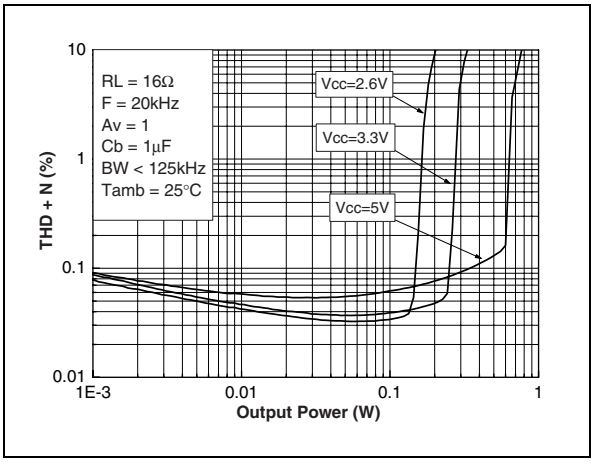


Figure 56. THD+N vs. output power

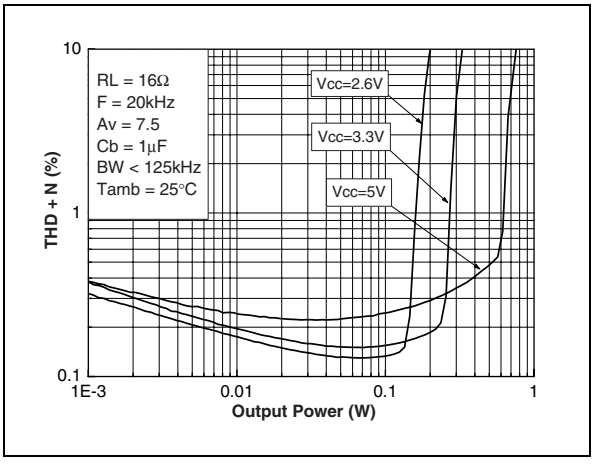


Figure 57. THD+N vs. output power

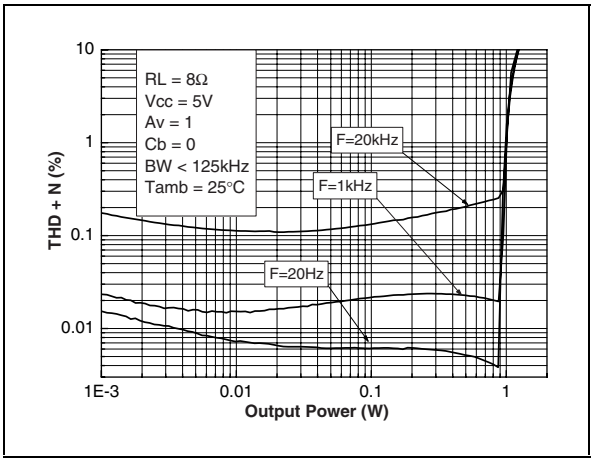


Figure 58. THD+N vs. output power

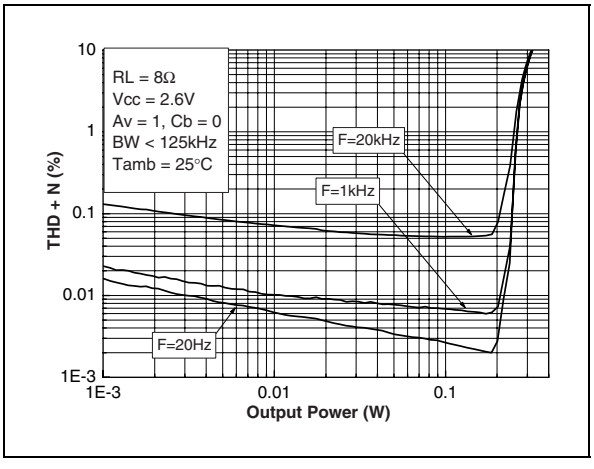


Figure 59. THD+N vs. output power

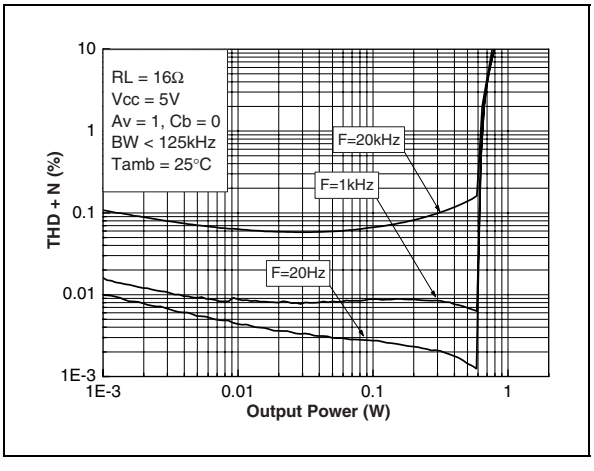


Figure 60. THD+N vs. output power

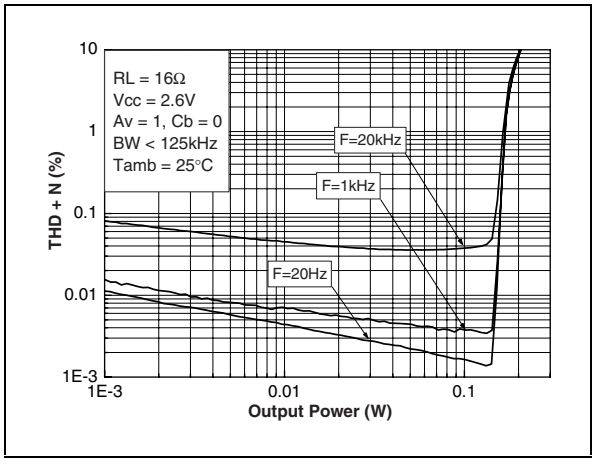


Figure 61. THD+N vs. frequency

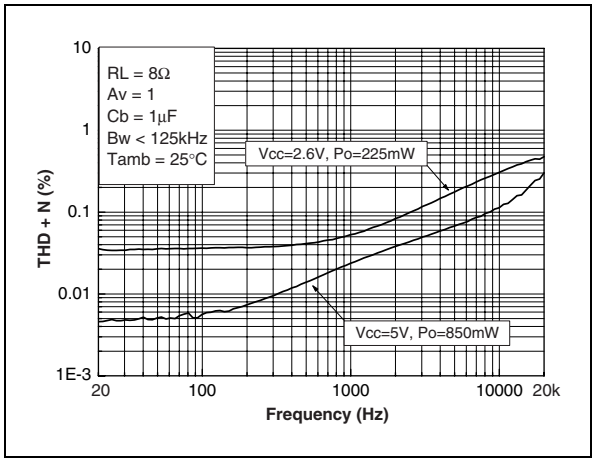


Figure 62. THD+N vs. frequency

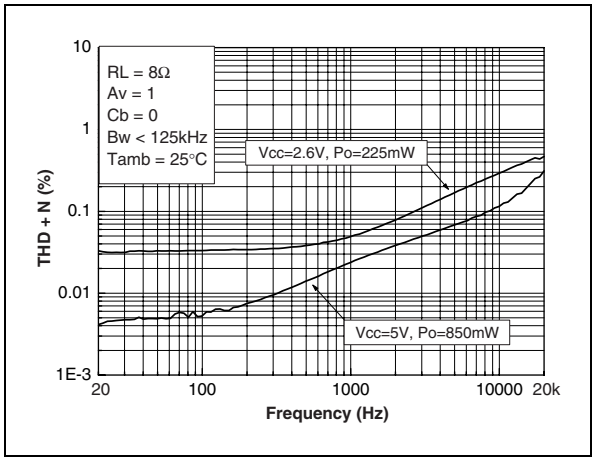


Figure 63. THD+N vs. frequency

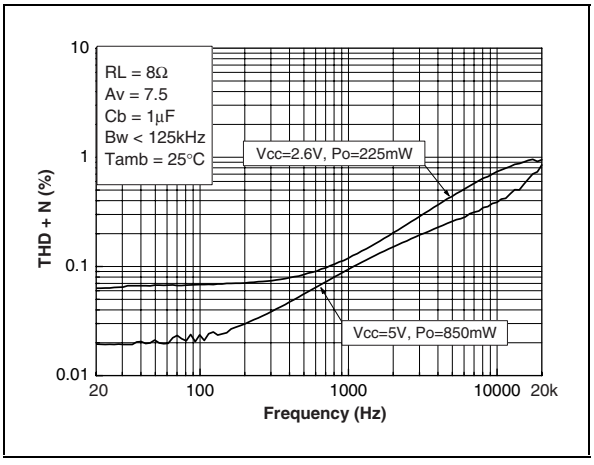


Figure 64. THD+N vs. frequency

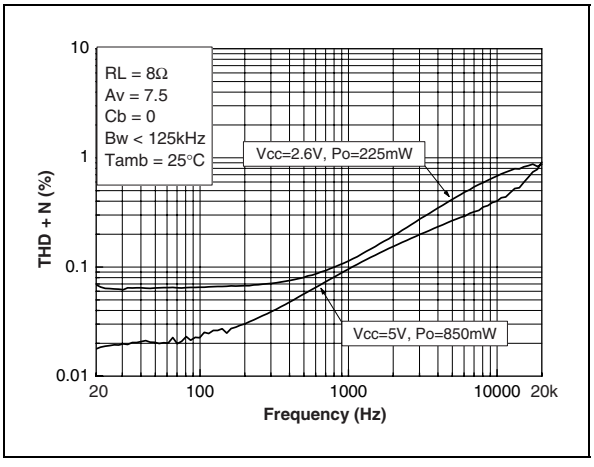


Figure 65. THD+N vs. frequency

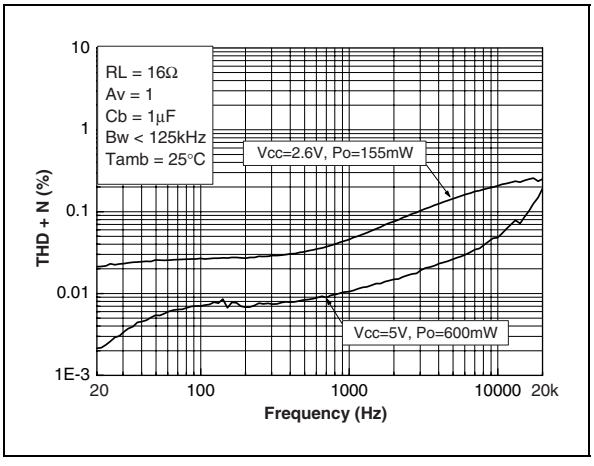


Figure 66. THD+N vs. frequency

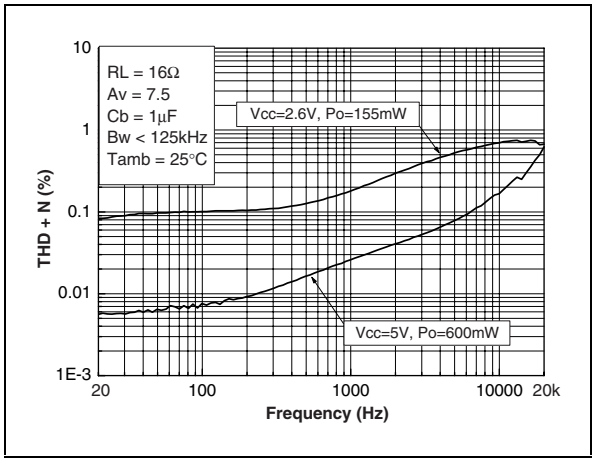


Figure 67. SNR vs. power supply voltage with unweighted filter

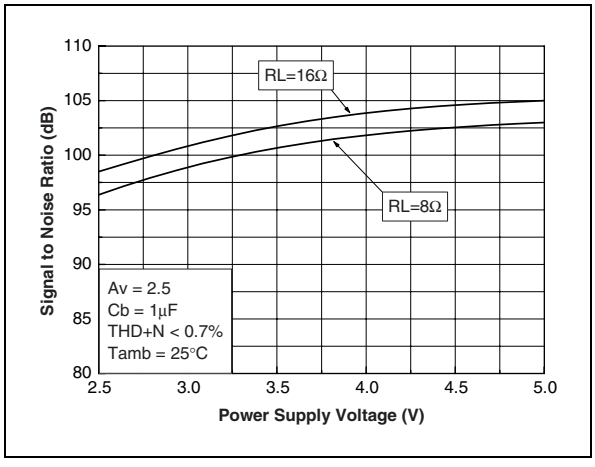


Figure 68. SNR vs. power supply voltage with a weighted filter

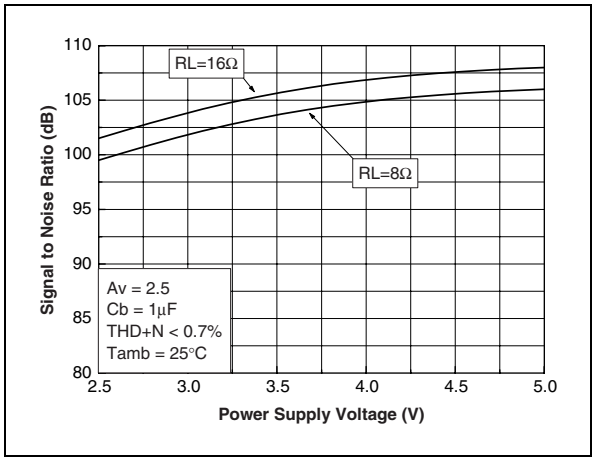
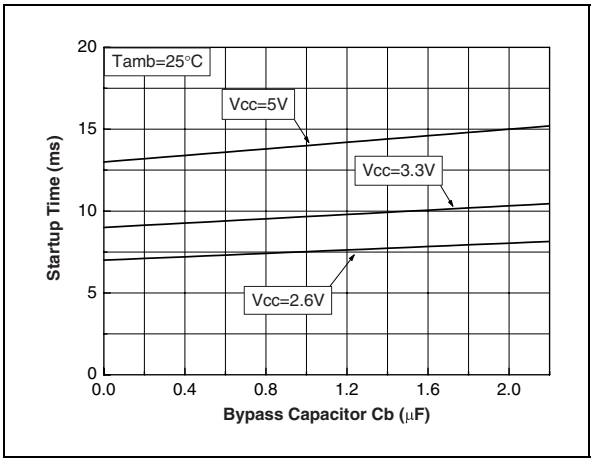


Figure 69. Startup time vs. bypass capacitor



4 Application Information

4.1 Differential configuration principle

The TS4994 is a monolithic full-differential input/ output power amplifier. The TS4994 also includes a common mode feedback loop that controls the output bias value to average it at Vcc/2 for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- Very high PSRR (Power Supply Rejection Ratio).
- High common mode noise rejection.
- Virtually zero pop without additional circuitry, giving an faster start-up time compared to conventional single-ended input amplifiers.
- Easier interfacing with differential output audio DAC.
- No input coupling capacitors required thanks to common mode feedback loop.
- In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. But, to reach maximal performances in all tolerance situations, it's better to keep this option.

The main **disadvantage** is:

- As the differential function is directly linked to external resistors mismatching, in order to reach maximal performances of the amplifier paying particular attention to this mismatching is mandatory.

4.2 Gain in typical application schematic

Typical differential applications are shown on the figures on page 2.

In the flat region of the frequency-response curve (no C_{in} effect), the differential gain is expressed by the relation:

$$Av_{diff} = \frac{V_{O+} - V_{O-}}{Diff._{Input} + -Diff._{Input-}} = \frac{R_{feed}}{R_{in}}$$

where $R_{in} = R_{in1} = R_{in2}$ and $R_{feed} = R_{feed1} = R_{feed2}$.

Note: For the rest of this chapter, Av_{diff} will be called Av to simplify the expression.

4.3 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at Vcc/2 for any DC common mode bias input voltage.

However, due to VICM limitation of the input stage (see *Electrical Characteristics on page 4*), the common mode feedback loop can ensure its role only within a defined range. This range depends upon the values of Vcc, R_{in} and R_{feed} (Av). To have a good estimation of the VICM value, we can apply this formula:

$$V_{ICM} = \frac{Vcc \times R_{in} + 2 \times V_{IC} \times R_{feed}}{2 \times (R_{in} + R_{feed})} \quad (V)$$

with

$$V_{IC} = \frac{Diff._{Input+} + Diff._{Input-}}{2} \quad (V)$$

and the result of the calculation must be in the range:

$$0.6V \leq V_{ICM} \leq Vcc - 0.9V$$

If the result of VICM calculation is not in the previous range, an input coupling capacitor must be used.

Example: With Vcc=2.5V, R_{in}=R_{feed}=20k and V_{IC}=2V, we found V_{ICM}=1.63V. This is higher than 2.5V-0.9V=1.6V, so input coupling capacitors are required or you will have to change the V_{IC} value.

4.4 Low and high frequency response

In the low frequency region, C_{in} starts to have an effect. C_{in} forms, with R_{in}, a high-pass filter with a -3dB cut-off frequency. F_{CL} is in Hz.

$$F_{CL} = \frac{1}{2 \times \pi \times R_{in} \times C_{in}} \quad (Hz)$$

In the high-frequency region, you can limit the bandwidth by adding a capacitor (C_{feed}) in parallel with R_{feed}. It forms a low-pass filter with a -3dB cut-off frequency. F_{CH} is in Hz.

$$F_{CH} = \frac{1}{2 \times \pi \times R_{feed} \times C_{feed}} \quad (Hz)$$

While these bandwidth limitations are in theory attractive, in practice, because of low performance in terms of capacitor precision (and by consequence in terms of mismatching), they deteriorate the values of PSRR and CMRR.

We will discuss the influence of mismatching on PSRR and CMRR performance in more detail in the following paragraphs.

Example: A typical application with input coupling and feedback capacitor with F_{CL}=50Hz and F_{CH}=8kHz. We assume that the mismatching between $R_{in1,2}$ and $C_{feed1,2}$ can be neglected. If we sweep the frequency from DC to 20kHz we observe the following with respect to the PSRR value:

- From DC to 200Hz, the C_{in} impedance decreases from infinite to a finite value and the C_{feed} impedance is high enough to be neglected. Due to the tolerance of $C_{in1,2}$, we must introduce a mismatch factor (R_{in1} x C_{in} $\neq$ R_{in2} x C_{in2}) that will decrease the PSRR performance.
- From 200Hz to 5kHz, the C_{in} impedance is low enough to be neglected when compare to $R_{in,}$ and the C_{feed} impedance is high enough to be neglected as well. In this range, we can reach the PSRR performance of the TS4994 itself.
- From 5kHz to 20kHz, the C_{in} impedance is low to be neglected when compared to $R_{in,}$ and the C_{feed} impedance decreases to a finite value. Due to tolerance of $C_{feed1,2}$, we introduce a mismatching factor (R_{feed1} x C_{feed1} $\neq$ R_{feed2} x C_{feed2}) that will decrease the PSRR performance.

4.5 Calculating the influence of mismatching

On PSRR performance:

For this calculation, we consider that C_{in} and C_{feed} have no influence.

We use the same kind of resistor (same tolerance) and ΔR is the tolerance value in %.

The following equation is valid for frequencies ranging from DC to about 1kHz. Above this frequency, parasitic effects start to be significant and a literal equation is not possible to write.

The PSRR equation is (ΔR in %):

$$PSRR \leq 20 \times Log\left[\frac{\Delta R \times 100}{(10000 - \Delta R^2)}\right] \quad (dB)$$

This equation doesn't include the additional performance provided by bypass capacitor filtering. If a bypass capacitor is added, it acts, together with the internal high output impedance bias, as a low-pass filter, and the result is a quite important PSRR improvement with a relatively small bypass capacitor.

The complete PSRR equation (ΔR in %, C_b in microFarad and F in Hz) is:

$$PSRR \leq 20 \times \log\left[\frac{\Delta R \times 100}{(10000 - \Delta R^2) \times \sqrt{1 + F^2 \times {C_b}^2 \times 22.2}}\right] \quad (dB)$$

Example: With ΔR=0.1% and C_b=0, the minimum PSRR would be -60dB. With a 100nF bypass capacitor, at 100Hz the new PSRR would be -93dB.

This example is a worst case scenario, where each resistor has extreme tolerance and illustrates the fact that with only a small bypass capacitor, the TS4994 produce high PSRR performance.

In addition, it's important to note that this is a theoretical formula. As the TS4994 has self-generated noise, you should consider that the highest practical PSRR reachable is about -110dB. It is therefore unreasonable to target a -120dB PSRR.

The three following graphs show PSRR versus frequency and versus bypass capacitor C_b in worst-case condition (ΔR=0.1%).

Figure 70. PSRR vs. frequency worst case condition

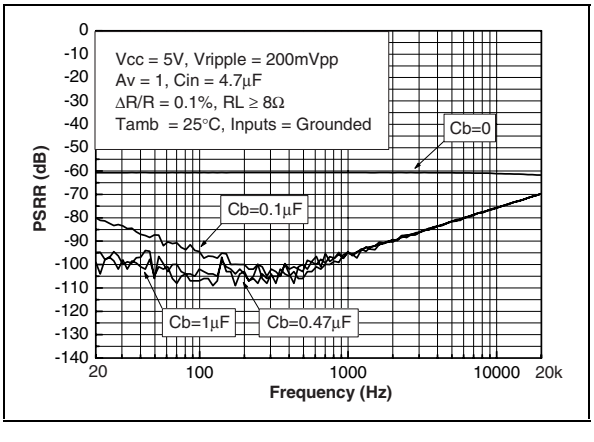


Figure 71. PSRR vs. frequency worst case condition

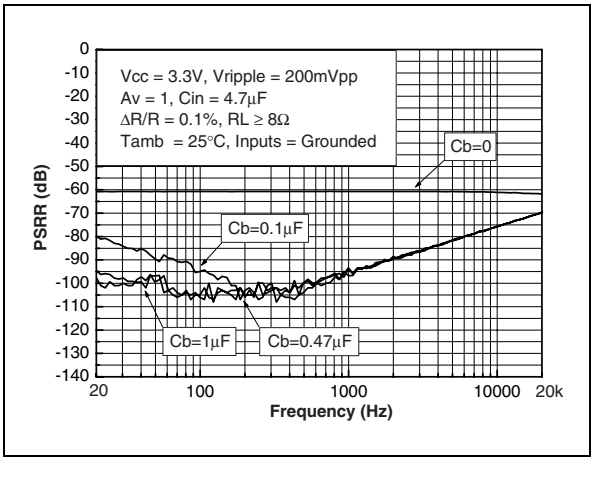
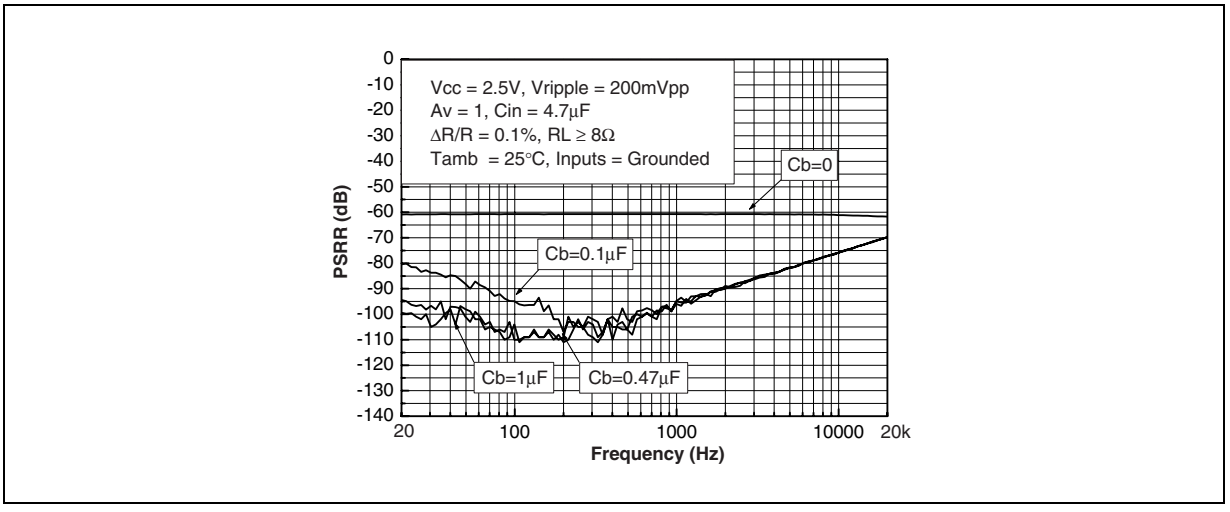


Figure 72. PSRR vs. frequency worst case condition



The two following graphs show typical application of TS4994 with four 0.1% tolerances and a random choice for them.

Figure 73. PSRR vs. frequency with random choice condition

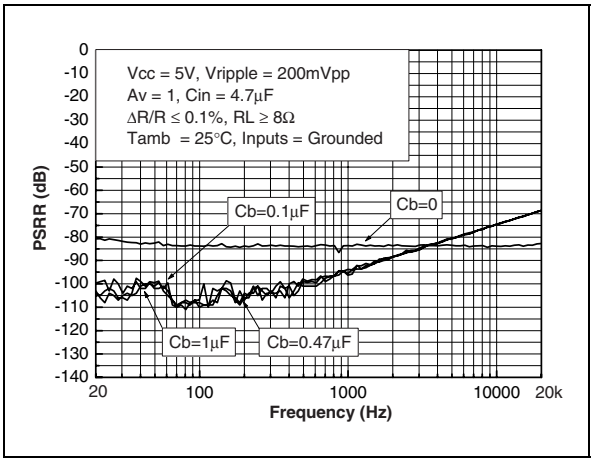
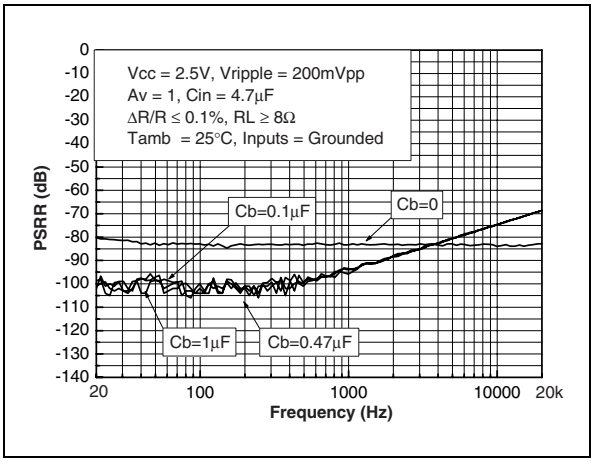


Figure 74. PSRR vs. frequency with random choice condition



CMRR performance

For this calculation, we consider there to be no influence of C_{in} and C_{feed}. C_b has no influence in the calculation of the CMRR.

We use the same kind of resistor (same tolerance) and ΔR is the tolerance value in %.

The following equation is valid for frequencies ranging from DC to about 1kHz. Above this frequency, parasitic effects start to be significant and a literal equation is not possible to write.

The CMRR equation is (ΔR in %):

$$CMRR \leq 20 \times Log\left[\frac{\Delta R \times 200}{(10000 - \Delta R^2)}\right] \quad (dB)$$

Example: With ΔR=1%, the minimum CMRR would be -34dB.
With a DC Vic=2.5V, the DC differential output (Voo) which results is 50mV maximum. As this Voo is across the load, for an 8Ω load the extra consumption would be 50mV/8=6.2mA.

With ΔR=1%, the minimum CMRR would be -53dB that give Voo=5.6mV and an maximum extra consumption less than 700µA.

This example is of a worst case scenario where each resistor has extreme tolerance and illustrates the fact that for CMRR, good matching is essential.

As with the PSRR, due to self-generated noise, the TS4994 CMRR limitation would be about -110dB.

Figures 75 and 76 show CMRR versus frequency and versus bypass capacitor C_b in worst-case condition (ΔR=0.1%).

Figure 75. CMRR vs. frequency worst case condition

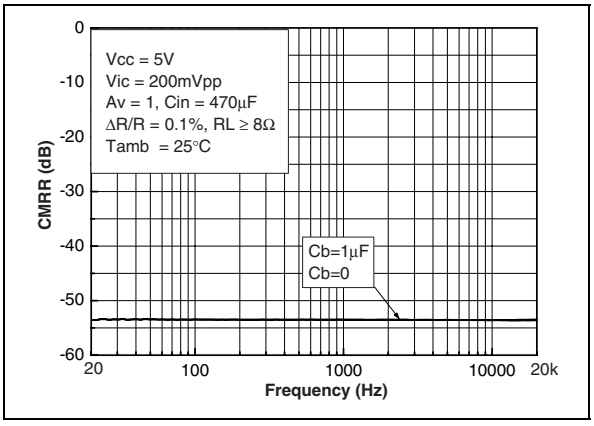
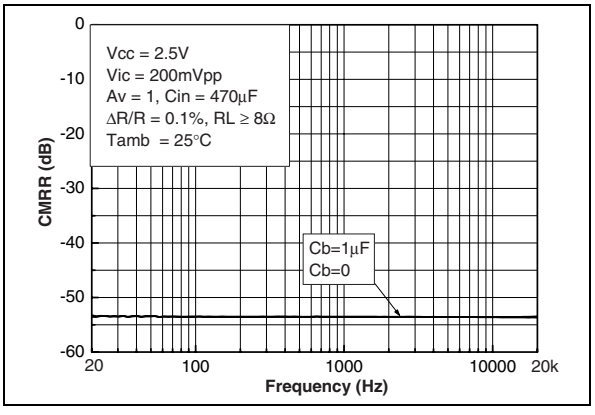


Figure 76. CMRR vs. frequency worst case condition



Figures 77 and 78 show CMRR versus frequency for a typical application with four 0.1% tolerances and a random choice for them.

Figure 77. CMRR vs. frequency with random choice condition

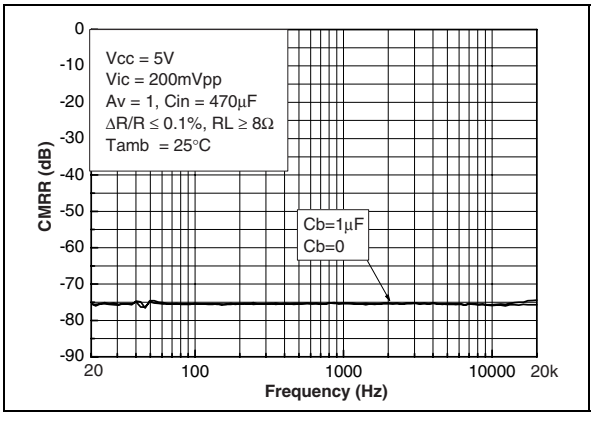
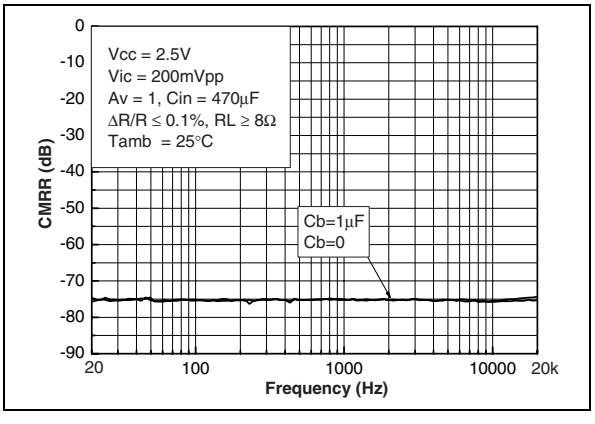


Figure 78. CMRR vs. frequency with random choice condition



4.6 Power dissipation and efficiency

Assumptions:

- Load voltage and current are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{cc})

Regarding the load we have:

$$V_{out} = V_{PEAK} \sin\omega t \text{ (V)}$$

and

$$I_{out} = \frac{V_{out}}{R_L} \text{ (A)}$$

and

$$P_{out} = \frac{V_{PEAK}^2}{2R_L} \text{ (W)}$$

Therefore, the average current delivered by the supply voltage is:

$$I_{CC\ AVG} = 2\frac{V_{PEAK}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is:

$$P_{supply} = Vcc\ Icc_{AVG} \text{ (W)}$$

Then, the **power dissipated by each amplifier** is
$P_{diss} = P_{supply} - P_{out}$ (W)

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - P_{out}$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{out}} = 0$$

and its value is:

$$Pdiss\,max = \frac{2Vcc^2}{\pi^2 R_L} \text{ (W)}$$

Note: This maximum value is only dependent on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when Vpeak = Vcc, so

$$\frac{\pi}{4} = 78.5\%$$

The maximum die temperature allowable for the TS4994 is 125°C. However, in case of overheating, a thermal shutdown set to 150°C, puts the TS4994 in standby until the temperature of the die is reduced by about 5°C.

To calculate the maximum ambient temperature T_{AMB} allowable, we need to know:

- Power supply Voltage value, Vcc
- Load resistor value, RL
- The package type, RTH_{JA}

Example: Vcc=5V, RL=8Ω, RTH_{JA}Flip-Chip=100°C/W (100mm^2 copper heatsink).

We calculate $P_{dissmax}$ = 633mW.

With

$$T_{AMB} = 125°C - RTH_{JA} \times P_{diss} \quad (°C)$$

T_{AMB} = 125-100x0.633=61.7°C

4.7 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4994. A power supply bypass capacitor C_S and a bias voltage bypass capacitor C_B.

C_S has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_S of 1µF, you can expect similar THD+N performances to those shown in the datasheet.

In the high frequency region, if C_S is lower than 1µF, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is higher than 1µF, those disturbances on the power supply rail are more filtered.

C_b has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

4.8 Wake-up Time: T_{WU}

When the standby is released to put the device ON, the bypass capacitor C_b will not be charged immediately. As C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called the wake-up time or T_{WU} and is specified in the tables found in *Electrical Characteristics on page 4*, with C_b=1µF. During the wake-up time phase, the TS4994 gain is close to zero. After the wake-up time period, the gain is released and set to its nominal value.

If C_b has a value other than 1µF, please refer to the graph in *Figure 69 on page 18* to establish the wake-up time value.

4.9 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

Note: In shutdown mode, Bypass pin and Vin+, Vin- pins are short-circuited to ground by internal switches. This allows a quick discharge of C_b and C_{in} capacitors.

4.10 Pop performance

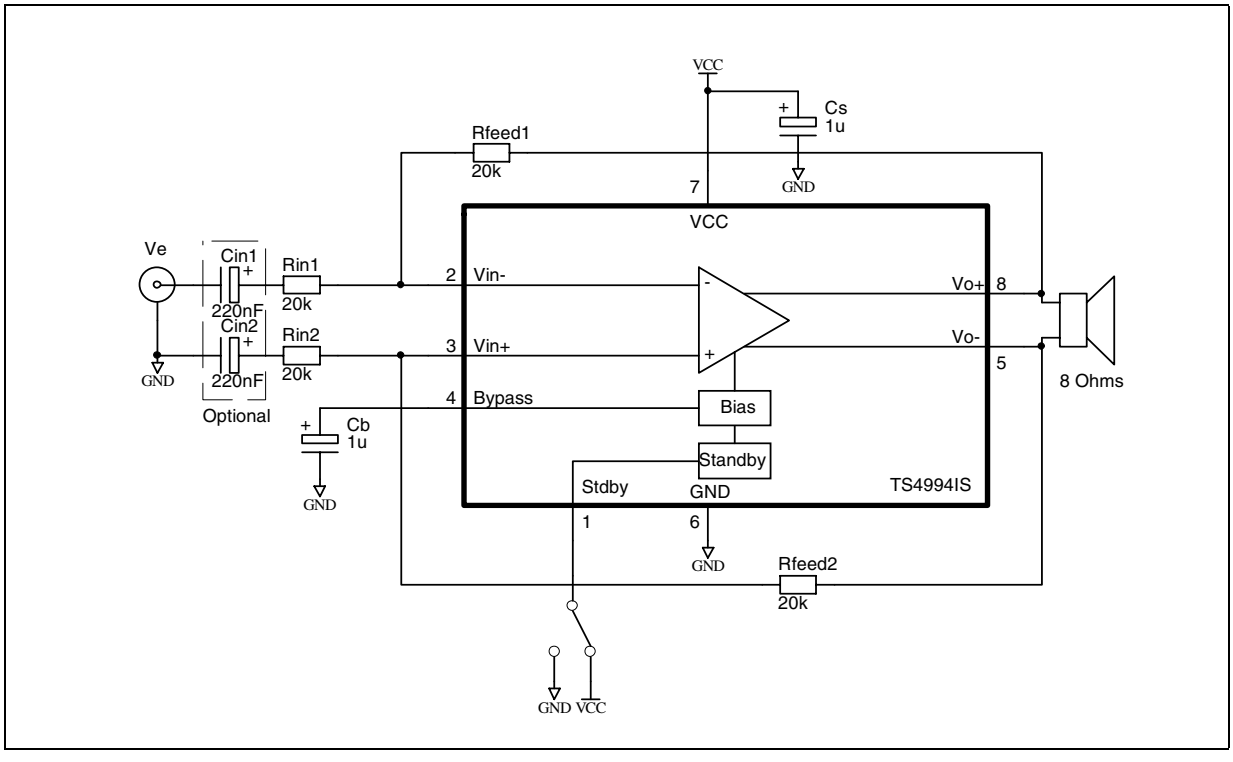
In theory, due to a fully differential structure, the pop performance of the TS4994 should be perfect. However, due to R_{in}, R_{feed}, and C_{in} mismatching, some noise could remain at startup. In TS4994 we included a pop reduction circuitry reach the pop that is theoretical with mismatched components. With this circuitry, the TS4994 is close to zero pop for all common applications possible.

In addition, when the TS4994 is set in standby, due to the high impedance output stage configuration in this mode, no pop is possible.

4.11 Single ended input configuration

It's possible to use the TS4994 in a single-ended input configuration. However, input coupling capacitors areneeded in this configuration. The schematic in Figure 79 shows this configuration using the miniSO8 version of the TS4994 as example.

Figure 79. Single ended input typical application



The components calculations remain the same except for the gain. The new formula is:

$$Av_{SE} = \frac{V_{O+} - V_{O-}}{Ve} = \frac{R_{feed}}{R_{in}}$$

4.12 Demoboard

A demoboard for the TS4994 is available, however it is designed only for the TS4994 in the DFN10 package. However, we can guarantee that all electrical parameters are similar except for the power dissipation.

For more information about this demoboard, please refer to **Application Note AN2013**.

Figure 80. Demoboard schematic

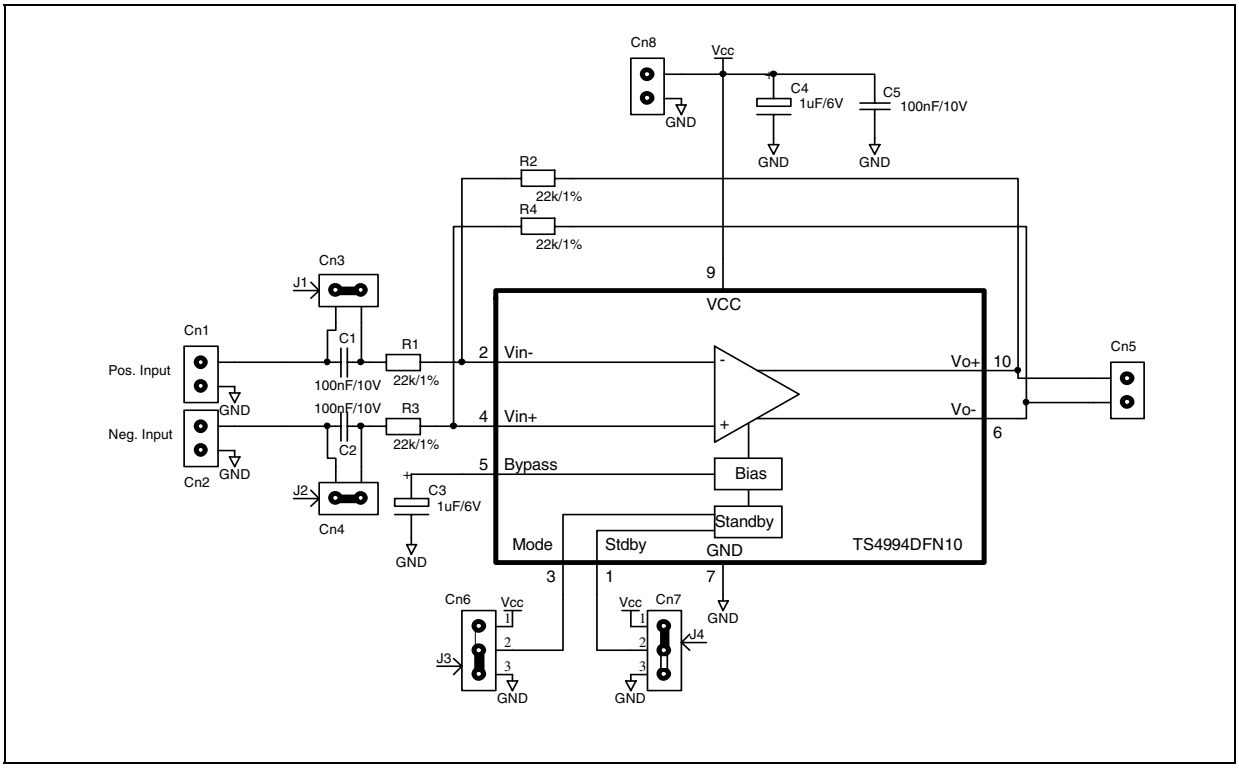


Figure 81. Components location

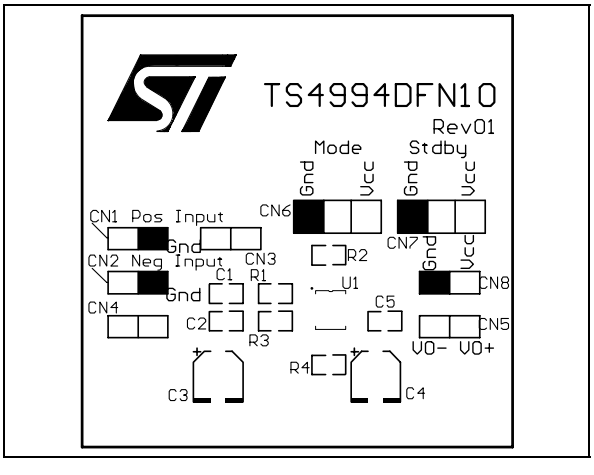


Figure 82. Top layer

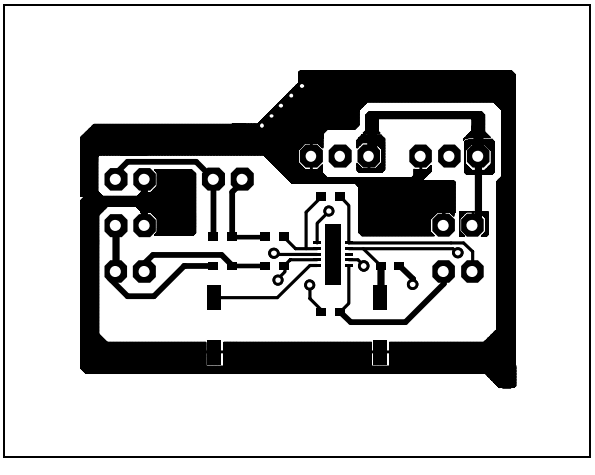
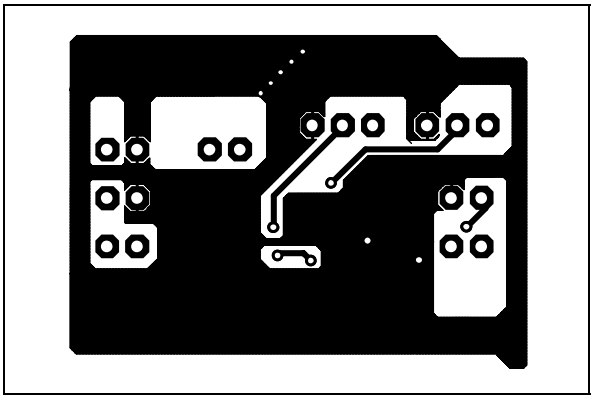


Figure 83. Bottom layer

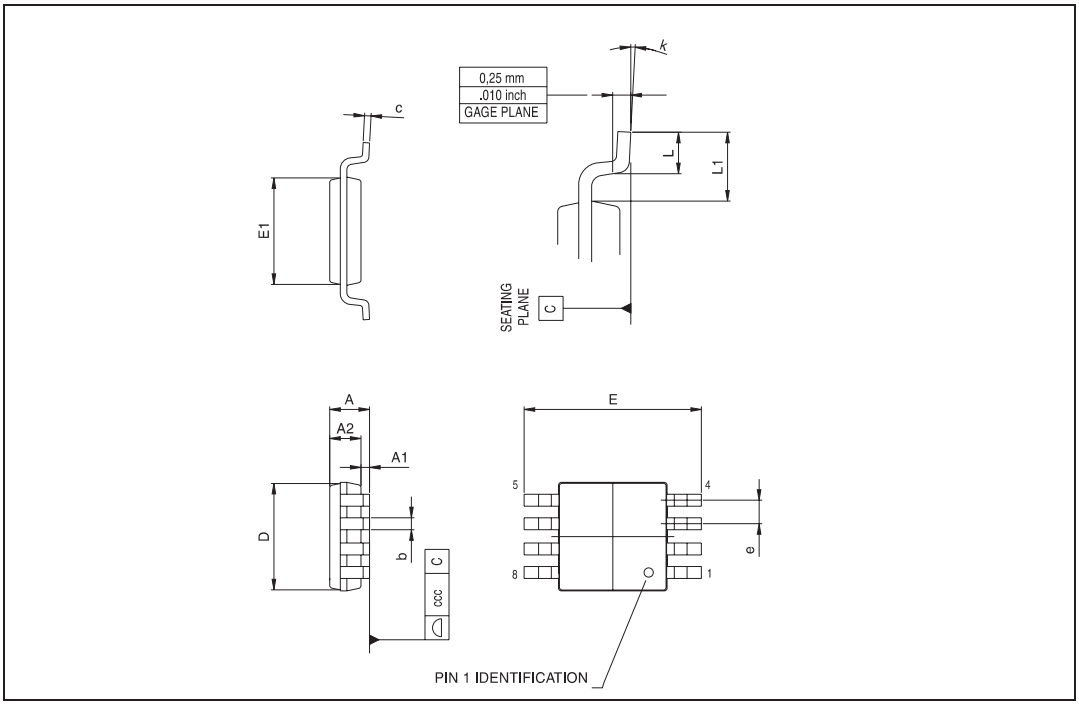


5 Package Mechanical Data

5.1 MiniSO8 package

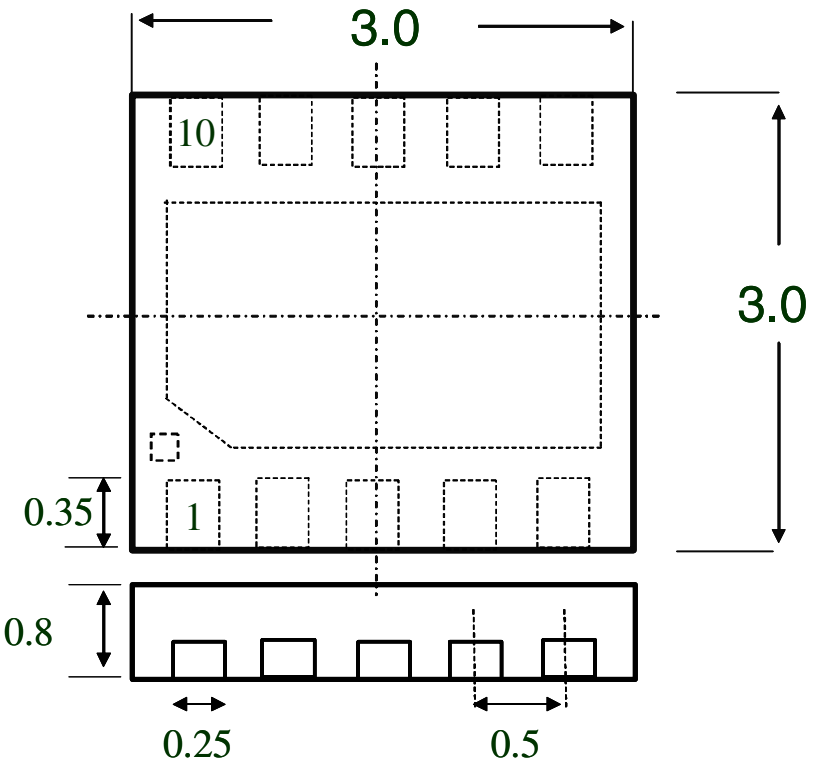
miniSO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



5.2 DFN10 package

Dimensions in millimeters unless otherwise indicated.



*** The Exposed Pad is connected to the Ground**

6 Revision History

Date	Revision	Description of Changes
01 Sept. 2003	1	First Release
01 Oct. 2004		Curves updated in the document
01 Jan. 2005	2	Update Mechanical Data on Flip-Chip Package
17 Mar. 2005	3	Remove datas on Flip-Chip Package