

Transistors

<Di>

Parameter	Symbol	Limits	Unit
Repetitive peak reverse voltage	V_{RM}	30	V
Reverse voltage	V_R	20	V
Forward current	I_F	0.5	A
Forward current surge peak	I_{FSM}^{*1}	2.0	A
Power dissipation	P_D^{*2}	0.5	W / ELEMENT
Junction temperature	T_j	150	°C

*1 60Hz · 1cycle

*2 Mounted on ceramic board

<MOSFET and Di>

Parameter	Symbol	Limits	Unit
Total power dissipation	P_D^{*1}	1.0	W / TOTAL
Range of storage temperature	T_{stg}	-55 to +150	°C

*1 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	10	μA	$V_{GS}=20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	–	–	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	$V_{DS}=30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	–	2.5	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	–	170	240	mΩ	$I_D=1.4A, V_{GS}=10V$
		–	250	350	mΩ	$I_D=1.4A, V_{GS}=4.5V$
		–	270	380	mΩ	$I_D=1.4A, V_{GS}=4V$
Forward transfer admittance	$ Y_{fs} ^*$	1.0	–	–	S	$V_{DS}=10V, I_D=1.4A$
Input capacitance	C_{iss}	–	70	–	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	–	15	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	–	12	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	–	6	–	ns	$V_{DD} \doteq 15V$
Rise time	t_r^*	–	6	–	ns	$I_D=0.7A$
Turn-off delay time	$t_{d(off)}^*$	–	13	–	ns	$V_{GS}=10V$
Fall time	t_f^*	–	8	–	ns	$R_L=21\Omega$
Total gate charge	Q_g^*	–	1.4	2.0	nC	$V_{DD} \doteq 15V, V_{GS}=5V$
Gate-source charge	Q_{gs}^*	–	0.6	–	nC	$I_D=1.4A$
Gate-drain charge	Q_{gd}^*	–	0.3	–	nC	$R_L=11\Omega, R_G=10\Omega$

*Pulsed

<Body diode characteristics (source-drain)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	–	–	1.2	V	$I_S=0.6A, V_{GS}=0V$

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_F	–	–	0.36	V	$I_F=0.1A$
		–	–	0.47	V	$I_F=0.5A$
Reverse current	I_R	–	–	100	μA	$V_R=20V$

Transistors

●Electrical characteristics curves

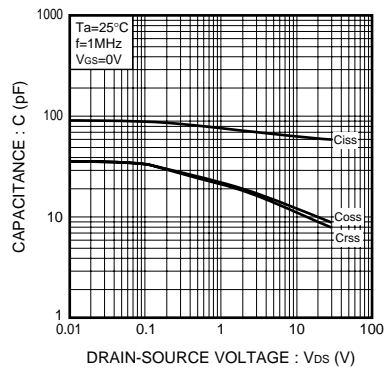


Fig.1 Typical Capacitance vs. Drain-Source Voltage

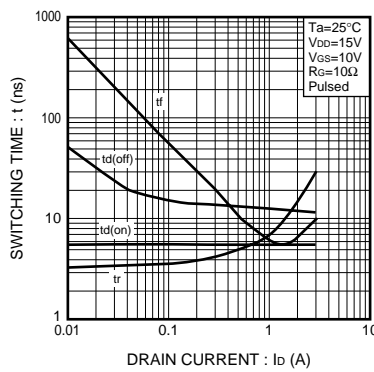


Fig.2 Switching Characteristics

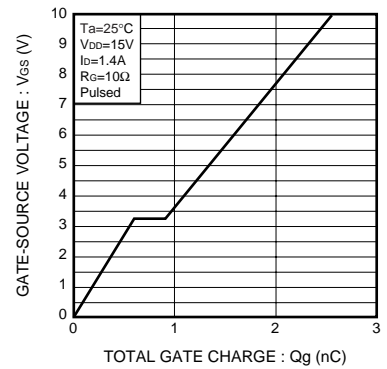


Fig.3 Dynamic Input Characteristics

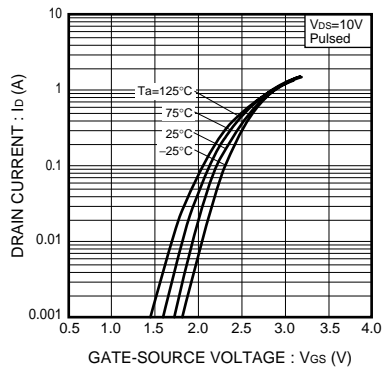


Fig.4 Typical Transfer Characteristics

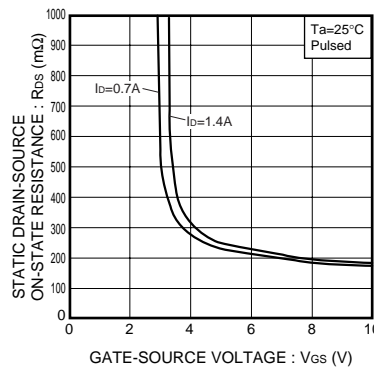


Fig.5 Static Drain-Source On-State Resistance vs. Gate-source Voltage

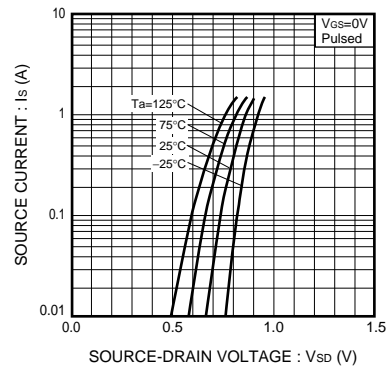


Fig.6 Source Current vs. Source-Drain Voltage

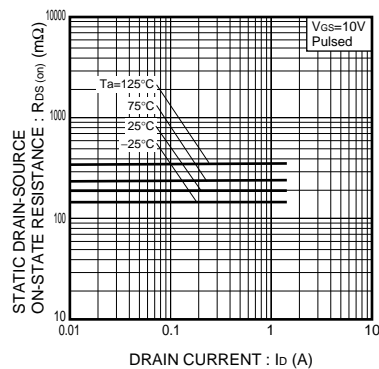


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

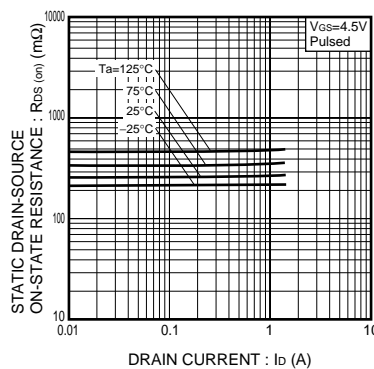


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

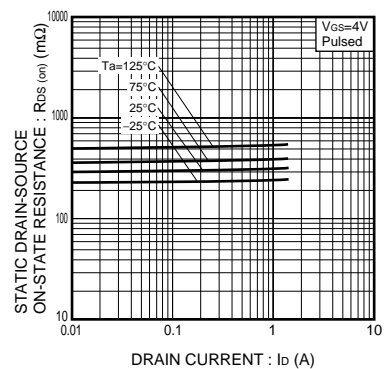


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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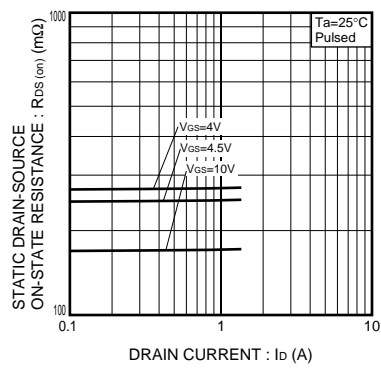


Fig.10 Static Drain-Source On-State Resistance vs. Drain Current (IV)

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