2.5V Drive Pch+SBD MOSFET

US5U38

●Structure

Silicon P-channel MOSFET Schottky Barrier DIODE

● Features

- 1) The US5U38 combines Pch MOSFET with a Schottky barrier diode in a TUMT5 package.
- 2) Low on-resistance with fast switching.
- 3) Low voltage drive (2.5V).
- 4) Built-in schottky barrier diode has low forward voltage.

Applications

Switching

Packaging specifications

	Package	Taping		
Type	Code	TR		
	Basic ordering unit (pieces)	3000		
US5U38		0		

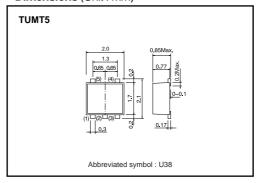
● Absolute maximum ratings (Ta=25°C)

<MOSFET>

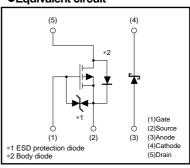
Parameter		Symbol	Limits	Unit		
Drain-source voltage	V_{DSS}	-20	V			
Gate-source voltage	Vgss	±12	V			
Drain current	Continuous	I _D	±1.0	A		
	Pulsed	I _{DP} *1	±4.0	А		
Source current	Continuous	Is	-0.4	A		
(Body diode)	Pulsed	Isp *1	-4.0	A		
Channel temperature		Tch	150	°C		
Power dissipation	P _D *3	0.7	W / ELEMENT			
<di></di>						
Repetitive peak reverse voltage		V _{RM}	25	V		
Reverse voltage	VR	20	V			
Forward current	lF	0.7	A			
Forward current surge peak	I _{FSM} *2	3.0	A			
Junction temperature	Tj	150	°C			
Power dissipation	P _D *3	0.5	W / ELEMENT			
<mosfet and="" di=""></mosfet>						
Power dissipation	P _D *3	1.0	W / TOTAL			
Range of storage temperatu	Tstg	-55 to +150	°C			
A Duration - Durational Addy - 2001 - Asset - 20 Manufacture - 20 Manufact						

^{*1} Pw≤10μs, Duty cycle≤1% *2 60Hz•1cyc. *3 Mounted on a ceramic board

●Dimensions (Unit: mm)



●Equivalent circuit



●Electrical characteristics (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	Igss	_	-	±10	μА	Vgs=±12V, Vps=0V
Drain-source breakdown voltage	V(BR) DSS	-20	_	_	٧	ID=-1mA, VGS=0V
Zero gate voltage drain current	IDSS	-	-	-1	μΑ	V _{DS} =-20V, V _{GS} =0V
Gate threshold voltage	VGS (th)	-0.7	_	-2.0	V	Vps=-10V, Ip=-1mA
Static drain-source on-state resistance	*	-	280	390	mΩ	In=-1A, Vgs=-4.5V
	RDS (on)	-	310	430	mΩ	In=-1A, Vgs=-4.0V
		-	570	800	mΩ	ID=-0.5A, VGS=-2.5V
Forward transfer admittance	Y _{fs} *	0.7	_	_	S	VDS=-10V, ID=-0.5A
Input capacitance	Ciss	_	150	_	pF	Vps=-10V
Output capacitance	Coss	_	20	_	pF	V _G s=0V
Reverse transfer capacitance	Crss	_	20	_	pF	f=1MHz
Turn-on delay time	td (on) *	_	9	_	ns	ID=-0.5A
Rise time	tr *	_	8	_	ns	VDD≒-15V VGS=-4.5V
Turn-off delay time	td (off) *	_	25	_	ns	$R_{\perp} = 30\Omega$
Fall time	t _f *	-	10	_	ns	R _G =10Ω
Total gate charge	Qg *	-	2.1	_	nC	ID=-1A, VDD≒-15V
Gate-source charge	Qgs *	-	0.5	_	nC	Vgs=-4.5V
Gate-drain charge	Q _{gd} *	_	0.5	_	nC	$R_L = 15\Omega$, $R_G = 10\Omega$

^{*} Pulsed

<Body diode (source-drain)>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward voltage	Vsp	_	_	-1.2	V	Is=-0.4A, Vgs=0V

<u><Di</u>>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward voltage	VF	_	_	0.49	V	I==0.7A
Reverse current	lR	_	_	200	μΑ	V _R =20V

Electrical characteristic curves

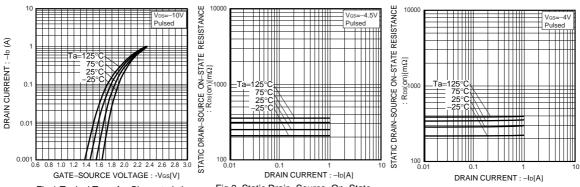


Fig.1 Typical Transfer Characteristics

Fig.2 Static Drain-Source On-State Resistance vs.Drain Current (I)

Fig.3 Static Drain-Source On-State Resistance vs.Drain Current (II)

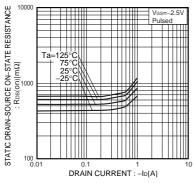


Fig.4 Static Drain-Source On-State Resistance vs.Drain-Current (III)

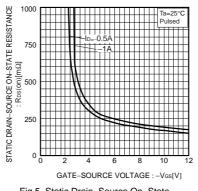


Fig.5 Static Drain–Source On–State Resistance vs.Gate–Source Voltage

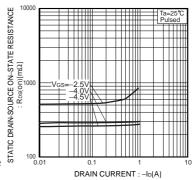


Fig.6 Static Drain–Source On–State Resistance vs.Drain Current

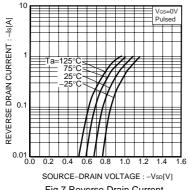


Fig.7 Reverse Drain Current
vs. Source-Drain Current

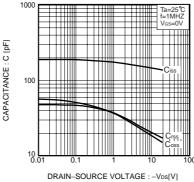


Fig.8 Typical Capactitance vs.Drain–Source Voltage

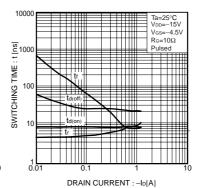


Fig.9 Switching Characteristics

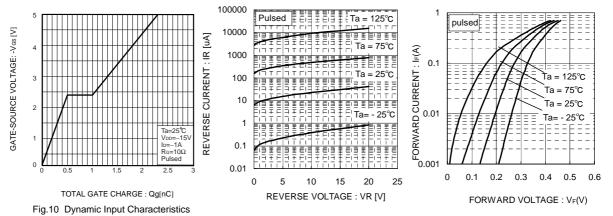


Fig.11 Reverse Current vs. Reverse Voltage

Fig.12 Forward Current vs. Forward Voltage

●Notice

- 1. SBD has a large reverse leak current compared to other type of diode. Therefore; it would raise a junction temperature, and increase a reverse power loss. Further rise of inside temperature would cause a thermal runaway.
 This built-in SBD has low V_F characteristics and therefore, higher leak current. Please consider enough the surrounding temperature, generating heat of MOSFET and the reverse current.
- 2. This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Measurement circuits

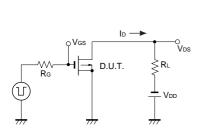


Fig.13 Switching Time Measurement Circuit

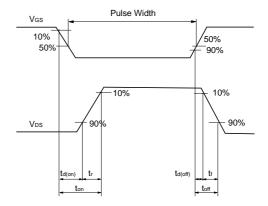


Fig.14 Switching Waveforms

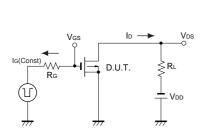


Fig.15 Gate Charge Measurement Circuit

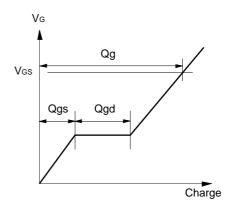


Fig.16 Gate Charge Waveforms

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